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10726-P020US PATENT

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SPECIAL HANDLING REQUEST

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: §
Robert M. Nally, et al. §
§ Group Art Unit: 2609
Serial No.: 08/376,919 § Examiner:
Filed: January 23, 1995 §
§
For: APPARATUS, SYSTEMS AND METHODS §
FOR CONTROLLING GRAPHICS AND §
VIDEO DATA IN MULTIMEDIA DATA §
PROCESSING AND DISPLAY SYSTEMS §

Box PATENT APPLICATION
Commissioner of Patents and Trademarks
Washington, D.C. 20231

PETITION TO MAKE SPECIAL UNDER 37 C.F.R. § 1.102(D)

Sir:

This is a Petition to Make Special the above-identified patent application, the specification of which is enclosed herewith. The basis for this Petition is that Applicants believe that the claims of this invention are being infringed by others.

In accordance with MPEP § 708.02, attached is the Declaration of Robert M. Nally which sets forth facts demonstrating that at least one claim of the subject application defining the disclosed invention, is now being infringed by the making, using or selling by an unauthorized party of devices covered by at least one claim of the subject application.

There is also attached the Declaration of David H. Tannenbaum, attorney for Cirrus Logic, assignee of application Serial No. 08/376,919, filed on January 23, 1995, showing that a comparison of the claims has been made against information

describing the devices that are the subject of the Declaration of Robert M. Nally. The affidavit of Mr. Tannenbaum also recites facts which show that both he and Mr. Nally are very familiar with the state of the art in the area of this application and that all of the claims are allowable over any prior art known to either of them. Mr. Tannenbaum further declares that it is his opinion that it is unquestionable that the accused infringing device will be found to infringe at least one claim of the pending subject application.

The fee of $130.00 for filing this Petition is attached hereto. Please credit any overpayment or debit any underpayment of this Petition fee to Winstead, Sechrest & Minick P.C. Deposit Account No. 23-2426. A duplicate copy of this sheet is attached.

The devices of the present invention, as defined by the claims of the subject applications, are state of the art and are being sold for incorporation into PC's by at least one competitor of Cirrus Logic. Once such devices have been incorporated into a PC it is difficult and very expensive to remove them. Thus, it is critical that any infringement be dealt with at a very early stage.

Because of the very secretive nature of the business, and the care which one competitor takes to insure that another competitor does not obtain its designs until the very latest possible time, as set forth in Mr. Nally's Declaration, it is not practical for Cirrus Logic to obtain an actual device in any short time frame and to review that device in detail for the purpose of comparing an actual device specifically against the claims.

However, as set forth in Mr. Tannenbaum's Declaration, based upon a mutual supplier's comments, the comments of the Vice President for Engineering of the Competitor, and available documentation (see Exhibit B attached to Robert M. Nally's Declaration) describing the technical details of the accused device, the likelihood that an infringement is now occurring based upon the use or sale of an infringing device is certain.

Until a patent issues, which can form the basis for a law suit and discovery, Applicants are unable to gather enough facts to conclusively demonstrate infringement.

Applicants have chosen to not reveal the name of the competitor who is selling the infringing device, nor the name of the mutual supplier, so as to avoid any possible premature embarrassment to any of the parties. Revealing such names at this point, prior to the allowance of any patent claims, could be detrimental to future business relationships between the parties and is not in the best interest of any party, nor of the public. The name "Pixel," which appears on Exhibit A attached to the Declaration of Robert M. Nally, was a company that was acquired by Cirrus Logic.

As set forth in the Declaration of Robert M. Nally, the effective life of products of this nature is less than two years. Thus, if this Petition to Make Special is not granted, the value of any resulting patent will be greatly diminished and the business position of Cirrus Logic with respect to market acceptance of the devices covered by the subject application will likewise be diminished.

In view of the above, applicant requests that this Petition to Make Special be granted, and the examination of the application be advanced.

Respectfully submitted,

David H. Tannenbaum
Registration No. 24,745

Date: April 5, 1995

WINSTEAD SECHREST & MINICK P.C.
5400 Renaissance Tower
1201 Elm Street
Dallas, Texas 75270-2199
(214) 745-5354

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	§	
	§	
Robert M. Nally et al.	§	
	§	Group Art Unit: 2609
Serial No.: 08/376,919	§	
	§	Examiner:
Filed: January 23, 1995	§	
	§	
For: APPARATUS, SYSTEMS AND METHODS FOR CONTROLLING GRAPHICS AND VIDEO DATA IN MULTIMEDIA DATA PROCESSING AND DISPLAY SYSTEMS	§	

DECLARATION OF ROBERT M. NALLY

I, Robert M. Nally, am an employee of Cirrus Logic, having been employed since July 5, 1991.

1. My educational background is Physics, I received a B.S. in Physics from the University of Houston in 1983.

2. I currently hold one U.S. patent, and six applications for patents have been filed in my name in the United States.

3. My principle function at Cirrus Logic has been to design video/graphics controllers. Along these lines I designed a VGA controller with dual data paths from a single frame buffer into the CTR refresh controls. One data path was for Video data (16 bit YUV 422), the other was for 8 bit CLUT data. This design became the subject of Application Serial No. 08/376,919. The application was prepared and the claims drafted to cover a device which was the subject of Cirrus Logic's Private Specification "Functional Specifications Alpine CDX," a copy of which (dates removed) is attached hereto as Exhibit A.

4. Cirrus Logic is a leader in the design of devices of this type. Cirrus Logic has primarily only a few competitors and a limited number of customers in the highly technical field of graphic controllers. Information on competitor's product

specifications is difficult to come by and the design cycles are long (approximately 18 months to 24 months) and expensive (approximately 3 to 4 million dollars). The R&D advances of one company over the other are critical to success or failure of a product. A company could easily lose market leadership for a family of products in a single generation of product design. Every company in this field takes great precautions to keep its products and designs secret from its competitors until the products actually come to market, since lead-time over a competitor is directly related to profitability. Advance information is generally only given to customers for the purpose of sales and to assist customers in the technical integration of a device into their products. Design information is not shared with a competitor.

5. About 18 weeks ago, a person who I know to be the Vice President of a competitor of Cirrus Logic and who had tried to recruit me into his company some months earlier, approached me at a trade show and informed me that his company had in their possession a copy of the Cirrus Logic Private Specification "Functional Specifications for Alpine CDX." Another employee of Cirrus Logic was with me at the time, and heard the statement " I have your spec" made by this V.P. of the competitive company. He repeated this statement a second time when I informed him that Cirrus Logic had not yet released information in the product covered by the Alpine CDX Specification. The V.P. of the competitor then went on to compliment me on the effectiveness of the design. He said, "very nice, very nice."

6. Prior to this time, the competitor in question came to market with a graphics controller that attempted to address the same market but did not effectively address the problem disclosed in application Serial No. 08/376,919. This competitor then obtained Cirrus Logic's "Function Specifications for Alpine CDX" and redesigned their product to add the same functionality as disclosed in application Serial No. 08/376,919.

7. Exhibit B (competitor's name removed), which was shown to me on or about March 29, 1995, is a Preliminary Specification showing how the competitor's product now contains circuitry which performs the exact functions as set forth in the Cirrus Logic "Functional Specifications Alpine CDX" and as contained in application Serial No. 08/376,919. I have been told by at least one mutual customer that this new product from our competitor is now being designed into that customer's systems thereby displacing Cirrus Logic's products having the same functionality.

8. A mutual customer who is known to be working with both Cirrus Logic and the competitor has specifically stated that the competitor's product has the same functionality as the Cirrus Logic product and the customer would like for us to give them more information on our product so that they can verify if the two products are 100% functionally compatible.

9. I, in conjunction with David H. Tannenbaum, patent attorney for Cirrus Logic, have reviewed the claims of application Serial No. 08/376,919, including the claims of the Preliminary Amendment, and I have no question that those claims cover the device which is shown in the competitor's Specification attached hereto as Exhibit B which I believe is now being sold by the Cirrus Logic competitor.

10. Prior to Cirrus Logic's design of the "Functional Specifications for Alpine CDX," there did not exist a product of this type in the marketplace. I am familiar with the prior art devices in the field of video and graphics and do not know of any prior art which is material to the claims, including the claims contained in the Preliminary Amendment of application Serial No. 08/376,919. I have confirmation of this from a major software developer who is in the process of designing an operating system to exploit this new technology. The software developer has access to all of the major competitors in the video graphics field and has stated that Cirrus Logic was first to have a

working product with the functionality covered by application Serial No. 08/376,919.

11. I estimate that the lifetime of this generation of products is less than two years and thus any delay in issuing the patent will be detrimental to Cirrus Logic.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Robert M. Nally

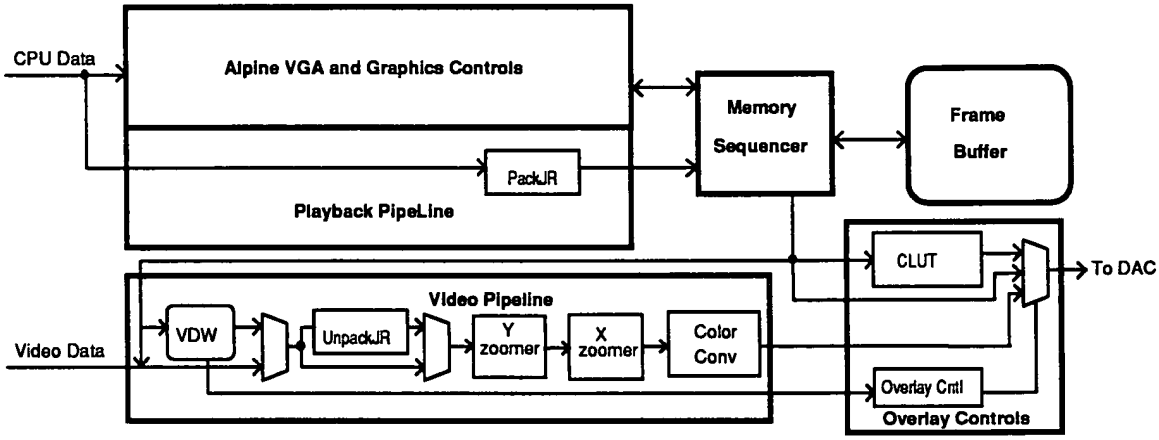
Date: April 4 1995

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EXHIBIT A

I. Boundaries
   A. Maintain 64 bit ALPINE Family compatible. (CL543x).
   B. Added cost for video and playback not to exceed 2.00 .
   C. Baseline VAFC overlay interface for 1024 x 768 or less resolution displays only.

II. Goals
   A. To provide color conversion and display controls for both CinePak and overlayed Video at a cost less than 2.00.
   B. To have sample parts on the market by July 94.
   C. To have high quality 2x and 4x zooming (X and Y) for CinePak playback.
   D. To have 2x and 4x zooming (in X only) for video overlay by meeting VAFC clocking guidelines and using internal zooming to interpolate to actieve display data rates



III. Design Proposal

A. Playback and Overlay Controls

A rectanular video view ports unit will position the video and determine when overlay or the playback window takes place. There are two overlay and one playback modes:

1. Playback

The data is stored in the frame buffer in PackJR format. The data will be stored in "on screen" memory. The Overlay Selector will be directing the data through the graphics pipeline when ever the CRTC is rastering outside the video display window (VDW) and will be directing the data through the video pipeline when the CRTC is rastering inside the VDW. NO OVERLAY COLOR KEYING is involved in the operation of this mode, the playback window framing in the VDW will be the only means of determining the path the data takes when going from the frame buffer to the display screen.

2. Digital Video Overlay

The Overlay Selector will be selecting graphical data from the graphics pipeline when ever the CRTC is rastering outside the video display window (VDW) and will be selecting overlayed video coming from the VAFC port when the CRTC is rastering inside the VDW. The Overlay Color Key will be the only means of controlling the overlay.

3. Analog Video Overlay using Alpha Values.

The alpha value is output through the VPort in digital form in sync with the RGB analog outputs in this mode. This is to allow customers to control external analog mixers with the 8 bit alpha value. Using the alpha value and the VPort in this mode prevents either from being used in any other mode or configuration. This mode only applies to the aRGB 8:8:8:8 mode.

B. PackJR

When Alpine CDX is in an eight bit graphics mode, all playback data will be stored in the frame buffer in a Packed or encoded YUV 4:1:1 format. The data will actually be placed in "on screen" memory in the frame buffer, even if it is being X zoomed on the backend. PackJR is an encoded error diffused YUV color space. The data is stored in memory in a raster oriented format where each four pixels in a raster line are packed into one 32 bit word. The following table shows how the four pixels are formatted into one 32 bit word.

Y3	Y2	Y1	Y0	U	V
D<31:27>	D<26:22>	D<21:17>	D<16:12>	D<11:6>	D<5:0>

The played back video data is sent to Alpine CDX in a YUV 4:2:2 format. Alpine VFW , after performing any required Y zooming on the data, will then pack the YUV data into the PackJR format before transfering it to the frame buffer. During screen refresh time, the packed data is directed to the video pipeline, by the VDW, where it is unpacked and color converted to true color RGB.

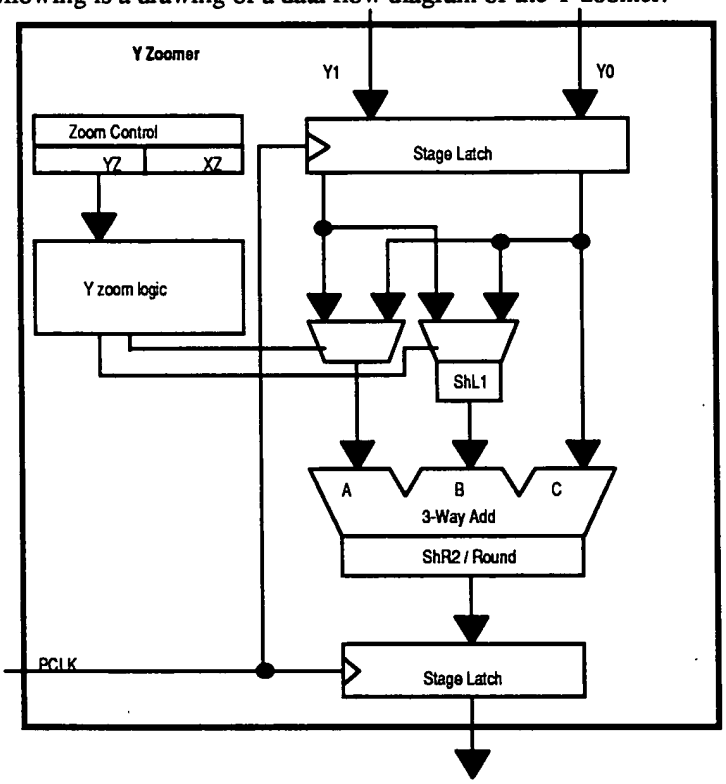
C. Zoom Controls

A quarter phase bilinear interpolator is proposed for zooming CinePak and video streams. Zooming will be 2-diminsional for fixed zoom ratios 1:2 and 1:4. Support for non-integar zooming will be looked at, whether we support it are not will depend on cost.

The Y zoomer is a quarter phase interpolator. It performs only the following zoom functions:

	A		B		C		Line
Yout =	1/4 Y0	+	1/2 Y0	+	1/4 Y0;		Y(0)
Yout =	1/4 Y1	+	1/2 Y0	+	1/4 Y0;		Y(1/4)
Yout =	1/4 Y0	+	1/2 Y1	+	1/4 Y0;		Y(1/2)
Yout =	1/4 Y1	+	1/2 Y1	+	1/4 Y0;		Y(3/4)

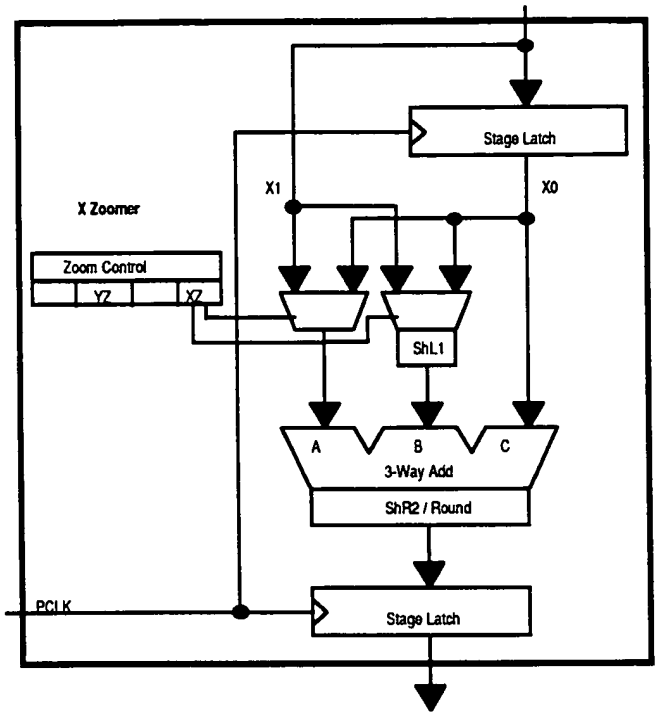
The Y zoomer is a "frontend" zoomer and sets between the host bus and the packJR unit. All Y zooming is performed on the data before it is placed in the frame buffer. The software will be responsible for staging the appropriate lines of data into the frontend of the Y zoomer. The Y zoomer will have the capacity to store only a few pixels of each line at a time, therefore the software has to be a "span" oriented and not a "raster" oriented driver. The following is a drawing of a data flow diagram of the Y zoomer.



The X zoomer a quarter phase interpolator as well, and the same four equations apply to the X dimension.

	D		E		F	Pixel
Xout =	1/4 X0	+	1/2 X0	+	1/4 X0;	X(0)
Xout =	1/4 X1	+	1/2 X0	+	1/4 X0;	X(1/4)
Xout =	1/4 X0	+	1/2 X1	+	1/4 X0;	X(1/2)
Xout =	1/4 X1	+	1/2 X1	+	1/4 X0;	X(3/4)

The X zoomer is a "backend" zoomer and sets between the color converter and the DAC.
All data loaded into the X zoomers will always be RGB 8:8:8 data, therefore YUV data will have to color converted before it is sent to the X zoomer.



D. Color Conversion

E. Video Display Windows (VDW)

The VDW will be used in different ways by the different overlay modes.

F. Video Port

The table below shows the pin definitions for the current Alpine video interface, the 16-bit VAFC interface, and the MPEG video interface. Since we could not arrive at an acceptable method to multiplex the 16-bit VAFC data bus into an 8-bit Alpine video port, the 16-bit VAFC interface shown below is proposed. The additional eight data lines (P[15:8]) use four pins that were previously reserved for the Audio WavePort, two pins that are used in the current Alpine video interface (but are not required for VAFC), and two pins from the display memory interface.

The decision to eliminate the WavePort is based on customer feedback and on meetings with Crystal. The important issue for Alpine customers is SoundBlaster compatibility, which WavePort does not provide.

The loss of the two frame buffer memory interface pins will have the following affect:
- No support for 256Kx16, dual WE#, asymmetric devices. (Note that dual CAS# devices are recommended over dual WE# in Appendix B7-2 of the Alpine Technical Reference Manual.)
- No support for 4Mbyte display memory.

The VAFC interface timing will probably prevent the use of the optional configuration EEPROM interface. P8, P9, P13, and P14 would need to be tri-stated to allow the EEPROM interface signals to function. Due to the possibility of 20ns delay from DCLK to VCLK, any delay on the P bus could cause a timing violation.

The MPEG interface mode uses a subset of the signals used by the 16-bit VAFC interface.

Table 1: Alpine-CDX pin definitions

	Current Alpine		16-bit VAFC I/F		MPEG I/F	
pin #	name	type	name	type	name	type
16	MCLK	I/O	DCLK	O	DCLK	O
96	VSYNC	O	VSYNC	O	VSYNC	O
98	HSYNC	O	HSYNC	O	HSYNC	O
105	TWR#	I	P12	I	P12	I
106	EEDI	I	P13	I	P13	I
107	EECS	O	P14	I	P14	I
108	rsvd		P15	I	P15	I
109	OVRW#	O	GRDY	O	GRDY	O
110	P0	I/O	P0	I	P0	I
111	P1	I/O	P1	I	P1	I
112	P2	I/O	P2	I	P2	I
113	P3	I/O	P3	I	P3	I
115	P4	I/O	P4	I	P4	I
116	P5	I/O	P5	I	P5	I
117	P6	I/O	P6	I	P6	I
118	P7	I/O	P7	I	P7	I
120	EVIDEO/EEDI	I/O	EVIDEO#	I	EVIDEO#	-
122	ESYNC/EESK	I/O	P8	I	P8	I
123	EDCLK	I/O	P9	I	P9	I
125	DCLK	I/O	VCLK	I	-	-
126	BLANK#	I/O	BLANK#	O	-	-
169	RAS0#/OE#	O	P10	I	P10	I
190	MA9	O	P11	I	P11	I

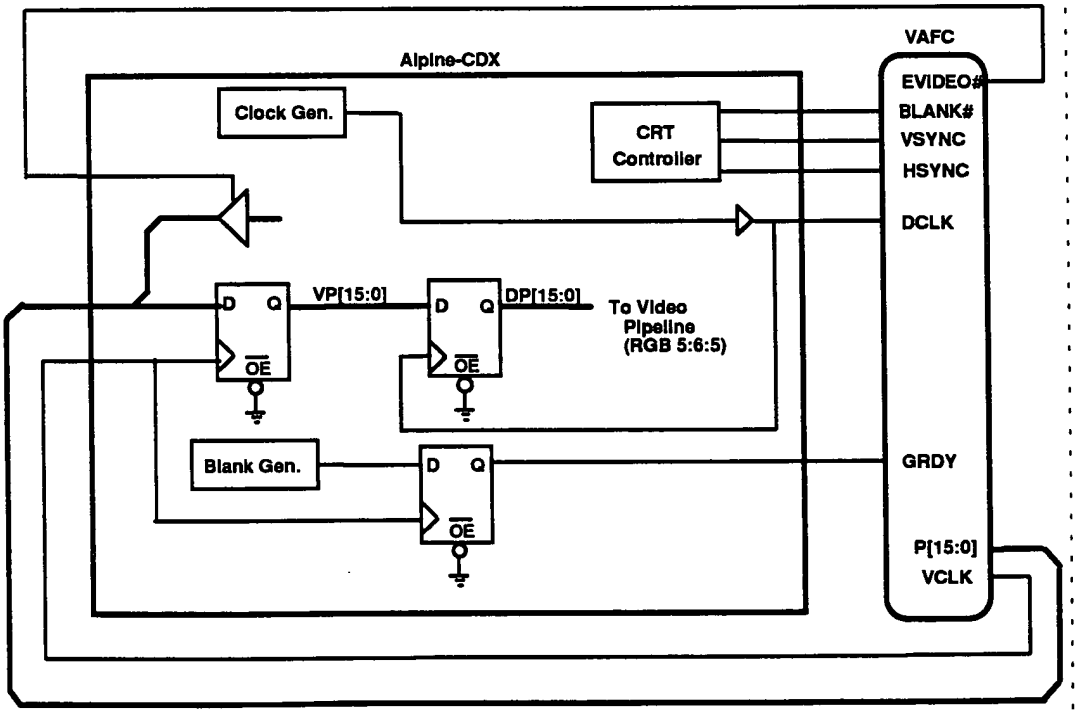
VAFC Interface:

Figure 1 shows the Alpine-CDX interface to VAFC in baseline input mode. VAFC data is referenced to VCLK (which could be delayed as much as 20ns from DCLK) so the first register stage clocks Pixel bus data on the rising edge of VCLK. The next register stage clocks the data on the rising edge of DCLK. From there, data is presented to the video pipeline. The data format is RGB 5:6:5.

The VAFC baseline input specification requires the video data to be synchronized to the graphics data, so Alpine-CDX is the source of the syncs and blanking signals. Alpine-CDX sources DCLK (37.5MHz max) and the video board returns it as VCLK. Alpine-CDX generates GRDY (referenced to VCLK) to indicate to the video system that it is ready to receive data.

The VAFC specification requires that the graphics system power up in baseline 8-bit palletized output mode (EVIDEO# high). The following pins are driven by Alpine-CDX in baseline output mode: P[7:0], DCLK, VSYNC, HSYNC, and BLANK#.

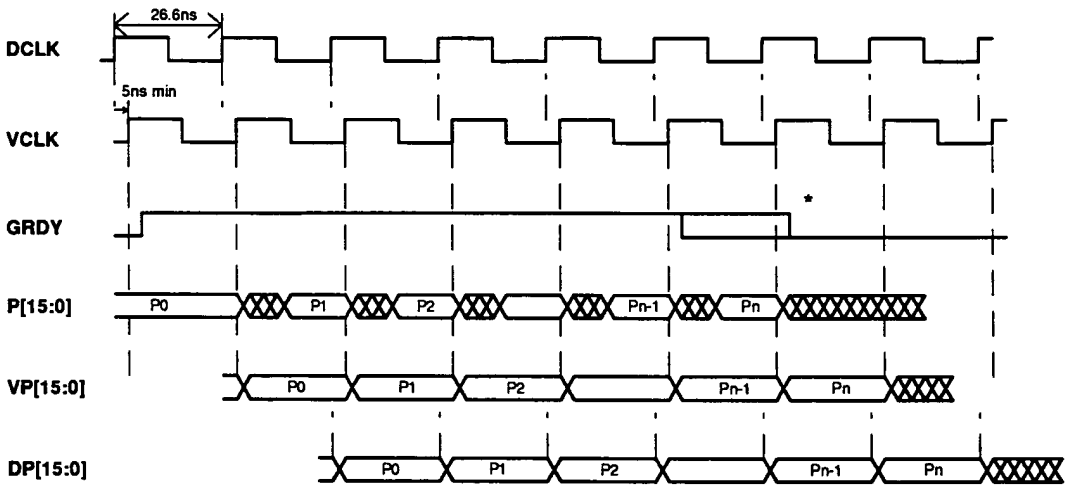
Figure 1: VAFC Baseline Input Interface



The delay from DCLK to VCLK is specified to be a minimum of 5ns up to a maximum of 20ns in the VAFC spec. The following two timing diagrams show the interface timing for the

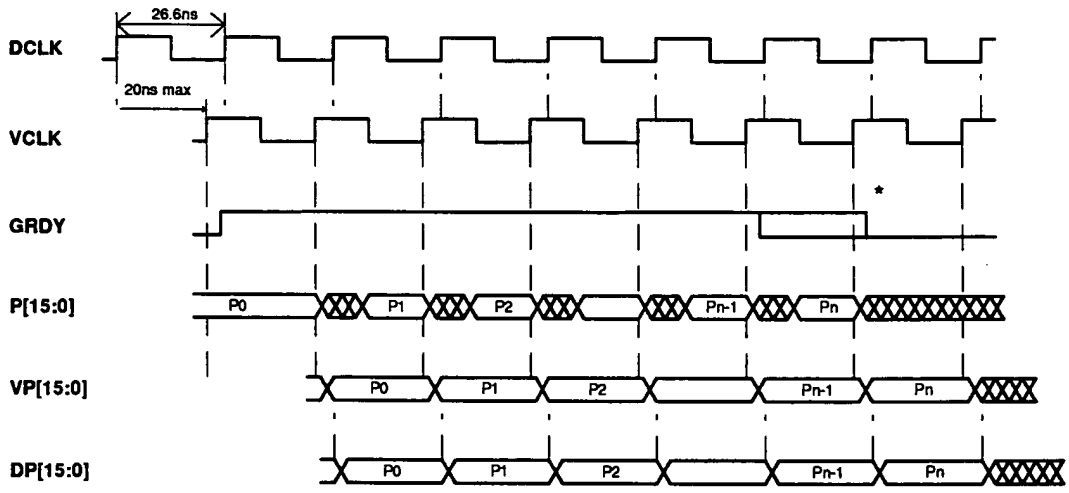
two extremes. Figure 2 shows the case where the delay between DCLK and VCLK is minimum and Figure 3 shows the case where the delay between DCLK and VCLK is maximum. In each diagram, the vertical dashed lines are used for signals referenced to VCLK and the vertical dash-dot lines are used for signals referenced to DCLK. Note that in either case, the first data value input to the video pipeline can be referenced back to the clock cycle where GRDY was asserted.

Figure 2: VAFC Baseline Input Timing (For Minimum DCLK to VCLK Delay)



* VAFC specifies that GRDY is active for N-1 cycles (where N is the number of data transfers).
A configuration bit will allow GRDY to be active for N cycles.

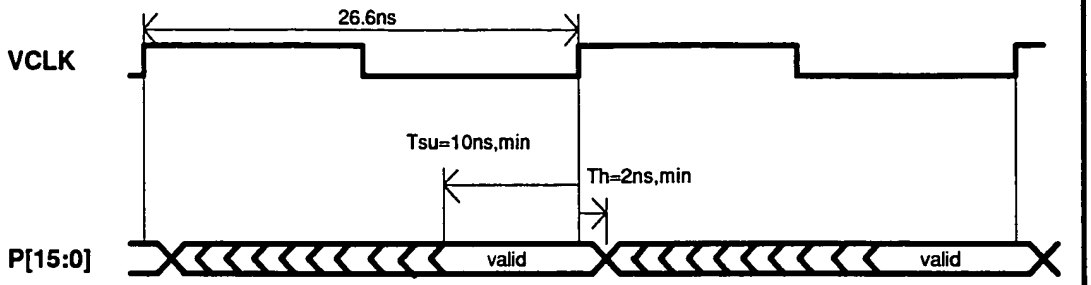
Figure 3: VAFC Baseline Input Timing (For Maximum DCLK to VCLK Delay)



* VAFC specifies that GRDY is active for N-1 cycles (where N is the number of data transfers).
A configuration bit will allow GRDY to be active for N cycles.

Figure 4 shows the detailed input timing that Alpine-CDX needs to meet in VAFC baseline mode.

Figure 4: VAFC Baseline Input Timing (Detailed Data Input Timing)



MPEG Interface:

Figure 2 shows the Alpine-CDX interface to the Cirrus MPEG chip. The MPEG interface is very similar to the VAFC interface. The first register stage clocks Pixel bus data on the rising edge of VCLK (which is externally connected to the DCLK output). The next register stage clocks the data on the rising edge of DCLK. From there, data is presented to the video pipeline. The data format is PackJr if Y-zooming is used or YUV 4:2:2 if Y-zooming is not used..

Alpine-CDX is the source of the syncs, DCLK, and GRDY.

Figure 5: MPEG Input Interface

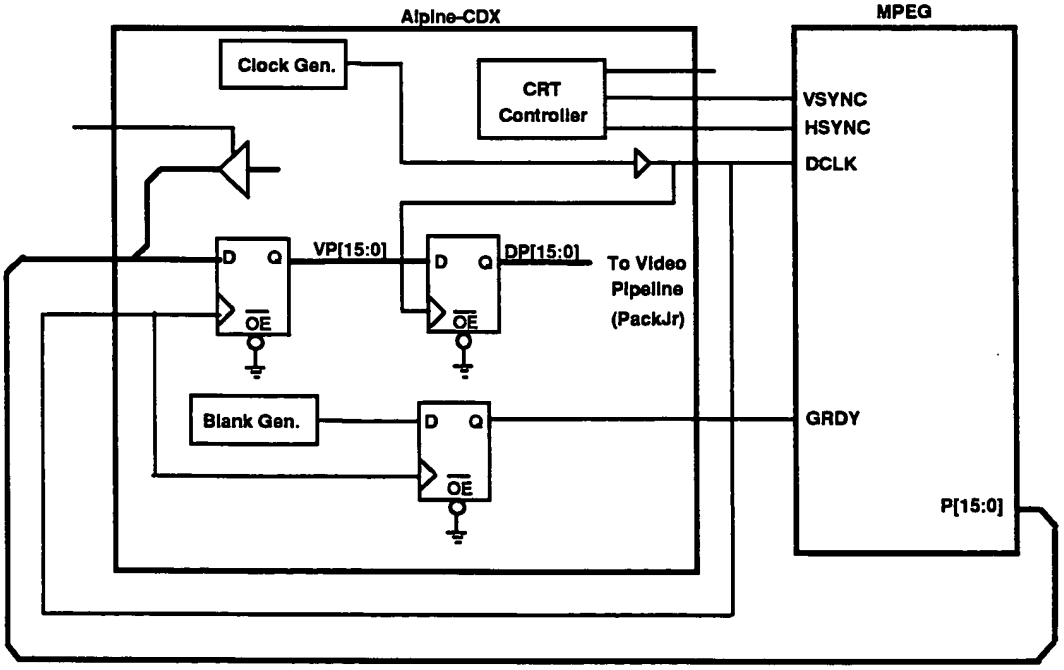


Table 2 shows the storage format for four pixels of PackJr data. Alpine-CDX requires that the least-significant two bytes be transferred first, followed by the most-significant two bytes.

Table 2:

Y3	Y2	Y1	Y0	U	V
D<31:27>	D<26:22>	D<21:17>	D<16:12>	D<11:6>	D<5:0>

Support for 2X and 4X Y-zooming using an interpolation algorythm requires the Cirrus MPEG decoder to output pixel data from two lines at a time. This is best illustrated by example:

For Y-zooming with a ratio of 1:2:

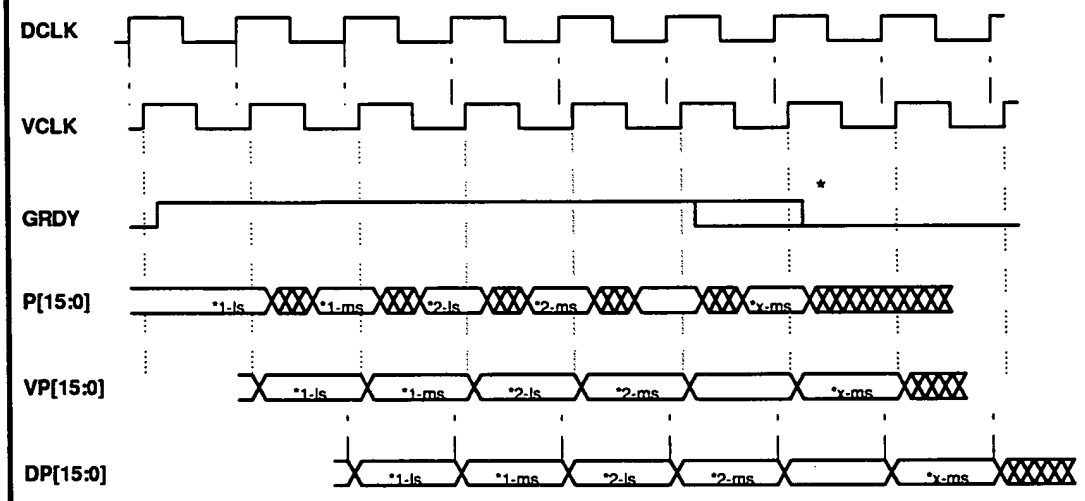
1. The MPEG decoder sends the first four pixels of the first input line followed by the first four pixels of the second input line. Then it sends the second four pixels of the first line followed by the second four pixels of the second line. The MPEG decoder continues to alternately send four-pixel segments from the first and second input lines until both lines have been transferred. As the MPEG decoder is sending pixels from the first two lines, Alpine-CDX outputs the pixels from the first input line and throws away the second line pixels.
2. The MPEG decoder sends the first and second lines again, in alternating four-pixel segments, as described above. This time Alpine-CDX generates a new line two output from the two input data lines using the interpolation algorythm.
3. The MPEG decoder sends pixel data from the second and third input lines in the same four-pixel alternating scheme described in 1. Alpine-CDX generates output line three from input line two and throws away the pixels from input line three.
4. The MPEG decoder sends the second and third lines again, in alternating four-pixel segments. This time Alpine-CDX generates a new line four output from the two input data lines using the interpolation algorythm.
5. This sequence continues until the last line of input video is reached. The MPEG decoder will send two lines of video to Alpine-CDX using the alternating four-pixel scheme, but all the data comes from the last line.

For Y-zooming with a ratio of 1:4, the same transfer scheme is used except each pair of lines from the MPEG decoder is sent four times.

Figure 6 shows the timing for the MPEG decoder interface. The delay from DCLK to VCLK will be minimal. The meaning of the data are as follows:

*1-ls: least-significant two bytes of the first 4-pixel PackJr segment from line n.
*1-ms: most-significant two bytes of the first 4-pixel PackJr segment from line n.
*2-ls: least-significant two bytes of the first 4-pixel PackJr segment from line n+1.
*2-ms: most-significant two bytes of the first 4-pixel PackJr segment from line n+1.
:
:
*x-ms: most-significant two bytes of the last 4-pixel PackJr segment from line n+1.

Figure 6: MPEG Input Timing (DCLK connected directly to VCLK)



* VAFC specifies that GRDY is active for N-1 cycles (where N is the number of data transfers).
A configuration bit will allow GRDY to be active for N cycles.

EXHIBIT B

PRELIMINARY

GUI and Video Accelerator

Features

Complete Hardware Compatibility
- PCI rev. 2 and VL Bus 2.0 compliant
- Supports VESA DDC, DPMS, and VAFC standards
- 100% IBM® VGA compatible on BIOS, register, and hardware levels
- 208-pin PQFP package

Accelerated Graphics Functions
- Internal 64-bit memory data bus
- 256 Raster Operations (ROPs) for 8-bits per pixel (PseudoColor), 15-/16-bits per pixel (HiColor), and 24-bit per pixel (TrueColor) graphic modes
- Optimized graphic engine for BitBLTs, line drawing, short stroke vectors, rectangle fills, trapezoid fills, clipping, ROP4 assist, and text transfer
- Accelerated color expansion modes
- Internal hardware cursor (64x64x2 or 32x32x2)
- Built-in 64x32 pattern register

Extended Display Resolution
- High resolution non-interlaced display through 1280x1024-256, 1024x768-64K, 800x600-64K colors, or 640x480-16M colors
- Extended text modes (80 or 132 columns by 25, 30, 43, or 60 rows)

Highly Integrated Design
- Fully integrated 24-bit TrueColor DAC with color look-up table, 135 MHz clock synthesizer, read cache, command FIFO, and GUI accelerator
- 256x18 color look-up table with HiColor and TrueColor bypass mode support
- Two wire interface to EEPROM or VESA DDC

Improved Manufacturability
- Pin scan testing
- Signature analysis

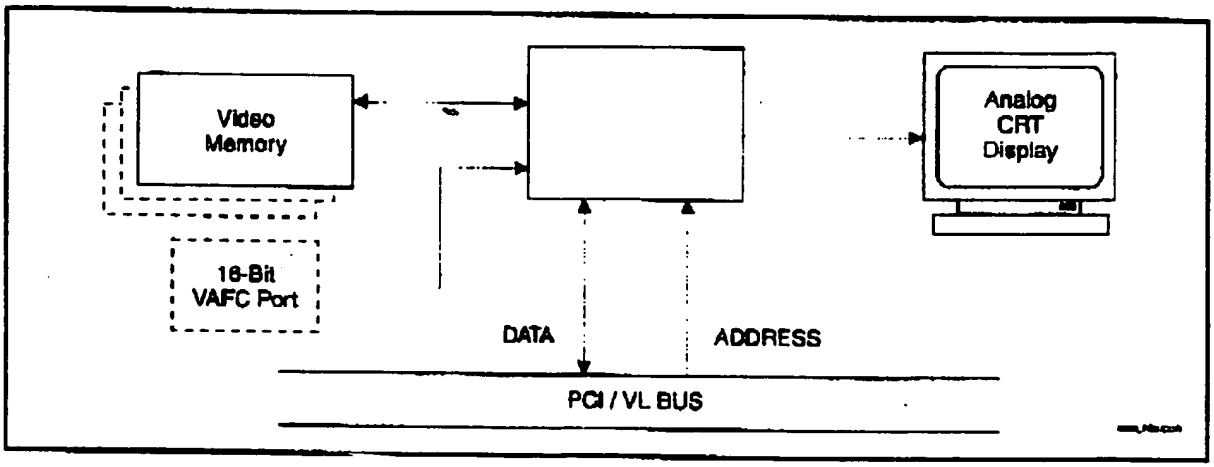
Software CODEC Acceleration
- On-chip Color Space Conversion (CSC), H/V scaling, and overlay control for 30 FPS software video CODEC display
- 16-bit VAFC video stream can be merged for dual-video display

Simple Bus Interface Support
- Flexible Bus Interface Unit for zero wait state 32-bit glueless connection to VESA Local Bus 2.0 (VL Bus) or PCI 2.0 Bus with no additional TTL
- PCI burst mode support
- Big-endian and little-endian format
- Memory Mapped I/O or PCI and VL Bus
- Zero-wait state host write buffer and read cache

"Deep Green PC" Power Management
- VESA Display Power Management Signaling (DPMS) compatible
- RAMDAC power-down and clock idle interface
- Support for graphics system shutdown

Flexible Display Memory Interface
- 1 MB to 4 MB display memory configuration with densities of 256Kx4, 256Kx8, and 256Kx16
- Only two 256Kx16 DRAMs for 1024x768-256
- Dynamic frame buffer sharing
- Extended Data Out (EDO) mode DRAM

Extended Performance Options
- Support for WRAM
- DCI acceleration and dual-mixed mode display



Application Diagram

Overview

The is a 100% pin-compatible version of the 64-bit T GUI Accelerator. The includes all advanced graphical acceleration features of the original and extends the feature set to the acceleration of software video CODEC standards such as Cinepak, Indeo, and MPEG. Video acceleration features include on-chip hardware Color Space Conversion (CSC), Horizontal/Vertical Scaling, and Overlay Control.

The shared feature set consists of a DRAM-based 64-bit accelerator with 135 MHz TrueColor DAC and clock-synthesizers integrated on chip. The devices include glueless VL and PCI Bus interfaces. Graphic acceleration functions include line-draw, expand, 256 ROPBLTs, and trapezoid fill for high-performance Windows operation. Green PC support includes VESA compliant Display Power Management (DPMS) and extended features such as RAMDAC shutdown. BIOS support includes DDC1 and 2B and full VESA BIOS Extensions (VBE). The 208-pin package and integration of RAMDAC, clock-synthesizers and video-acceleration make the devices an ideal solution for add-in and planar board graphic designs.

Complete Hardware Compatibility

The is the first of 64-bit product family. It is fully compliant with the PCI rev. 2 and the VL Bus 2.0 specifications and also supports VESA DDC and VAFC standards. The is 100% IBM VGA and compatible on the BIOS, register, and hardware level, allowing full compatibility with virtually any VGA application software. Additionally, the features a 208-pin PQFP package with optimized pin assignment for efficient PCB layout.

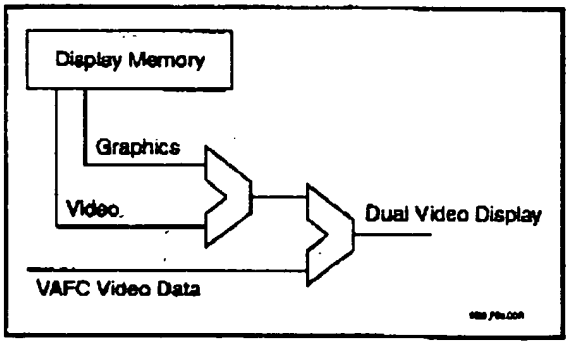
Accelerated Graphics Functions

The 64-bit graphics engine significantly boosts graphics performance through specialized hardware that accelerates the most frequently used GUI operations. The 64-bit memory data bus provides a higher memory bandwidth, which allows greater and faster data transfer rates for improved system throughput. Functions directly supported in hardware include: BitBLT, image and text transfer, line draw, short stroke vector draw, rectangle fills, clipping, and trapezoid fills. Graphic functions are optimized further by a 64-bit internal data bus and a hardware cursor operation (64x64x2 or 32x32x2 pixel image) which offloads the CPU. The graphics engine also supports 256 Raster Operations (ROPs) for 8 bpp (PseudoColor), 15 and 16 bpp (HiColor), and 24 bpp (TrueColor) graphic modes. Additionally, memory-mapped I/O registers on the graphics engine provide faster access time. These advanced functions combine to allow significant performance increases over standard Super VGA designs, providing outstanding graphics acceleration on GUIs such as Microsoft Windows and similar applications.

Software CODEC Acceleration

Software CODECs such as Indeo, Cinepak, and MPEG can be accelerated with the hardware video acceleration features. The places video data in off-screen graphics display memory and accelerates software CODEC operation by providing Color Space Conversion (CSC), Hardware Vertical/Horizontal Scaling and Overlay Control. The hardware video acceleration features allow up to 30 FPS motion video from CD-ROM without the need for expensive hardware options. Color format support includes YUV 4:2:2 and 8-bit RGB. The includes Windows '95™ compliant DCI drivers for maximum video compatibility.

The 16-bit VAFC port is baseline compatible with the VESA video standard. The video stream from the VAFC port is merged with the combined video and graphics image coming from the display memory to allow dual live-video displays, as seen below:



Improved Manufacturability

The is designed for high-volume PC markets requiring the lowest possible manufacturing costs. To help achieve this, the includes pin-scan testing for detecting opens and shorts on a manufacturing floor bed-of-nails. Also, an Internal Signature Analysis Circuit with built-in accumulator and timing circuit provides for easy testing of both integrity of the frame buffer and a large part of the functional circuit. No external circuitry is required to support either of these features, except a bed-of-nails PC board tester.

Extended Display Resolution

Support of non-interlaced 1024x768-256, 1024x768-64K, or 800x600-16M colors provides "full spectrum" color. Extended text modes of 80 or 132 columns by 25, 30, 43, or 60 rows allow an extended text area frequently used in many spreadsheet and database applications. Extended graphics and text modes are supported by software application drivers that provide a "ready-to-go" solution minimizing the need for additional driver development. The software application drivers support the following applications:

Microsoft Windows™	Ventura Publisher™
Wordstar™	Microsoft NT™
Autoshade™	CADKEY™
OS/2™	Lotus 1-2-3™
FrameMaker™	AutoCAD™
P-CAD™	Quattro Pro™
Microsoft Word™	VersaCAD™
Symphony™	WordPerfect™
SCO X-Windows™	

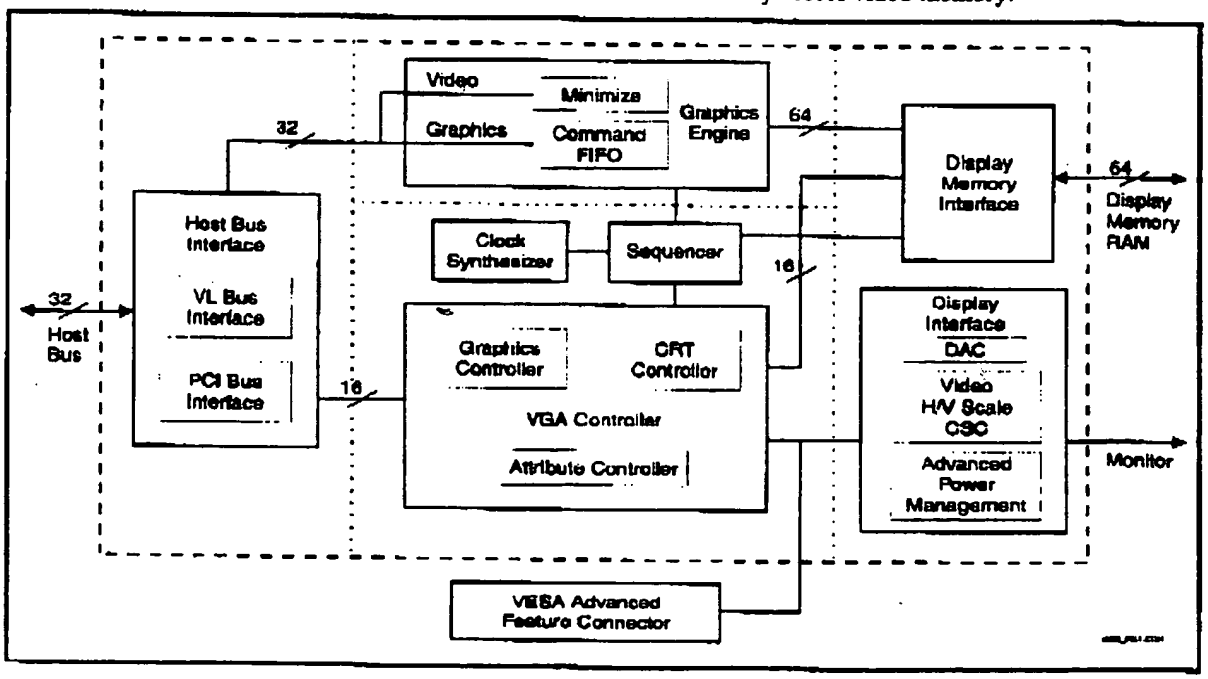
The also supports other VGA compatible applications using their own respective software drivers.

Highly Integrated Design

The highly integrated design offers a "no TTL" solution for cost-effective, high-performance graphic subsystem designs for the IBM PC and compatible systems. The integrated 24-bit TrueColor DAC and 135 MHz programmable clock synthesizer provide a complete graphic subsystem with the addition of only one DRAM. The also includes a fully integrated GUI accelerator, read cache, and command FIFO that optimize memory bandwidth and maximize graphics performance. No TTL support is needed for the system bus or display memory interface and a two-wire communications interface allows direct support of either an external EEPROM or VESA DDC monitor interface.

Simple Bus Interface Support

A flexible Bus Interface Unit (BIU) provides low-cost, single-chip solution for IBM PC or compatibles on 32-bit VESA Local Bus (VL Bus) or PCI Bus interfaces. Combined with "glueless" connections, the BIU allows an efficient design path for quick and easy integration to future generation PCs. The supports VL Bus speeds up to 50 MHz and PCI Bus speeds up to 33 MHz. Also, linear display memory addressing, zero-wait state host write buffer, and read cache increase operating speeds and contribute to peak performance levels. Graphics system throughput is further enhanced by a command FIFO, allowing maximum bus transfer speed for applications such as Windows or AutoCAD that directly access video memory.



Block Diagram

"Deep Green PC" Power Management

The . supports VESA Display Power Management Signaling (DPMS), which decreases monitor power consumption after a predetermined timeout period. "Deep Green PC" goes beyond the conventional VESA DPMS specification. VESA DPMS power-down states (ready, standby, suspend, and off) specify HSYNC and VSYNC signals to control the monitor power-down state. All power management functions are regulated using DMCLK, VMCLK, and RAMDAC control registers.

BIOS extensions can automatically turn off the RAMDAC and reduce clocks when DPMS power-down states are activated since the display no longer needs analog RGB signals. In addition, all registers in the offer read/write access allowing the complete shutdown of the graphics subsystem.

Flexible Display Memory Interface

The . features display memory configurations from 1 MB to 4 MB and supports a wide range of DRAM configurations (256Kx4, 256Kx8, and 256Kx16). A 32-bit or 64-bit memory bus interface, dynamic frame buffer sharing, and programmable DRAM timing provides a flexible interface that maximizes timing for increased performance, offering system designers a choice of power/performance options. A minimum DRAM interface requirement of two 256Kx16 DRAMs for 1024x768-256 color SVGA lowers chip count, system cost, and board space for cost-effective design solutions. The display memory interface also supports symmetrical or asymmetrical configuration and Dual CAS or Dual WE (Write Enable) DRAM configurations. Support for "Fast Page" mode and "Extended Data Out" (EDO) mode DRAM improves CPU performance by offering CPU access to the display memory at maximum bus bandwidth. A minimum one DRAM interface is achieved by using high bandwidth WRAM for increased system throughput and superior graphics operation.

Contact your local representative for:

- Technical Reference Manuals
- Evaluation Kits: Includes documentation plus evaluation board and software
- Reference Design Kits: Includes full documentation and software license for drivers to immediately enter production

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	§	
	§	
Robert M. Nally	§	
	§	Art Unit: 2609
Serial No.: 08/376,919	§	
	§	Examiner:
Filed: January 23, 1995	§	
	§	
For: APPARATUS, SYSTEMS AND METHODS FOR CONTROLLINGGRAPHICS AND VIDEO DATA IN MULTIMEDIA DATA PROCESSING AND DISPLAY SYSTEMS	§	

DECLARATION OF DAVID H. TANNENBAUM

I, David H. Tannenbaum, am a registered Patent attorney, registration number 24,745. I have prepared and prosecuted patent applications in the area of video processor technology for over six years.

1. I, along with James J. Murphy, registration number 34,503, have been retained as counsel to prepare and prosecute application serial number 08/376,919, titled APPARATUS, SYSTEMS AND METHODS FOR CONTROLLING GRAPHICS AND VIDEO DATA IN MULTIMEDIA DATA PROCESSING AND DISPLAY SYSTEMS. This application was filed in the U.S. Patent and Trademark Office on January 23, 1995.

2. A preliminary amendment was filed on April 4, 1995, adding additional claims.

3. I am very familiar with the prior art and I believe that all of the claims, including the claims contained in the Preliminary Amendment, are allowable in view of any prior art known by me. I have discussed in detail the scope of the claims of application Serial No. 08/376,919 with Robert Nally, an expert in the field to which the claims are directed, and he has informed me that it is his belief that all of the claims, including the claims contained in the Preliminary Amendment, are allowable in view of any prior art known by him.

4. I have read the facts contained in Mr. Nally's Declaration concerning the infringing devices and I agree with Mr. Nally's statements that in order for the competitor's devices to be pin and function compatible with the Cirrus Logic device it must then be the same as shown in Cirrus Logic's Specification attached as Exhibit A to the Declaration of Robert M. Nally.

5. I have reviewed the functional Specification of the Cirrus Logic competitor, attached as Exhibit B to the Declaration of Robert M. Nally, and compared that specification to the subject application and to the claims thereof, including the claims of the Preliminary Amendment.

6. It is my unquestionable opinion that the competitor's device, if designed in accordance with Exhibit B (the functional specification of the Cirrus Logic competitor) attached to Robert M. Nally's Declaration, would infringe one or more of the claims presently on file, or contained in the Preliminary Amendment, if those claims were to be held allowable.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

David H. Tannenbaum

Date: April 4, 1995

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CIRRUS LOGIC®

CL-GD7542 (Nordic)
LCD VGA Controller



NORDIC

PRELIMINARY DATA BOOK

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CL 28423

CL-GD7542 (Nordic) Version History

Revision 1.0.1 – May 19, 1994

Revision 1.0.2 – June 20, 1994

Revision 1.1 – August 26, 1994

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CL-GD7542

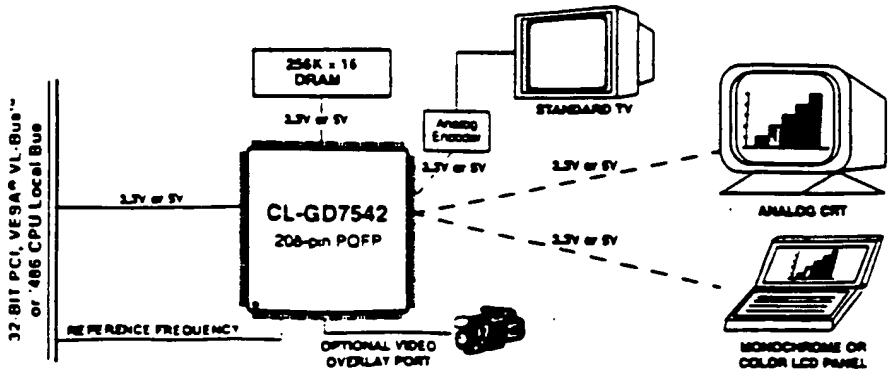
Preliminary Data Book

GUI-Accelerated SVGA LCD Controller with MVA™ Multimedia for Portable Computers

FEATURES

- **Single-chip Super VGA LCD controller**
  - Based upon industry-leading CL-GD542X desktop VGA
  - BIOS and drivers optimized from CL-GD542X code
  - IBM® VGA hardware-compatible
- **GUI acceleration**
  - BitBLT (bit block transfer) engine
  - Color expansion for 8- or 16-bit pixels
  - True packed-pixel addressing for 4-, 8-, and 16-bpp
  - Programmable linear memory addressing
  - 32 x 32 or 64 x 64 hardware cursor
- **Multimedia acceleration and enhancement**
  - MotionVideo™ Architecture (MVA™)
    - True-color, full-motion video playback
    - Multi-format frame buffer
    - Integrated YCrCb: RGB color space converter
    - 2x horizontal/vertical hardware zoom
  - 8-bit feature connector port or video overlay
  - Interface to analog encoders for NTSC/PAL-out
- **64 x 64 pixel size hardware pop-up icons**
  - Displays up to four independently controlled, 4-color icons
- **32-bit direct-connect CPU host bus interfaces**
  - '486 CPU local bus (up to 50 MHz @ 5V)
  - VESA® VL-Bus™
  - PCI system bus with burst support
    - Big-endian byte-order hardware support for PowerPC
- **Scalable 1- and 2-Mbyte display memory**
  - 32-bit-wide interface to display memory
  - Two or four 256K x 16 DRAMs, or four 512K x 8 DRAMs
- **Integrated programmable frequency synthesizer**
  - VCLK up to 85 MHz @ 5V; 65 MHz @ 3.3V
  - MCLK up to 50 MHz @ 5V; 45 MHz @ 3.3V
- **Integrated 24-bit true-color RAMDAC™**
  - 640 x 480 non-interlaced, 16M colors
  - 800 x 600 non-interlaced, 64K colors
  - 1024 x 768 non-interlaced, 256 colors
  - 1280 x 1024 interlaced, 256 colors
- **640 x 480 and 800 x 600 LCDs**
  - Dual-scan color and monochrome STN LCDs
  - Color-active matrix LCDs (9-, 12-, 18-, and 24-bit interfaces)
  - Active addressing LCDs
  - Dithering algorithm automatically adds up to 6 bits-per-primary color without decreasing spatial resolution
  - Enhanced frame-rate modulation algorithm improves display quality with fast-response STN LCDs (~100 ms)
  - SimulSCAN™ (simultaneous CRT and LCD)
- **Power-management capabilities**
  - 3.3V, 5.0V, and mixed-voltage operation
  - Hardware suspend input pin or software suspend option
    - Self-refresh DRAMs or DRAM refresh via 32-kHz clock
  - Internal timers for Standby mode and backlight control
  - LCD power sequencing
  - VESA® DPMS (Display Power Management Signaling)
  - DDC-1 (Display Data Channel) support
- **EIAJ Standard 208-pin plastic quad flat package**

Functional Block Diagram



CIRRUS LOGIC®

CL-GD7542

Super VGA LCD Controller

OVERVIEW

The CL-GD7542 GUI-accelerated SVGA LCD controller with MotionVideo™ provides the performance and integration required for the next generation of mid-range to premium portable computers. Features of the CL-GD7542 include BitBLT GUI acceleration, 800 x 600 LCD support, true-color capability, and mixed-voltage operation for low power consumption. A complete graphics subsystem can be built using only three active components: the CL-GD7542 and two DRAMs.

System manufacturers can further differentiate their portable products by taking advantage of the video multimedia enhancement and acceleration capabilities of the MotionVideo architecture, live-video overlay, and, with an external analog encoder, video output support offered for the following standards:

- NTSC (National Television System Committee)
- PAL (Phase-Alternation Line)

ADVANTAGES

Unique Features	Benefits
High Performance —	
■ BitBLT engine, color expansion, hardware cursor, linear addressing, and 32-bit memory interface	❒ Accelerates GUIs such as Microsoft® Windows™; provides high resolution and color-depth capabilities.
■ 32-bit local bus interfaces, operating up to 33 MHz, includes support for PCI with burst mode	❒ Increases system throughput; PCI interface allows use in X86, PowerPC™, or other platforms.
■ Hardware 'pop-up' icons	❒ Provides hot-key display for on-screen symbols such as battery fuel gauge, contrast/brightness controls, etc.
Multimedia —	
MVA (MotionVideo™ Architecture)	❒ Enhances video playback capabilities to support up to 30 fps with 24-bpp color quality.
■ Multi-format frame buffer and YCrCb-to-RGB color space conversion	❒ Displays separate graphics and video windows at independent color depths.
■ 2x hardware zoom for playback	❒ Enlarges video clips with little or no frame rate reduction.
■ 8-bit VAFC port	❒ Allows live 'TV in a window' capability.
■ Interface to NTSC/PAL analog encoders	❒ Integrated design can be developed to display computer-generated data on a TV or record to a VCR.
Enhanced LCD Support —	
■ 800 x 600 LCD support (both TFT and dual-scan STN) with comprehensive resolution-compensation support	❒ Supports latest LCD technology and enables full use of the display area whether in graphics or text mode.
■ Enhanced frame-rate modulation	❒ Improves display quality; reduces crosstalk, ghosting, and cursor 'submarining'.
■ Intelligent dithering algorithm expands the number of input bits per R, G, and B on TFT or STN LCDs	❒ Displays high- and true-color modes with smooth shading (no contouring) on all supported LCD types.
Power Management —	
■ 3.3V, 5.0V, or mixed-voltage support	❒ Minimizes operating power consumption; provides manufacturing flexibility.
■ Hardware-initiated Standby and Suspend modes and VESA® DPMS support for CRTs	❒ Reduces power consumption; supports Energy Star monitors for 'green PC' compliance.
Design Flexibility —	
■ VGA controller with integrated RAMDAC, dual-frequency clock synthesizer in a 208-pin PQFP	❒ Minimizes chip count and board space required for the display subsystem.
■ Big-endian byte ordering in display memory with PCI host interface	❒ Supports X86 designs with little-endian data; supports PowerPC™ designs with big-endian data.
Software —	
■ Drivers supplied for 3D-graphics libraries and emerging APIs (advanced programming interface) for games	❒ Supports emerging standards for Windows-based 3D applications.

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Software Support

Operating System and Application Software Drivers

Software Drivers[a]	Resolution Supported	Number of Colors
Microsoft®/Intel® DCI v1.4	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768 640 x 480, 800 x 600 640 x 480	256 colors 16 and 256 colors 65,536 colors 16.8 million colors
Microsoft® Windows™ v3.1	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768 640 x 480, 800 x 600 640 x 480	256 colors 16 and 256 colors 65,536 colors 16.8 million colors
Microsoft® Windows NT™ v3.1 (currently for 'X86; future for PowerPC™)	640 x 480, 800 x 600, 1024 x 768	16 and 256 colors
OS/2™ v2.0, v2.1	640 x 480, 800 x 600, 1024 x 768 640 x 480, 800 x 600 640 x 480	16 and 256 colors 65,536 colors 16.8 million colors
AutoCAD® v11, v12	640 x 480, 800 x 600, 1024 x 768 640 x 480, 800 x 600 640 x 480	16 and 256 colors 65,536 colors 16.8 million colors
Autoshade® v2.0 3D Studio® v1, v2	640 x 480, 800 x 600, 1024 x 768 640 x 480, 800 x 600 640 x 480	256 colors 65,536 colors 16.8 million colors

[a] Driver support for additional applications is provided by independent software vendors, either with specific drivers or through VESA mode support. In many instances, existing drivers for the CL-GD542X can be used with the CL-GD7542. For more information concerning driver support, contact the software manufacturer.

BIOS

Feature	Benefit
■ Available as 48-Kbyte BIOS to provide optimum performance with VGA and VESA® extended mode support, or as a 32-Kbyte subset with a 16-Kbyte relocatable module or loaded as TSRs (terminate and stay resident)	❒ Provides system design options for the best combination of performance and functionality.
■ Fully IBM® VGA-compatible BIOS	❒ Ensures compatibility with the existing base of PC applications.
■ VESA® VBE (video BIOS extensions) 1.2 and PM (power management) support	❒ Compatible with industry standard for extended mode support beyond VGA and power-management control.

Software Utilities

Utility	Function
CLPanel	LCD parameter optimization utility for OEM development use
OEMSI	BIOS-customization utility for OEM development use
PCLRegs	VGA controller register viewer/editor for OEM development use
Switcher	Video configuration TSR (terminate and stay resident)
CLMode	Video mode and video display configuration utility suitable for end-use distribution (includes foreign language translations)
WinMode	Windows™ application for graphic mode and display type configuration (includes foreign language translations, selectable from within the utility)
AutoResolution Switching	Windows™ application for automatically switching display resolutions (for example, from a 1024 x 768 CRT to lower-resolutions 640 x 480 or 800 x 600 LCDs) without relaunching Windows™

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1. Pin Definitions and Block Diagrams

1.1 Pin Definitions

1.1.1 Pin-Out Diagram

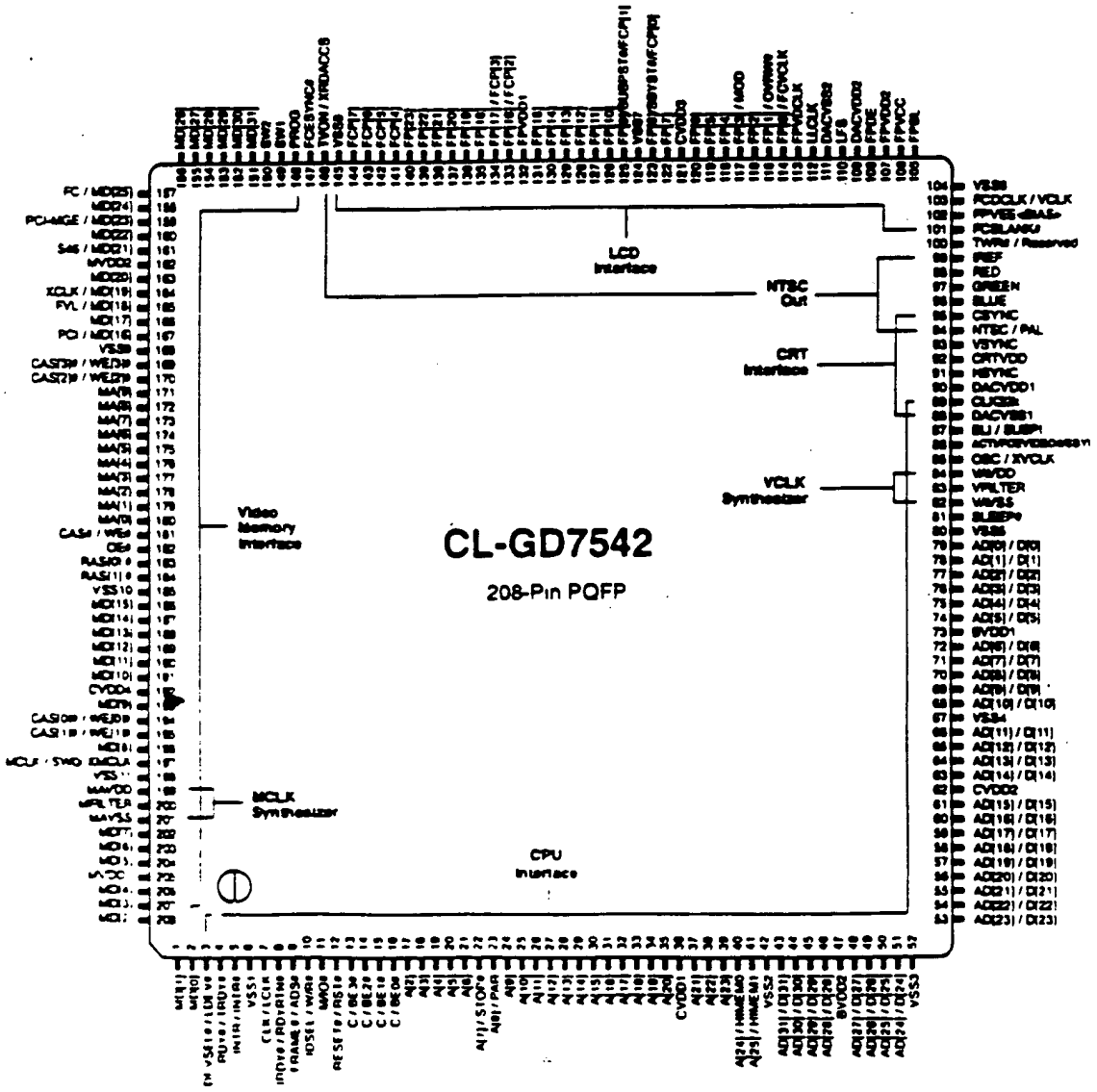


Figure 1–1. Pin-Out Diagram

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1.1.2 Pin Table

Table 1–1. Pins, by Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	MD[1]	37	A [21]	73	BVDD1
2	MD[0]	38	A [22]	74	D [5]
3	DEVSEL# / LDEV#	39	A [23]	75	D [4]
4	TRDY# / RDY#	40	HIMEM0	76	D [3]
5	INTR / INTR#	41	HIMEM1	77	D [2]
6	VSS1	42	VSS2	78	D [1]
7	CLK / LCLK	43	D [31]	79	D [0]
8	IRDY# / RDYRTN#	44	D [30]	80	VSS5
9	FRAME# / ADS#	45	D [29]	81	SLEEP# / EBROM#
10	IDSEL# / W/R#	46	D [28]	82	VAVSS
11	M/IO#	47	BVDD2	83	VFILTER
12	RESET#	48	D [27]	84	VAVDD
13	C / BE3#	49	D [26]	85	OSC
14	C / BE2#	50	D [25]	86	SBY1 / ACT1 / FCEVIDEO#
15	C / BE1#	51	D [24]	87	SUSP1 / BL1
16	C / BE0#	52	VSS3	88	DACVSS1
17	A [2]	53	D [23]	89	CLK32K
18	A [3]	54	D [22]	90	DACVDD1
19	A [4]	55	D [21]	91	HSYNC
20	A [5]	56	D [20]	92	CRTVDD
21	A [6]	57	D [19]	93	VSYNC
22	A [7] / STOP#	58	D [18]	94	NTSC / PAL
23	A [8] / PAR	59	D [17]	95	CSYNC
24	A [9]	60	D [16]	96	BLUE
25	A [10]	61	D [15]	97	GREEN
26	A [11]	62	CVDD2	98	RED
27	A [12]	63	D [14]	99	IREF
28	A [13]	64	D [13]	100	Reserved
29	A [14]	65	D [12]	101	FCBLANK#
30	A [15]	66	D [11]	102	FPVEE
31	A [16]	67	VSS4	103	VCLK / FCDCLK
32	A [17]	68	D [10]	104	VSS6
33	A [18]	69	D [9]	105	FPBL
34	A [19]	70	D [8]	106	FPVCC
35	A [20]	71	D [7]	107	FPVDD2
36	CVDD1	72	D [6]	108	FPDE

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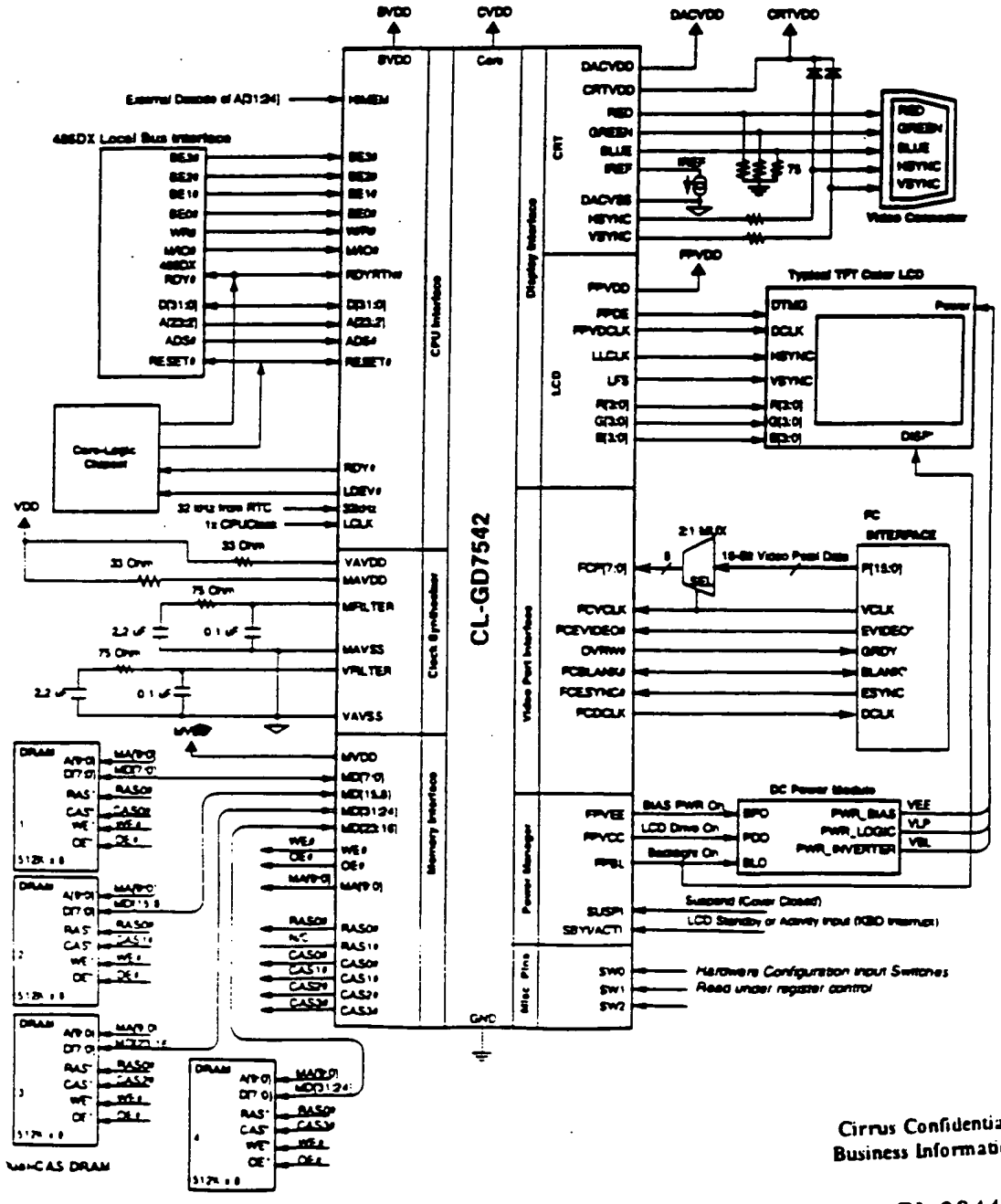
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Table 1-1. Pins, by Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
109	DACVDD2	143	FCP [6]	177	MA[3]
110	LFS	144	FCP [7]	178	MA[2]
111	DACVSS2	145	VSS8	179	MA[1]
112	LLCLK	146	TVON / XRDACCS	180	MA[0]
113	FPVDCLK	147	FCESYNC#	181	CAS# / WE#
114	FP [0] / FCVCLK	148	PROG	182	OE#
115	FP [1] / OVRW#	149	SW1	183	RAS[0]
116	FP [2]	150	SW2	184	RAS[1]
117	FP [3] / MOD	151	MD[31]	185	VSS10
118	FP [4]	152	MD[30]	186	MD[15]
119	FP [5]	153	MD[29]	187	MD[14]
120	FP [6]	154	MD[28]	188	MD[13]
121	CVDD3	155	MD[27]	189	MD[12]
122	FP [7]	156	MD[26]	190	MD[11]
123	FP [8] / SBYST# / FCP[0]	157	MD[25] / VAFC	191	MD[10]
124	VSS7	158	MD[24]	192	CVDD4
125	FP [9] / SUSPST# / FCP[1]	159	MD[23] / PCI-MGE	193	MD[9]
126	FP [10]	160	MD[22]	194	WE[0]# / CAS[0]#
127	FP [11]	161	MD[21] / S46	195	WE[1]# / CAS[1]#
128	FP [12]	162	MVDD2	196	MD[8]
129	FP [13]	163	MD[20]	197	SW0
130	FP [14]	164	MD[19]	198	VSS11
131	FP [15]	165	MD[18] / FVL	199	MAVDD
132	FPVDD1	166	MD[17]	200	MFILTER
133	FP [16]	167	MD[16] / PCI	201	MAVSS
134	FP [17]	168	VSS9	202	MD[7]
135	FP [18]	169	WE[3]# / CAS[3]#	203	MD[6]
136	FP [19]	170	WE[2]# / CAS[2]#	204	MD[5]
137	FP [20]	171	MA[9]	205	MVDD1
138	FP [21]	172	MA[8]	206	MD[4]
139	FP [22]	173	MA[7]	207	MD[3]
140	FP [23]	174	MA[6]	208	MD[2]
141	FCP [4]	175	MA[5]		
142	FCP [5]	176	MA[4]		

1.2 Block Diagrams: LCD Interfaces to CL-GD7542

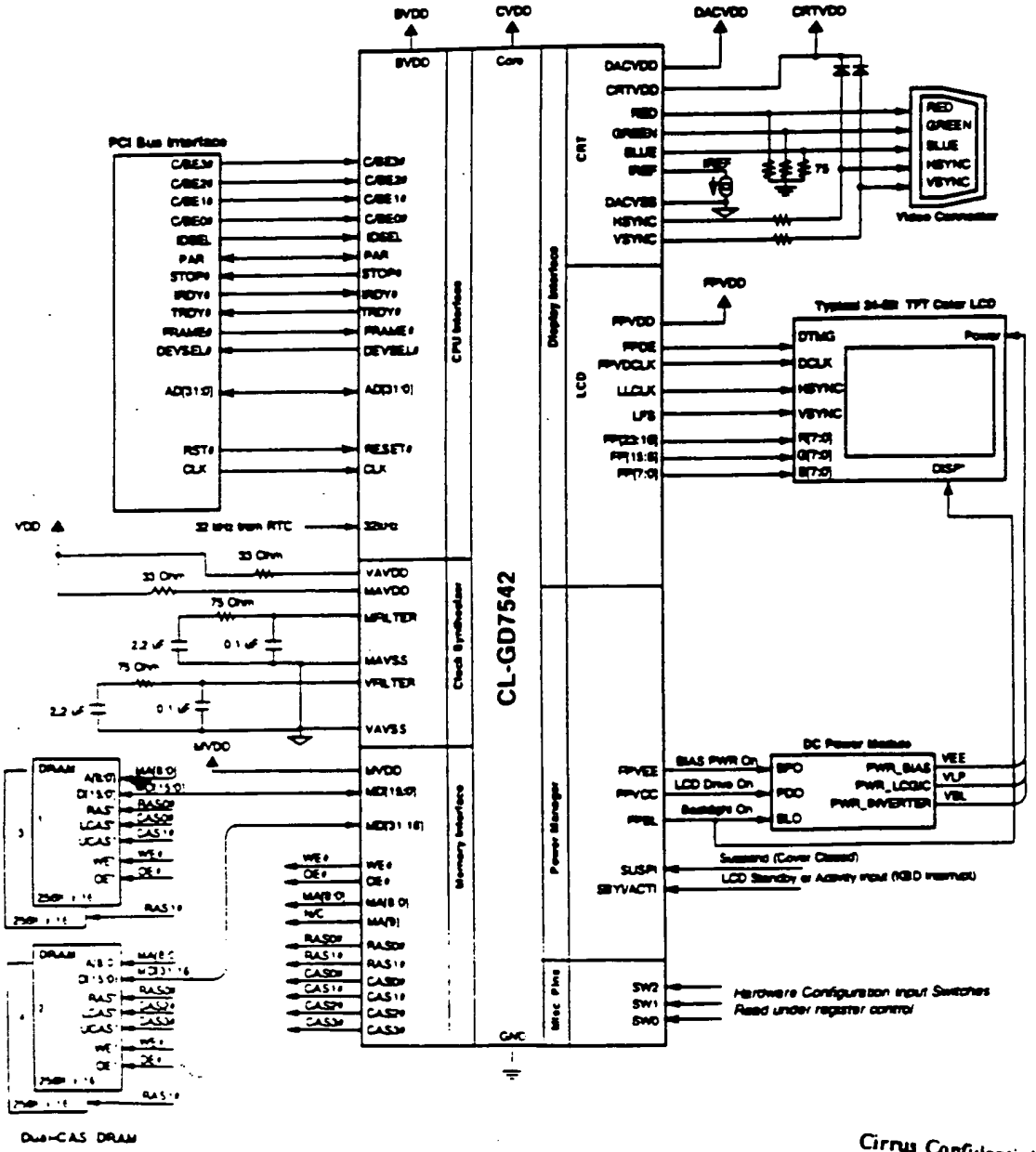
1.2.1 TFT (512-Color) to 486DX or VESA 32-Bit Local Bus, 2-Mbyte 512K x 8 DRAM, Video Port



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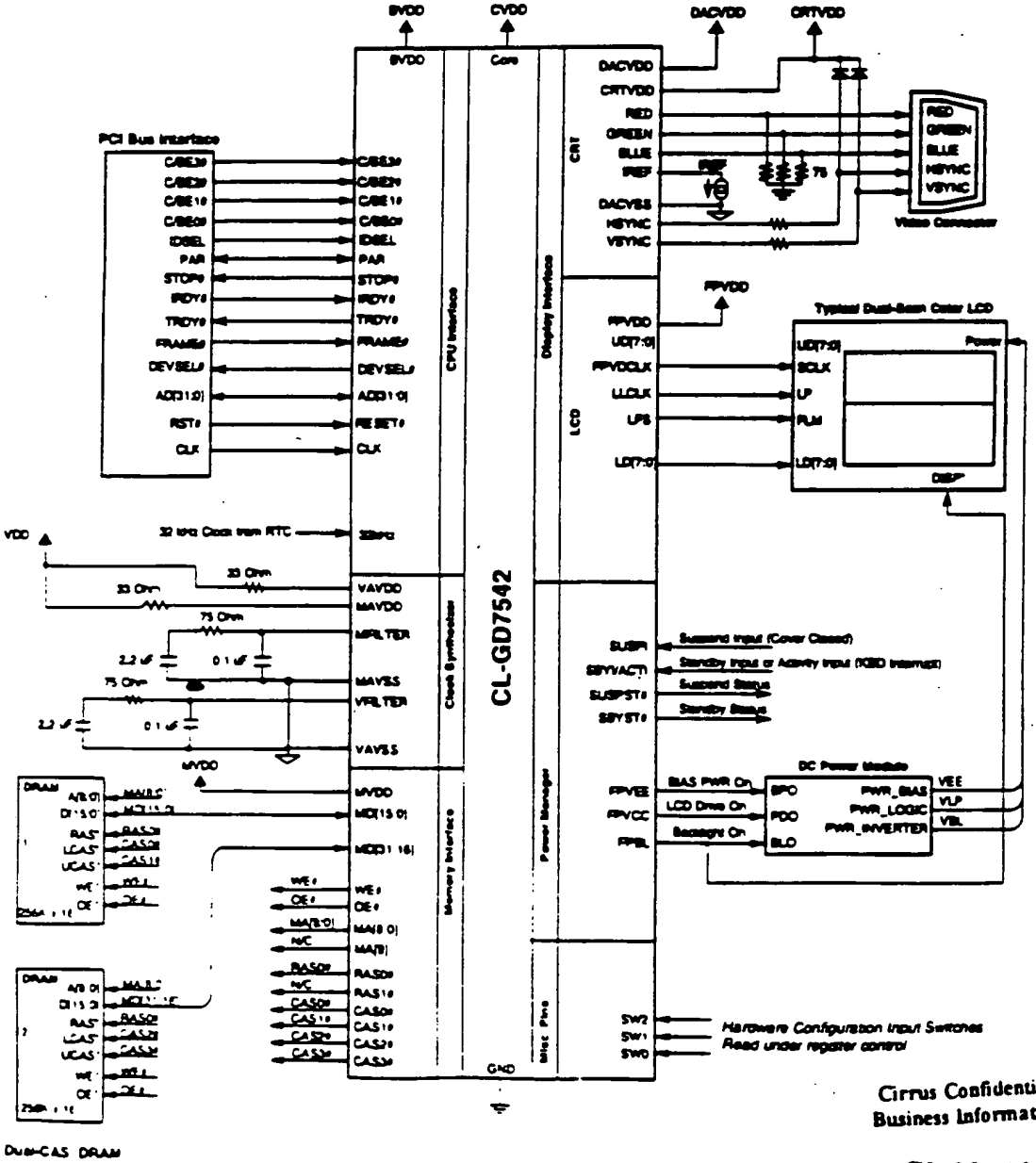
1.2.2 TFT (24-Bit Color) to PCI Bus, 2-Mbyte 256K x 16 DRAM.



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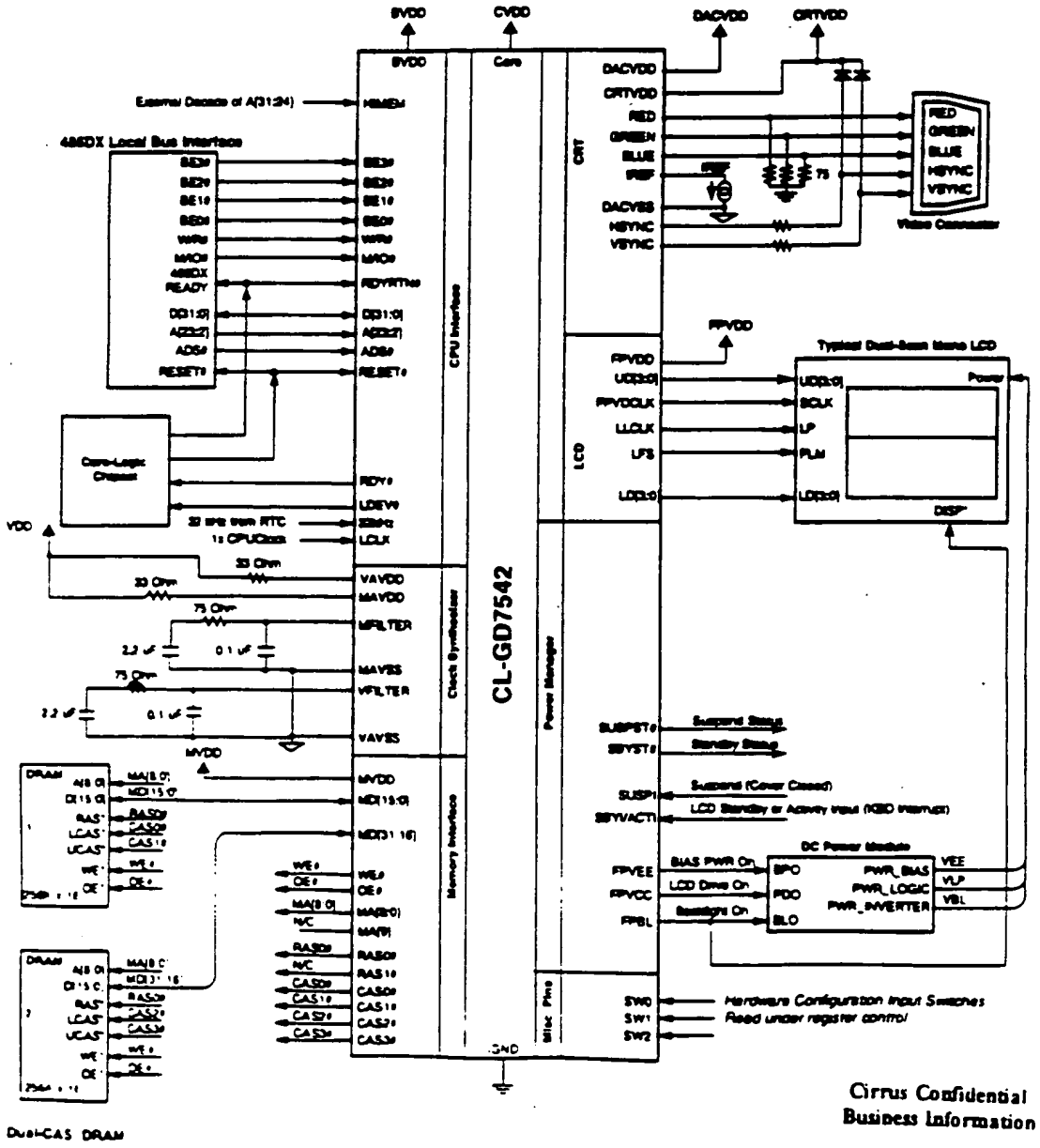
1.2.3 Dual-Scan Color (16-Bit) to PCI Bus, 1-Mbyte 256K x 16 DRAM.



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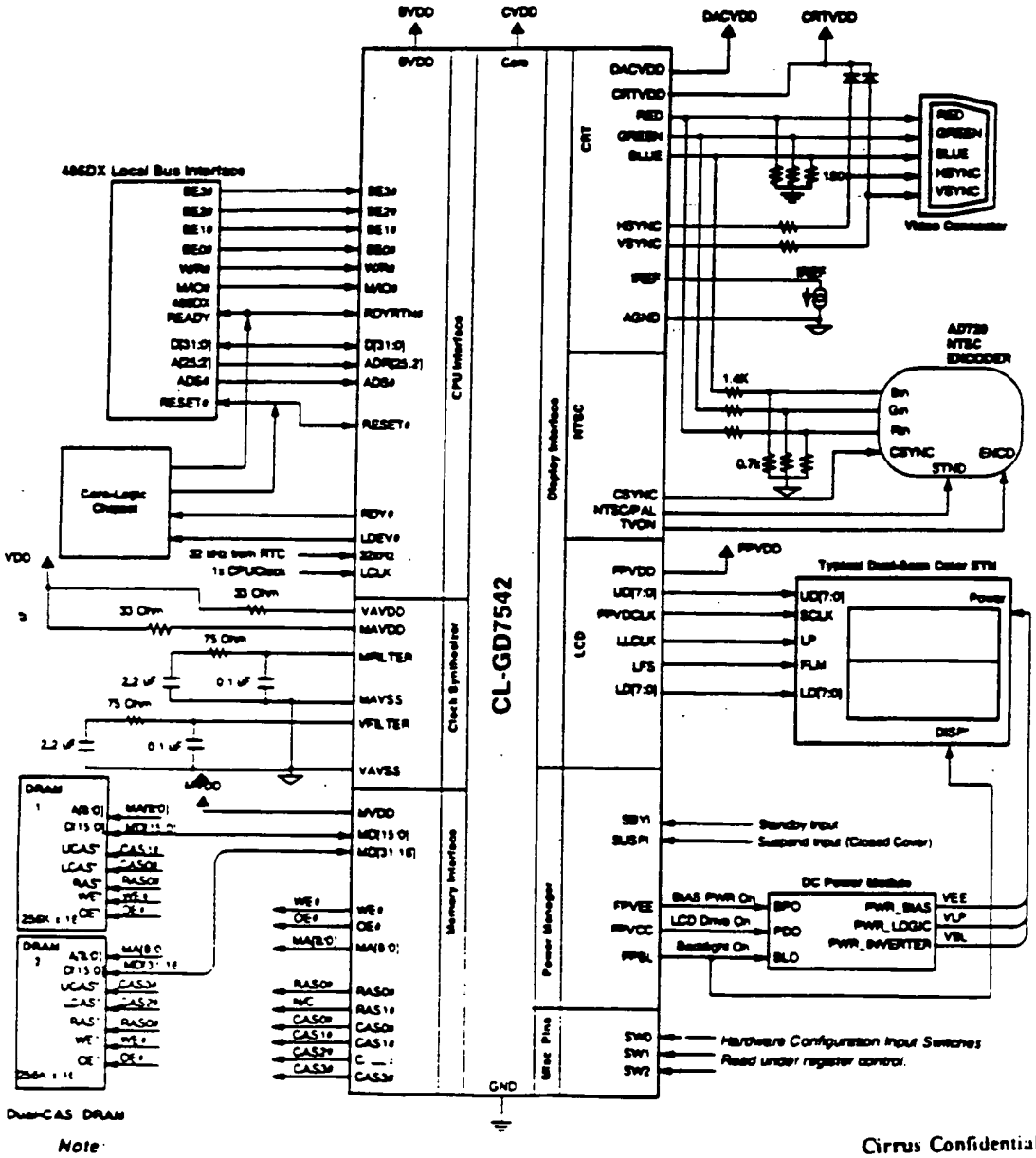
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1.2.4 Dual-Scan Mono (8-Bit) to 486DX or VESA 32-Bit Local Bus, 1-Mbyte 256K x 16 DRAM



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1.2.5 Dual-Scan Color (16-Bit) to 486DX or VESA 32-Bit Local Bus, 1-Mbyte 256K x 16 DRAM, NTSC Output

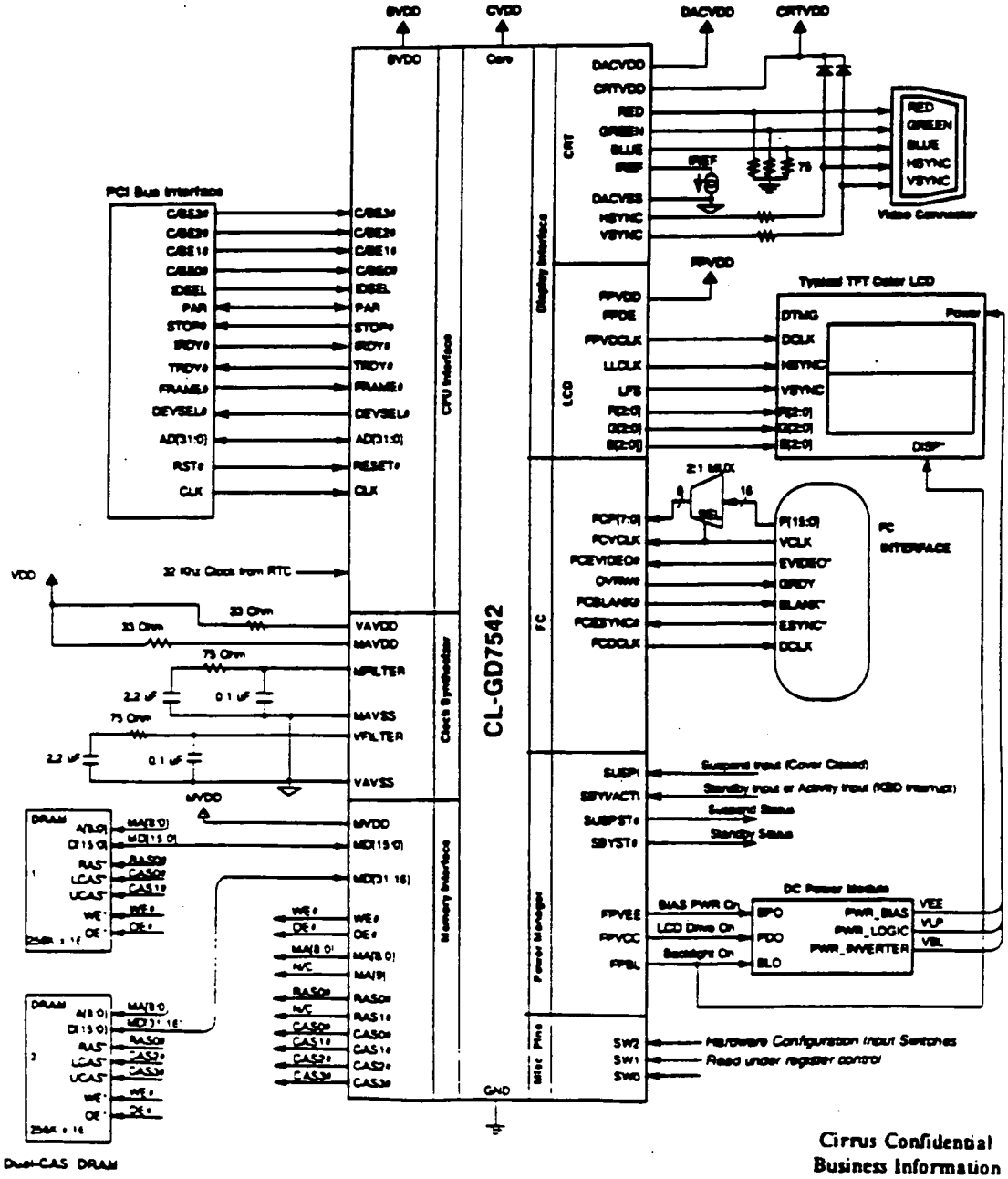


Note:
In this diagram the CRT must be disconnected when using the NTSC output.

This diagram illustrates general signal connections. All information is preliminary and subject to change. For detailed design examples, refer to the CL-GD7542 Application Handbook.

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1.2.6 TFT (9-Bit Color) to PCI Bus, 1-Mbyte 256K x 16 DRAM, FC Interface



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2. Detailed Pin Descriptions

The following abbreviations are used for pin types in the following sections:

- (I) indicates Input
- (O) indicates Output
- (I/O) indicates a bidirectional function
- (I or 0) indicates either an Input or Output function, depending on the mode
- (OC) indicates Open-Collector Output
- (3-S) indicates 3-State Output
- (#) indicates active-low function

2.1 Host Interface Pins — VESA Local Bus and PCI Bus Pin Identification

As explained in this section, a number of bus interface pins are defined according to the local bus type to which the CL-GD7542 is connected.

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2.1.1 Host Interface – '486 or VESA Local Bus Pins

Pin Name	Pin No.	Type	Local Bus Name/Description
A[23:2]	39:37 35:17	I	**ADDRESS [23:2]:** These inputs are used to select the resource to be accessed during memory or I/O operations.
BE[3:0]#	13:16	I	**BYTE ENABLE[3:0]#:** These active-low inputs are connected directly to the corresponding CPU byte-enable output.
D[31:0]	43:46,48:51 53:61,63,66 68:72,74:79	I/O	**DATA [31:0]:** These bidirectional pins are used to transfer data during any memory or I/O operation. For the VESA Local Bus or '486 32-bit Local Bus, these pins are connected directly to D[31:0].
HIMEM[0:1] A[24:25]	40,41	I	**HIGH MEMORY [1:0]:** These active-high inputs are a decode of the upper CPU Address bits. Normally, these inputs are used as A[24:25]. However, they can be used as A[31:30] and leave 2 GBytes of upper address space for MPEG (Moving Picture Experts Group) and JPEG (Joint Picture Expert Group) boards.
INTR	5	3-S	**INTERRUPT REQUEST:** This active-high output indicates that the CL-GD7542 has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. For a description of controls for this pin, refer to Register CR11[3:0].
ADS#	9	I	**ADDRESS DATA STROBE#:** This active-low input indicates that a new cycle has begun. The ADS# signal is generated from a decode of the CPU output signals, A[23:2] and M/IO#. This output will be low before the middle of the first timing (T2) cycle after ADS# goes low. This pin must be connected directly to the ADS# pin on the local bus.
LCLK	7	I	**LOCAL CLOCK:** This active-low input is the timing reference when the CL-GD7542 is connected to a '486 Local Bus. For the VESA Local Bus, this pin is connected to LCLK. For the '486 Local Bus, this pin is connected to CLK1X. If no CLK1X is available from the '486, CLK2 must be divided by two and tied to the CL-GD7542 LCLK pin, and clock skew must be less than 2.0 ns.
LDEV#	3	OC	**LOCAL BUS DEVICE#:** This open-collector output is driven low to indicate that the CL-GD7542 will respond to the current cycle. This pin is connected to LDEV#.

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2.1.1 Host Interface — '486 or VESA Local Bus Pins *(cont.)*

Pin Name	Pin No.	Type	Local Bus Name/Description
M/IO#	11	I	**MEMORY I/O#** This input indicates whether a memory or I/O operation is to occur. It must be connected directly to the M/IO# pin on the CPU. When M/IO# is high, a memory operation is selected. When M/IO is low, an I/O operation is selected.
RDY#	4	3-S	**READY#:** This active-low signal is used as an output to terminate a CL-GD7542 bus cycle. For VESA Local Bus, this pin is connected to the LRDY# pin. For the '486 Local Bus, this pin is connected to the RDY# pin.
RDYRTN#	8	I	**READY RETURN#:** This input establishes a handshake between the CL-GD7542 and VESA Local Bus so that the CL-GD7542 is informed when the cycle has ended. RDYRTN# typically goes low in the same LCLK cycle that LRDY# goes low. When LCLK is higher than 33 MHz, RDYRTN# may trail LRDY# by one LCLK cycle. During DMA or system I/O bus master operations, RDYRTN# goes low for one LCLK cycle when the DMA or system I/O bus masters command ends. For the VESA Local Bus, this pin is connected to RDYRTN#. For the '486 Local Bus, this pin is connected to RDY#.
RESET#	12	I	**RESET#:** This input, when low, initializes the CL-GD7542 to a known state. The trailing (rising) edge of this input loads the Configuration registers SR22[7:0] and SR24[7] with the data on MD[25:16] pins. The data on the MD[25:16] pins is determined either by internal pull-down resistors or optional external pull-up resistors. When RESET# is low, it forces all outputs to a high-impedance state, and it initializes all registers to their Reset state.
SLEEP#	81	I	**SLEEP#:** This active-low input is used by the external hardware to put the CL-GD7542 into bus Sleep mode. When this input is low, the memory and I/O interface is disabled, and the displays are turned off. Once this pin is low, no other chip access is possible until this pin goes high.
W/R#	10	I	**WRITE/READ#:** This input indicates whether a write or read operation is selected by the CPU. It must be connected directly to the W/R# pin on the CPU. When W/R# is high, a write will occur. When W/R# is low, a read will occur.

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2.1.2 Host Interface – PCI Bus Pins

Pin Name	Pin No.	Type	Local Bus Name/Description
AD[31:0]	43:46, 48:51, 53:61, 63:66 68:72,74:79	I/O	**ADDRESS AND DATA [31:0]:** These multiplexed, bidirectional pins are used to transfer system address and data during any memory or I/O operation on the PCI Bus. During the first clock of a transaction, these pins contain a 32-bit physical byte address. During subsequent clocks, they contain data. These pins directly connect to AD[31:0] of the PCI Bus.
C/BE#[3:0]	13:16	I or O	**COMMAND AND BYTE ENABLE#[3:0]:** These multiplexed pins are used to transfer Bus Command and Byte Enables during any memory or I/O operation on the PCI Bus. During the address phase of the operation, these pins define the bus command. (Refer to Table 2–1.) During the data phase, these pins are used as Byte Enable Outputs. C/BE#0 applies to Byte 0. C/BE#3 applies to Byte 3. These pins directly connect to C/BE#[3:0] of the PCI Bus.

Table 2–1. Command and Byte Enable#

C/BE#				Command Type	Comments
[3]	[2]	[1]	[0]		
0	0	0	0	Interrupt Acknowledge	–
0	0	0	1	Special Cycle	–
0	0	1	0	I/O Read	Valid
0	0	1	1	I/O Write	Valid
0	1	0	0	Reserved	–
0	1	0	1	Reserved	–
0	1	1	0	Memory Read	Valid
0	1	1	1	Memory Write	Valid
1	0	0	0	Reserved	–
1	0	0	1	Reserved	–
1	0	1	0	Configuration Read	Valid
1	0	1	1	Configuration Write	Valid
1	1	0	0	Memory Read Multiple	–
1	1	0	1	Dual Address Cycle	–
1	1	1	0	Memory Read Line	–
1	1	1	1	Memory Write and Invalidate	–

2.1.2 Host Interface – PCI Bus Pins *(cont.)*

Pin Name	Pin No.	Type	Local Bus Name/Description
CLK	7	I	**CLOCK:** This is the timing reference for the CL-GD7542, when it is connected to a PCI Bus. This pin must be connected directly to the PCI Bus CLK pin.
DEVSEL#	3	OC	**DEVICE SELECT#:** This open-collector output is driven low to indicate that the CL-GD7542 will respond to the current cycle.
FRAME#	9	I	**FRAME#:** This active-low input indicates the beginning and duration of an access. FRAME# goes low to indicate the beginning of a bus transaction. While FRAME# is low, data transfers continue. The transaction is in its final data phase when FRAME# goes high.
IDSEL	10	I	**INITIALIZATION DEVICE SELECT#:** This active-high input signal is used as a chip select in lieu of the upper 24 address lines during configuration read and write cycles.
INTR#	5	3-S	**INTERRUPT REQUEST#:** This active-low output indicates that the CL-GD7542 has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. It is controlled by register CR11[3:0].
IRDY#	8	I	**INITIATOR READY#:** This active-low input establishes a handshake between the CL-GD7542 and PCI Bus, so that the CL-GD7542 knows when the cycle has ended. Wait states are inserted until both IRDY# and TRDY# are low.
PAR	23	3-S	**PARITY:** This signal provides even parity across AD[31:0] and C/BE#[3:0]. The CL-GD7542 samples this signal during write cycles, and transmits the correct parity for read cycles.
RST#	12	I	**RST#:** This input, when low, initializes the CL-GD7542 to a known state. The trailing (rising) edge of this input loads the Configuration registers SR22[7:0] and SR24[7] with the data on MD[25:16], which is determined either by internal pull-down resistors or optional external pull-up resistors.
STOP#	22	3-S	**STOP#:** This active-low output indicates a current request to the PCI Bus Master to stop the current transaction.
TRDY#	4	3-S	**TARGET READY#:** This active-low signal is used as an output to terminate a CL-GD7542 bus cycle.

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2.2 Flat Panel LCD Interface Pins

The flat panel LCD interface is determined by the type of LCD flat panel used. Refer to the Cirrus Logic **CL-GD7542 Panel Interface Connection Table** in the *CL-GD7542 Applications Book* for specific connection information. Also, see Table 1-3 for LCD-vs-Pin cross-reference.

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[0]	114	O	B0	**24-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data Bit 0 (LSB) for 24-bit TFT color LCDs.
FP[1]	115	O	B1	**24-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data Bit 1 for 24-bit TFT color LCDs.
FP[2]	116	O	B2	**24-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data Bit 2 for 24-bit TFT color LCDs.
			B0	**18-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data Bit 0 (LSB) for 18-bit TFT color LCDs.
FP[3]	117	O	B3	**24-BIT TFT BLUE BIT [3]:** This bit is BLUE Color Data Bit 3 for 24-bit TFT color LCDs.
			B1	**18-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data Bit 1 for 18-bit TFT color LCDs.
FP[4]	118	O	B4	**24-BIT TFT BLUE BIT [4]:** This bit is BLUE Color Data Bit 4 for 24-bit TFT color LCDs.
			B2	**18-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data Bit 2 for 18-bit TFT color LCDs.
			B0	**12-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data Bit 0 (LSB) for 12-bit TFT color LCDs.
			SLD0	**16-BIT STN COLOR LOWER BIT [0]:** This bit is Lower Data Bit 0 (LSB) for 16-bit dual-scan and single-scan STN color LCDs.
			SLD0	**8-BIT STN COLOR LOWER BIT [0]:** This bit is Lower Data Bit 0 (LSB) for 8-bit dual-scan and single-scan STN color LCDs.
			LD0	**LOWER DATA [0]:** This bit is Lower Panel Data Bit 0 (LSB) for dual-scan STN monochrome LCDs.

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[5]	119	O	B5	**24-BIT TFT BLUE BIT [5]:** This bit is BLUE Color Data Bit 5 for 24-bit TFT color LCDs.
			B3	**18-BIT TFT BLUE BIT [3]:** This bit is BLUE Color Data Bit 3 for 18-bit TFT color LCDs.
			B1	**12-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data Bit 1 for 12-bit TFT color LCDs.
			B0	**9-BIT TFT BLUE BIT [0]:** This bit is BLUE Color Data Bit 0 (LSB) for 9-bit TFT color LCDs.
			SLD1	**16-BIT STN COLOR LOWER BIT [1]:** This bit is Lower Data Bit 1 for 16-bit dual-scan and single-scan STN color LCDs.
			SLD1	**8-BIT STN COLOR LOWER BIT [1]:** This bit is Lower Data Bit 1 for 8-bit dual-scan and single-scan STN color LCDs.
			LD1	**LOWER DATA [1]:** This bit is Lower Panel Data Bit 1 for dual-scan STN monochrome LCDs.
FP[6]	120	O	B6	**24-BIT TFT BLUE BIT [6]:** This bit is BLUE Color Data Bit 6 for 24-bit TFT color LCDs.
			B4	**18-BIT TFT BLUE BIT [4]:** This bit is BLUE Color Data Bit 4 for 18-bit TFT color LCDs.
			B2	**12-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data Bit 2 for 12-bit TFT color LCDs.
			B1	**9-BIT TFT BLUE BIT [1]:** This bit is BLUE Color Data Bit 1 for 9-bit TFT color LCDs.
			SLD2	**16-BIT STN COLOR LOWER BIT [2]:** This bit is Lower Data Bit 2 for 16-bit dual-scan and single-scan STN color LCDs.
			SLD2	**8-BIT STN COLOR LOWER BIT [2]:** This bit is Lower Data Bit 2 for 8-bit dual-scan and single-scan STN color LCDs.
			LD2	**LOWER DATA [2]:** This bit is Lower Panel Data Bit 2 for dual-scan STN monochrome LCDs.

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[7]	122	O	B7	**24-BIT TFT BLUE BIT [6]:** This bit is BLUE Color Data Bit 7 (MSB) for 24-bit TFT color LCDs.
			B5	**18-BIT TFT BLUE BIT [4]:** This bit is BLUE Color Data Bit 5 (MSB) for 18-bit TFT color LCDs.
			B3	**12-BIT TFT BLUE BIT [3]:** This bit is BLUE Color Data Bit 3 (MSB) for 12-bit TFT color LCDs.
			B2	**9-BIT TFT BLUE BIT [2]:** This bit is BLUE Color Data Bit 2 (MSB) for 9-bit TFT color LCDs.
			SLD3	**16-BIT STN COLOR LOWER BIT [3]:** This bit is Lower Data Bit 3 for 16-bit dual-scan and single-scan STN color LCDs.
			SLD3	**8-BIT STN COLOR LOWER BIT [3]:** This bit is Lower Data Bit 3 (MSB) for 8-bit dual-scan and single-scan STN color LCDs.
			LD3	**LOWER DATA [3]:** This bit is Lower Panel Data Bit 3 (MSB) for dual-scan STN monochrome LCDs.
FP[8]	123	O	G0	**24-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data Bit 0 (LSB) for 24-bit TFT color LCDs.
FP[9]	125	O	G1	**24-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data Bit 1 for 24-bit TFT color LCDs.
FP[10]	126	O	G2	**24-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data Bit 2 for 24-bit TFT color LCDs.
			G0	**18-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data Bit 0 (LSB) for 18-bit TFT color LCDs.
			SUD4	**16-BIT STN Color Upper Bit [4]:** This bit is Upper Data Bit 4 for 16-bit dual-scan and single-scan STN color LCDs.
FP[11]	127	O	G3	**24-BIT TFT GREEN BIT [3]:** This bit is GREEN Color Data Bit 3 for 24-bit TFT color LCDs.
			G1	**18-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data Bit 1 for 18-bit TFT color LCDs.
			SUD5	**16-BIT STN Color Upper Bit [5]:** This bit is Upper Data Bit 5 for 16-bit dual-scan and single-scan STN color LCDs.

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[12]	128	O	G4	**24-BIT TFT GREEN BIT [4]:** This bit is GREEN Color Data Bit 4 for 24-bit TFT color LCDs.
			G2	**18-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data Bit 2 for 18-bit TFT color LCDs.
			G0	**12-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data Bit 0 (LSB) for 12-bit TFT color LCDs.
			SLD4	**16-BIT STN COLOR LOWER BIT [0]:** This bit is Lower Data Bit 4 for 16-bit dual-scan and single-scan STN color LCDs.
			SUD0	**8-BIT STN COLOR UPPER BIT [0]:** This bit is Upper Data Bit 0 (LSB) for 8-bit dual-scan and single-scan STN color LCDs.
			UD0	**UPPER DATA [0]:** This bit is Upper Panel Data Bit 0 (LSB) for dual-scan STN monochrome LCDs.
FP[13]	129	O	G5	**24-BIT TFT GREEN BIT [5]:** This bit is GREEN Color Data Bit 5 for 24-bit TFT color LCDs.
			G3	**18-BIT TFT GREEN BIT [3]:** This bit is GREEN Color Data Bit 3 for 18-bit TFT color LCDs.
			G1	**12-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data Bit 1 for 12-bit TFT color LCDs.
			G0	**9-BIT TFT GREEN BIT [0]:** This bit is GREEN Color Data Bit 0 (LSB) for 9-bit TFT color LCDs.
			SLD5	**16-BIT STN COLOR LOWER BIT [5]:** This bit is Lower Data Bit 5 for 16-bit dual-scan and single-scan STN color LCDs.
			SUD1	**8-BIT STN COLOR UPPER BIT [1]:** This bit is Upper Data Bit 1 for 8-bit dual-scan and single-scan STN color LCDs.
			UD1	**UPPER DATA [1]:** This bit is Upper Panel Data Bit 1 for dual-scan STN monochrome LCDs

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[14]	130	O	G6	**24-BIT TFT GREEN BIT [6]:** This bit is GREEN Color Data Bit 6 for 24-bit TFT color LCDs.
			G4	**18-BIT TFT GREEN BIT [4]:** This bit is GREEN Color Data Bit 4 for 18-bit TFT color LCDs.
			G2	**12-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data Bit 2 for 12-bit TFT color LCDs.
			G1	**9-BIT TFT GREEN BIT [1]:** This bit is GREEN Color Data Bit 1 for 9-bit TFT color LCDs.
			SLD6	**16-BIT STN COLOR LOWER BIT [6]:** This bit is Lower Data Bit 6 for 16-bit dual-scan and single-scan STN color LCDs.
			SUD2	**8-BIT STN COLOR UPPER BIT [2]:** This bit is Upper Data Bit 2 for 8-bit dual-scan and single-scan STN color LCDs.
			UD2	**UPPER DATA [2]:** This bit is Upper Panel Data Bit 2 for dual-scan STN monochrome LCDs.
FP[15]	131	O	G7	**24-BIT TFT GREEN BIT [6]:** This bit is GREEN Color Data Bit 7 (MSB) for 24-bit TFT color LCDs.
			G5	**18-BIT TFT GREEN BIT [4]:** This bit is GREEN Color Data Bit 5 (MSB) for 18-bit TFT color LCDs.
			G3	**12-BIT TFT GREEN BIT [3]:** This bit is GREEN Color Data Bit 3 (MSB) for 12-bit TFT color LCDs.
			G2	**9-BIT TFT GREEN BIT [2]:** This bit is GREEN Color Data Bit 2 (MSB) for 9-bit TFT color LCDs.
			SLD7	**16-BIT STN COLOR LOWER BIT [7]:** This bit is Lower Data Bit 7 (MSB) for 16-bit dual-scan and single-scan STN color LCDs.
			SUD3	**8-BIT STN COLOR UPPER BIT [3]:** This bit is Upper Data Bit 3 (MSB) for 8-bit dual-scan and single-scan STN color LCDs.
			UD3	**UPPER DATA [3]:** This bit is Upper Panel Data Bit 3 (MSB) for dual-scan STN monochrome LCDs.
FP[16]	133	O	R0	**24-BIT TFT RED BIT [0]:** This bit is RED Color Data Bit 0 (LSB) for 24-bit TFT color LCDs.
FP[17]	134	O	R1	**24-BIT TFT RED BIT [1]:** This bit is RED Color Data Bit 1 for 24-bit TFT color LCDs.
FP[18]	135	O	R2	**24-BIT TFT RED BIT [2]:** This bit is RED Color Data Bit 2 for 24-bit TFT color LCDs.
			R0	**18-BIT TFT RED BIT [0]:** This bit is RED Color Data Bit 0 (LSB) for 18-bit TFT color LCDs.
			SUD6	**16-BIT STN COLOR UPPER BIT [6]:** This bit is Upper Data Bit 6 for 16-bit dual-scan and single-scan STN color LCDs.

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[19]	136	O	R3	**24-BIT TFT RED BIT [3]:** This bit is RED Color Data Bit 3 for 24-bit TFT color LCDs.
			R1	**18-BIT TFT RED BIT [1]:** This bit is RED Color Data Bit 1 for 18-bit TFT color LCDs.
			SUD7	**16-BIT STN COLOR UPPER BIT [7]:** This bit is Upper Data Bit 7 (MSB) for 16-bit dual-scan and single-scan STN color LCDs.
FP[20]	137	O	R4	**24-BIT TFT RED BIT [4]:** This bit is RED Color Data Bit 4 for 24-bit TFT color LCDs.
			R2	**18-BIT TFT RED BIT [2]:** This bit is RED Color Data Bit 2 for 18-bit TFT color LCDs.
			R0	**12-BIT TFT RED BIT [0]:** This bit is RED Color Data Bit 0 (LSB) for 12-bit TFT color LCDs.
			SUD0	**16-BIT STN COLOR UPPER BIT [0]:** This bit is Upper Data Bit 0 (LSB) for 16-bit dual-scan and single-scan STN color LCDs.
FP[21]	138	O	R5	**24-BIT TFT RED BIT [5]:** This bit is RED Color Data Bit 5 for 24-bit TFT color LCDs.
			R3	**18-BIT TFT RED BIT [3]:** This bit is RED Color Data Bit 3 for 18-bit TFT color LCDs.
			R1	**12-BIT TFT RED BIT [1]:** This bit is RED Color Data Bit 1 for 12-bit TFT color LCDs.
			R0	**9-BIT TFT RED BIT [0]:** This bit is RED Color Data Bit 0 (LSB) for 9-bit TFT color LCDs.
			SUD1	**16-BIT STN COLOR UPPER BIT [1]:** This bit is Upper Data Bit 1 for 16-bit dual-scan and single-scan STN color LCDs.
FP[22]	139	O	R6	**24-BIT TFT RED BIT [6]:** This bit is RED Color Data Bit 6 for 24-bit TFT color LCDs.
			R4	**18-BIT TFT RED BIT [4]:** This bit is RED Color Data Bit 4 for 18-bit TFT color LCDs.
			R2	**12-BIT TFT RED BIT [2]:** This bit is RED Color Data Bit 2 for 12-bit TFT color LCDs.
			R1	**9-BIT TFT RED BIT [1]:** This bit is RED Color Data Bit 1 for 9-bit TFT color LCDs.
			SUD2	**16-BIT STN COLOR UPPER BIT [2]:** This bit is Upper Data Bit 2 for 16-bit dual-scan and single-scan STN color LCDs.

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2.2 Flat Panel LCD Interface Pins *(cont.)*

Pin Name	Pin #	Pin Type	Pin Function	Description
FP[23]	140	O	R7	**24-BIT TFT RED BIT [6]:** This bit is RED Color Data Bit 7 (MSB) for 24-bit TFT color LCDs.
			R5	**18-BIT TFT RED BIT [4]:** This bit is RED Color Data Bit 5 (MSB) for 18-bit TFT color LCDs.
			R3	**12-BIT TFT RED BIT [3]:** This bit is RED Color Data Bit 3 (MSB) for 12-bit TFT color LCDs.
			R2	**9-BIT TFT RED BIT [2]:** This bit is RED Color Data Bit 2 (MSB) for 9-bit TFT color LCDs.
			SUD3	**16-BIT STN COLOR UPPER Bit [2]:** This bit is Upper Data Bit 3 (for 16-bit dual-scan and single-scan STN color LCDs.
FPDE	108	O		**FLAT PANEL DISPLAY ENABLE:** For those LCDs that require an external display enable, this pin is used to provide a data enable. For the CL-GD7542, it is the second Shift Clock output for single-scan dual-clock STN color LCDs.
FPVDCLK	113	O		**FLAT PANEL VIDEO CLOCK:** This signal is used to drive the LCD shift clock which is designated as CP2 by some LCD manufacturers.
LFS	110	O		**LCD FRAME START:** This output provides a pulse to start a new frame on LCDs.
LLCLK	112	O		**LCD LINE CLOCK:** This output is used to drive the LCD line clock. This signal is also designated as LP or CP1 by some LCD manufacturers.
MOD	117	O		**MODULATION:** This output provides AC inversion. It should be connected to the MOD, FR, or DF inputs of the LCD, as appropriate. Some LCD manufacturers provide this function in the LCD circuitry, in which case this pin does not need to be connected.

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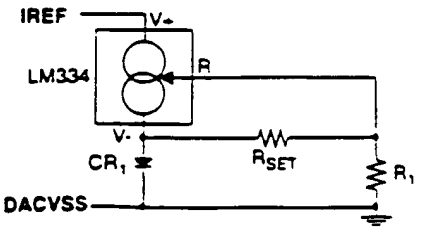
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2.3 CRT Interface Pins

Pin Name	Pin No.	Type	Description
BLUE	96	O	**BLUE VIDEO:** This analog output supplies current that corresponds to the blue value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 6-bit value from the Lookup Table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to the IREF signal as follows: $I_{full} = (63/30) \times IREF$ To maintain IBM VGA compatibility, each DAC output is typically terminated to monitor ground with a 150-ohm 2% resistor. This resistor, in parallel with the 75-ohm resistor in the monitor, will yield a 50-ohm impedance to ground. For a full-scale voltage of 700 mV, the full-scale current output should be 14 mA.
GREEN	97	O	**GREEN VIDEO:** This analog output supplies current corresponding to the green value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
HSYNC	91	3-S	**HORIZONTAL SYNC:** This output supplies the horizontal synchronization pulse to the monitor. The polarity of this output is programmable. This pin may be connected directly to the corresponding pin on the monitor connector.
IREF	99	I	**DAC CURRENT REFERENCE:** The current drawn from AVDD2/AVDD3 through this pin determines the full-scale output of each DAC. This pin should be connected to a constant-current source. For information on how to calculate the IREF constant current, refer to the IREF application note in the 7542 Applications Book.

Example:

V_{DD}	R_{SET} ± 1%	R_1 ± 1%	Diode CR_1
5.0 Volts	22.1 Ω	200 Ω	1N4148 or equivalent
3.3 Volts	15 Ω	121 Ω	Schottky Diode (V_F < 0.4V)



2.3 CRT Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Description
RED	98	O	**RED VIDEO:** This analog output supplies current corresponding to the red value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
VSYNC	93	3-S	**VERTICAL SYNC:** This output supplies the vertical synchronization pulse to the monitor. The polarity of this output is programmable. This pin may be connected directly to the corresponding pin on the monitor connector.

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2.4 NTSC and PAL Interface Pins

Because flat panel LCD control pins are used with NTSC and PAL interfaces, while the NTSC and PAL interface pins are used, flat panels should be isolated. External AND gates should be used to force flat panel control signals to the proper levels. (For design details, refer to the Application Note on NTSC.)

Name	Pin No.	Type	Description
BLUE	96	O	**BLUE VIDEO:** This analog output supplies current corresponding to the blue value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 6-bit value from the Lookup Table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to IREF as follows: $I_{full} = (63/30) \times IREF$ When an NTSC/PAL Encoder is used at the same time as the CRT, there must be a 1.4k-ohm series termination resistor between the CL-GD7542 and the R, G, and B inputs of the encoder. There is also a 0.7k ohm resistor connected to ground from each R, G, and B input, to provide the correct input-voltage level for the encoder. To maintain a full-scale voltage of 700 mV across the CRT inputs, the full-scale current output should be 14 mA. For termination details, refer to Section 2.3.
CSYNC	95	O	**COMPOSITE SYNC:** This output provides the Composite SYNC for the analog NTSC/PAL Encoder. For NTSC/PAL interfaces, connect CSYNC to the Encoder SYNC input.
GREEN	97	O	**GREEN VIDEO:** This analog output supplies current corresponding to the green value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
NTSC/PAL	94	O	**NTSC/PAL ENCODING SELECTION:** This output is used by the CL-GD7542 to select the desired NTSC or PAL encoding format. Register bits CR30[3:2] control the level on this pin.
RED	98	O	**RED VIDEO:** This analog output supplies current corresponding to the red value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
TVON	146	O	**TVON:** When SR25[6] = 0, this output controls the power to the NTSC/PAL Encoder. When this output is high, the encoder is powered on. When this output is low, the encoder is turned off.
XRDACCS			**EXTERNAL RAMDAC CHIP SELECT:** When SR25[6] = 1, a high on this output is used to enable an external RAMDAC. This function is not supported for PCI bus applications.

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2.5 Dual-Frequency Synthesizer Interface Pins

Pin Name	Pin No.	Type	Description
CLK32k	89	I	**32-kHz CLOCK:** This input may be connected to an externally supplied 32-kHz clock signal to be used for memory refresh during Suspend Mode. If this pin is not used, it should be tied to ground.
MCLK/XMCLK	197	I/O	**MCLK/XMCLK:** When SR23[3] = 0, the internal MCLK is available on this pin. When SR23[3] = 1, this pin is used as an input from an external XMCLK source. These configurations are intended for testing only.
MFILTER	200	O	**MEMORY CLOCK FILTER:** This pin must be connected to a Pi RC filter which is returned to MAVSS. The filter components, especially the input capacitor and the resistor, must be placed as close as possible to the MFILTER pin.

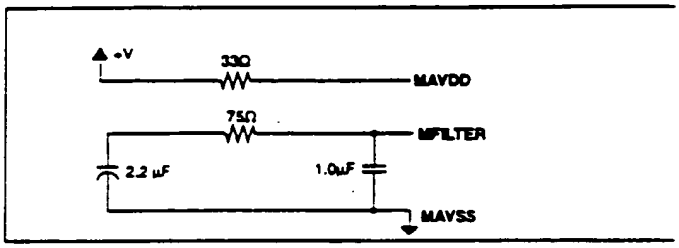


Figure 2–1. Typical Memory Clock Filter

OSC	85	I	**OSCILLATOR INPUT:** This TTL input pin supplies the reference frequency for the Dual-frequency Synthesizer. It requires an input frequency of 14.31818 MHz ± 0.01% with a duty cycle of 50% ± 10%. This input can be supplied from the appropriate pin on the PCI Bus, or from an oscillator.
XVCLK		I	**XVCLK INPUT:** External video clock source input – intended for testing only.
VFILTER	83	O	**VIDEO CLOCK FILTER:** This pin must be connected to a Pi RC filter which is returned to VAVSS. The filter components, especially the input capacitor and the resistor, must be placed as close as possible to the VFILTER pin.

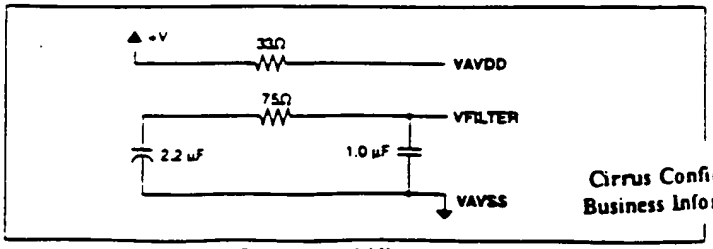


Figure 2–2. Typical Video Clock Filter

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2.6 Display Memory Interface Pins

Pin Name	Pin No.	Type	Description
CAS#	181	O	**COLUMN ADDRESS STROBE#:** This active-low output is used to latch the column address from MA[9:0] into the DRAMs. When register SRF[0] = 0 (dual-WE# DRAMs), this pin is defined as CAS#, and must be connected to the CAS# inputs of the DRAMs.
WE#			**WRITE ENABLE#:** When register SRF[0] = 1 (dual-CAS# DRAMs), this pin is defined as WE#, and must be connected to the WE# inputs of the DRAMs.
CAS[3:0]#	169:170	O	**COLUMN ADDRESS STROBE#:** These active-low outputs are used to control the CAS# (or WE#) inputs to the DRAMs. When register SRF[0] = 1 (dual-CAS# DRAMs), these active-low outputs must be connected to the CAS# inputs of the DRAMs.
WE[3:0]#	169:170, 195:194		**WRITE ENABLE# [3:0]:** When register SRF[0] = 0 (dual-WE# DRAMs), these active-low outputs must be connected to the WE# inputs of the DRAMs.
MA[9:0]	171:180	O	**MEMORY ADDRESS [9:0]:** These outputs drive the address inputs of the DRAMs.
MD[31:0]	151:161, 163:167, 186:191, 193,196, 202:204, 206:208,1:2	I/O	**MEMORY DATA [31:0]:** These 32 bidirectional pins are used to transfer data between the CL-GD7542 and display memory. These pins must be connected to the data pins of the DRAMS.
OE#	182	O	**OUTPUT ENABLE#:** This active-low output is used to control the Output Enables of the DRAMs. For 256K x 16 DRAMs with Dual-Write Enables, this pin must be connected to the OE# pins of all the DRAMs in the display memory array.
RAS#[1:0]	184:183	O	**ROW ADDRESS STROBE#:** These active-low outputs are used to latch the row address from MA[9:0] into the DRAMs. Each RAS pin is used for one bank of memory, for a total of two banks. These pins must be connected to the RAS# pins of all the DRAMs in the display memory array.

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2.7 Configuration Input Pins

During the rising edge of Reset#, the levels on these configuration input pins are read and stored in register SR22 and SR24[7].

Pin Name	Pin No.	Type	Description
FC	157	I	**FEATURE CONNECTOR:** When an external pull-up resistor (<60k ohms) is attached to this pin, a logic high is read and stored in SR24[7] during the rising edge of the Reset# pulse. This high level configures the CL-GD7542 to supply all the Feature Connector signals. (Refer to section 2.10.) When no pull-up, this pin is configured for other operations.
FVL	165	I	**FAST VESA Local BUS:** When an external pull-up resistor (<60k ohms) is attached to this pin, a logic high is read and stored in SR22[2] during the rising edge of the Reset# pulse. This high level configures the CL-GD7542 for a 50-MHz bus clock input. (Refer to Note a.)
PCI	167	I	**PCI BUS SELECT:** When an external pull-up resistor (<60k ohms) is attached to this pin, a logic high is read and stored in SR22[0] during the rising edge of the Reset# pulse. This high level configures the CL-GD7542 for PCI bus operation, and a minimum-grant value of 250 ns. PCI Burst Mode is selected when this pin is high and GRE[4] = 1. (Refer to Note a.)
PCI-MGE	159	I	**PCI BUS with MEMORY-GRANT EXTEND:** When an external pull-up resistor (<60k ohms) is attached to this pin, a logic high is read and stored in SR22[7] during the rising edge of the Reset# pulse. This high level configures the CL-GD7542 to support the PCI bus, and to extend the minimum-grant value from 250 ns to 500 ns. PCI Burst Mode is selected when this pin is high and register GRE[4] = 1. (Refer to Note a.)
S46	161	I	**SLEEP ADDRESS SELECT:** When an external pull-up resistor (<60k ohms) is attached to this pin, a logic high is read and stored in SR22[5] during the rising edge of the Reset# pulse. This high level selects the sleep address at 46E8[3], which is used when the CL-GD7542 is used as an adapter. When no pull-up resistor is supplied, the CL-GD7542 selects a sleep address at 3C3[0], which is the normal mother-board configuration.
XCLK	164	I	**EXTERNAL CLOCK SELECT:** An external pull-up resistor configures the CL-GD7542 for external clock inputs on the SW0 / MCLK / XMCLK and OSC / XVCLK pins. This configuration is used for testing only, and no pull-up resistor should be attached during normal operation. When no resistor is supplied, the CL-GD7542 uses its internal clock sources.

Note a. To choose the system bus, only one pull-up resistor may be supplied on PCI-MGE (pin 159), FVL (pin 165), or PCI (pin 167). When no pull-up resistor is supplied, the CL-GD7542 is configured for a VESA Local bus operation of 33 MHz or less.

2.8 Switch and Miscellaneous Configuration Input Pins

Pin Name	Pin No.	Type	Description
SW0	197	I	**SWITCH 0:** This pin is configured as a hardware input that can be read under register control. The level on this pin is stored in register SR24[0].
SW1	149	I	**SWITCH 1:** This pin is configured as a hardware input that can be read under register control. The level on this pin is stored in register SR24[1].
SW2	150	I	**SWITCH 2:** This pin is configured as a hardware input that can be read under register control. The level on this pin is stored in register SR24[2].
TWR#	100	I	**TEST WRITE#:** This active-low input is for factory testing and must not be connected to the system for normal operation. It has an internal pull-up resistor.

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2.9 Power Management Pins

Pin Name	Pin No.	Type	Description
ACTI	86	I	**ACTIVITY:** When SR23[6] = 1, this pin is an optional activity-sense input. With register masking, any low-to-high transition on this input may be used to reset the internal power-down timers. When SR23[6] = 1 and CR2D[6] = 1, the ACTI input when high can reset the Standby timer. When SR23[6] = 1 and CR2D[3] = 1, the ACTI input, when high, resets the Backlight timer.
SBYI			**STANDBY INPUT:** When SR23[6] = 0, this input is the hardware control for the Standby Mode. When SBYI goes high, it initiates the power-down sequence that starts the Standby Mode. When not used, this input should be connected to ground.
BLI	87	I	**BACKLIGHT INPUT:** When SR23[5] = 1, a high on this input turns off the backlight of the LCD display.
SUSPI			**SUSPEND INPUT:** When SR23[5] = 0, a high on this internally de-bounced input initiates hardware-controlled Suspend Mode. The hardware-controlled Suspend Mode is the most efficient power-saving mode for the system.
CLK32k	89	I	**32-kHz Clock:** This input may be connected to an externally supplied 32-kHz clock signal to be used for memory refresh during Suspend Mode. If not used, this pin should be tied to ground.
FPBL	105	O	**FLAT PANEL BACKLIGHT:** This output is part of the LCD power sequencing. It should be connected to the LCD backlight enable.
FPVCC	106	O	**FLAT PANEL VCC:** This output is part of the LCD power sequencing. It should be connected to the LCD logic-power enable.
FPVEE	102	O	**FLAT PANEL VEE:** This output is part of the LCD power sequencing. It should be connected to the LCD power enable.
PROG	148	O	**PROGRAMMABLE OUTPUT:** This output pin is forced high or low under the control of register CR30[7]. It is used by the BIOS to select 3.3V or 5.0V power supplies to support the operating frequencies selected.
SBYST#	123	O	**STANDBY STATUS#:** This output, when low, indicates that the CL-GD7542 is in Standby mode.
SLEEP#	81	I	**SLEEP#:** This active-low input is used by the external hardware to put the CL-GD7542 into bus Sleep mode.
SPST#	125	O	**SUSPEND STATUS#:** This output, when low, indicates that the CL-GD7542 is in Suspend mode.

2.10 Feature Connector Pins

When an external pull-up resistor (<60k ohms) is attached to the FC / MD[25] pin, a logic high is read and stored in SR24[7] during the rising edge of the Reset# pulse. This high level configures the CL-GD7542 to supply all the following Feature Connector signals. When no pull-up resistor is supplied, these pins are configured for other operations.

Pin Name	Pin No.	Type	Description
FCBLANK#	101	I or O	**FEATURE-CONNECTOR BLANK#:** When FCESYNC# is high, FCBLANK# is an output which supplies a blanking signal to the feature connector. When FCESYNC# is low, FCBLANK# is an input which can force RGB outputs to zero current.
FCDCLK	103	O	**FEATURE-CONNECTOR DOT CLOCK:** When the Feature Connector configuration is active, this pin provides the dot clock output to the subsystem that is driven by the Feature Connector.
VCLK			**VCLK:** Video clock output. This pin is intended to be used for testing only.
FCESYNC#	147	I	**FEATURE-CONNECTOR ESYNC#:** When this input is high, the HSYNC, VSYNC, and FCBLANK# outputs are enabled. When this input is low, the HSYNC and VSYNC outputs are forced to high-impedance (off), and FCBLANK# is configured as an input.
FCEVIDEO#	86	I	**FEATURE-CONNECTOR ENABLE VIDEO#:** This input controls the buffers on FCP[7:0]. When FCEVIDEO# is high, the FCP[7:0] pins are pixel data outputs. When FCEVIDEO# is low, the FCP[7:0] pins are inputs, and the contents of display memory are ignored.
FCP[7:0]	144:141, 134,133, 125, 123	I or O	**FEATURE-CONNECTOR PIXEL DATA:** When FCEVIDEO# is high, these pins are pixel data outputs that copy the pixel address to the palette RAM. When FCEVIDEO# is low, these pins are inputs that can be used to drive pixel data into the palette DAC.
FCVCLK	114	I	**FEATURE-CONNECTOR VIDEO CLOCK:** This pin should be connected to the pixel clock from the Feature Connector. (For more information, refer to SR23[7].)
OVRW#	115	O	**OVERLAY WINDOW:** This active-low output is asserted during the active portion of the video overlay window. It is intended to be used in applications involving video overlays. For additional connectivity information, see Appendix A8.

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2.11 Ground Pins

Pin Name	Pin No.	Description
DACVSS[1:2]	88, 111	**DIGITAL-TO-ANALOG CONVERTER VSS GROUND:** These two pins are used to supply ground reference to the Palette DAC of the CL-GD7542. Each pin **must** be connected to the Analog ground rail, which should be isolated from VSS (digital) ground.
MAVSS	201	**MCLK ANALOG VSS GROUND:** This pin is used to supply ground reference to the memory clock synthesizer of the CL-GD7542. This pin **must** be connected to the Analog ground rail, which should be isolated from VSS (digital) ground.
VAVSS	82	**VCLK ANALOG VSS GROUND:** This pin is used to supply ground reference to the video clock synthesizer of the CL-GD7542. This pin **must** be connected to the Analog ground rail, which should be isolated from VSS (digital) ground.
S[1:11]	6,42,52,67 80,104,124 145,168,185 198	**VSS (Digital) GROUND:** These 11 pins are used to supply ground reference for the core logic and pin groups of the CL-GD7542. Each pin **must** be connected directly to the ground rail. When a multi-layer board is used, each VSS pin **must** be connected to the ground plane.

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2.12 Power Pins

Pin Name	Pin No.	Description
BVDD[1:2]	47,73	**BUS VDD:** These two pins are used to supply either +3.3V or +5.0V to the bus interface pin group of the CL-GD7542. 1. Each pin **must** be connected directly to the VDD rail. 2. Each pin **must** be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. 3. When a multi-layer board is used, connect each BVDD pin to the power plane.
CRTVDD	92	**CRT VDD:** This pin is used to supply +3.3V or +5.0V to the CRT interface pin group of the CL-GD7542. 1. This pin **must** be connected directly to the VDD rail. 2. This pin **must** be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to the pin as possible. 3. When a multi-layer board is used, connect this CRTVDD pin to the power plane.
CVDD[1:4]	36,62, 121,192	**CORE VDD:** These four pins are used to supply +3.3V or +5.0V to the internal core logic of the CL-GD7542. 1. Each pin **must** be connected directly to the VDD rail. 2. Each pin **must** be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. 3. When a multi-layer board is used, connect each CVDD pin to the power plane.
DACVDD[1:2]	90, 109	**DIGITAL-TO-ANALOG CONVERTER VDD:** These two pins are used to supply +3.3V or +5.0V to the Palette DAC of the CL-GD7542. 1. Each pin **must** be connected directly to the VDD rail. 2. Each pin **must** be bypassed with 0.1-µF and 10 µF capacitors that have the proper high-frequency characteristics and are as close to each pin as possible. 3. When a multi-layer board is used, connect each DACVDD pin to the power plane.

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2.12 Power Pins *(cont.)*

Name	Pin No.	Description
FPVDD[1:2]	132,107	**FLAT PANEL VDD:** This pin is used to supply +3.3V or +5V to the flat panel interface pin group of the CL-GD7542. 1. Each pin must be connected directly to the VDD rail. 2. Each pin must be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to the pin as possible. 3. When a multi-layer board is used, connect these FPVDD pins to the power plane.
MAVDD	199	**MCLK ANALOG VDD:** This pin is used to supply +3.3V or +5.0V to the Memory Clock Synthesizer of the CL-GD7542. This pin must be connected to the VDD rail via a 33-ohm resistor and bypassed to MAVSS with 0.1 µF and 10 µF capacitors.
MVDD[1:2]	205,162	**MEMORY VDD:** These two pins are used to supply +3.3V or +5.0V to the internal memory (DRAM) interface pin group of the CL-GD7542. 1. Each pin must be connected directly to the VDD rail. 2. Each pin must be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. 3. When a multi-layer board is used, connect each MVDD pin to the power plane.
VAVDD	84	**VCLK ANALOG VDD:** This pin is used to supply +3.3V or +5.0V to the Video Clock Synthesizer of the CL-GD7542. This pin must be connected to the VDD rail via a 33-ohm resistor and bypassed to VAVSS with 0.1 µF and 10 µF capacitors.

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3. Functional Description

This section provides functional information and design guidelines for the CL-GD7542 Graphics User Interface Accelerator (GUIX) SVGA LCD Controller with MVA™.

3.1 General

The CL-GD7542 offers a tightly integrated, high-performance motherboard solution. Multiple designs can be developed, ranging from a relatively simple GUIX solution to a portable multimedia solution capable of displaying accelerated video playback windows with graphics or an overlaid live video window with graphics. All hardware necessary for CPU updates to memory, display refresh, and DRAM refresh is included in the CL-GD7542. A complete SVGA-compatible motherboard solution can be implemented with the CL-GD7542 plus two 256K x 16 DRAMs.

3.2 Functional Blocks

Figure 3–1 shows a block diagram of the CL-GD7542 GUIX SVGA LCD Controller with MVA. The functional blocks integrated in the CL-GD7542 are described in the following sections.

3.2.1 CPU Bus Interface

The CL-GD7542 connects directly to a '486/ VESA VL-Bus or a PCI bus. No additional logic circuitry is required to implement these bus interfaces.

486/VL-Bus

The CL-GD7542 interfaces directly to '486DX microprocessors and the VESA VL-Bus, at speeds up to 50 MHz with the core VDD at 5V. The CL-GD7542 supports both 1X and 2X bus clocks, but will require external circuitry to support the 2X clocks

PCI Bus

The CL-GD7542 interfaces directly to the PCI bus. No additional logic is required to support the CL-GD7542 multiplexed address and data pins. The CL-GD7542 executes 32-bit I/O and memory accesses at speeds up to 33 MHz. The CL-GD7542 also supports memory burst cycles. PCI bandwidth is at least 50% better utilized with burst cycles.

Linear Memory Addressing

The CL-GD7542 supports linear memory addressing, as an alternative to the standard VGA method of accessing display memory with 64-Kbyte segments. With linear memory addressing, the CL-GD7542 is configured so that it accesses display memory as a one- or two-MByte linearly addressed string of bytes.

For applications or drivers that support this method, Linear Memory Addressing improves graphics performance by simplifying access to display memory, since it is not necessary to calculate offsets into a relatively small window, nor is it necessary to test for a crossing of the window boundary.

The CL-GD7542 supports Linear Memory Addressing of the VGA address space, which may reside within any 1-Mbyte segment above the first 16 MBytes in a 4-GByte address space. For '486 local bus interfaces that use a 32-bit address, to select the desired 16-Mbyte partition with the A[31:24] address line, an external decoder may be needed. However, in general, there is no need for an external decode of the CPU addresses. Any one of the A[31] to A[24] lines can be directly connected to HIMEM0 or HIMEM1. For instance, if HIMEM1 is connected to A[31], then CL-GD7542 is mapped into the upper 2 GBytes of the CPU address space.

The register bits SR2D[7:6] extend the address space to 64 MBytes by re-mapping HIMEM0 and HIMEM1 within this address space. An external decoder may be needed only if a fully decoded 16M-byte partition within the 4 GByte address space is desired. The output from this address-line decoder drives the HIMEM0 and HIMEM1 inputs. The SR7[7:4] register is used to select the 1M-byte through 16M-byte range in any 16M-byte space allowed by the microprocessor. (Note: HIMEM0 and HIMEM1 are used only with VL-bus and 32-bit local buses).

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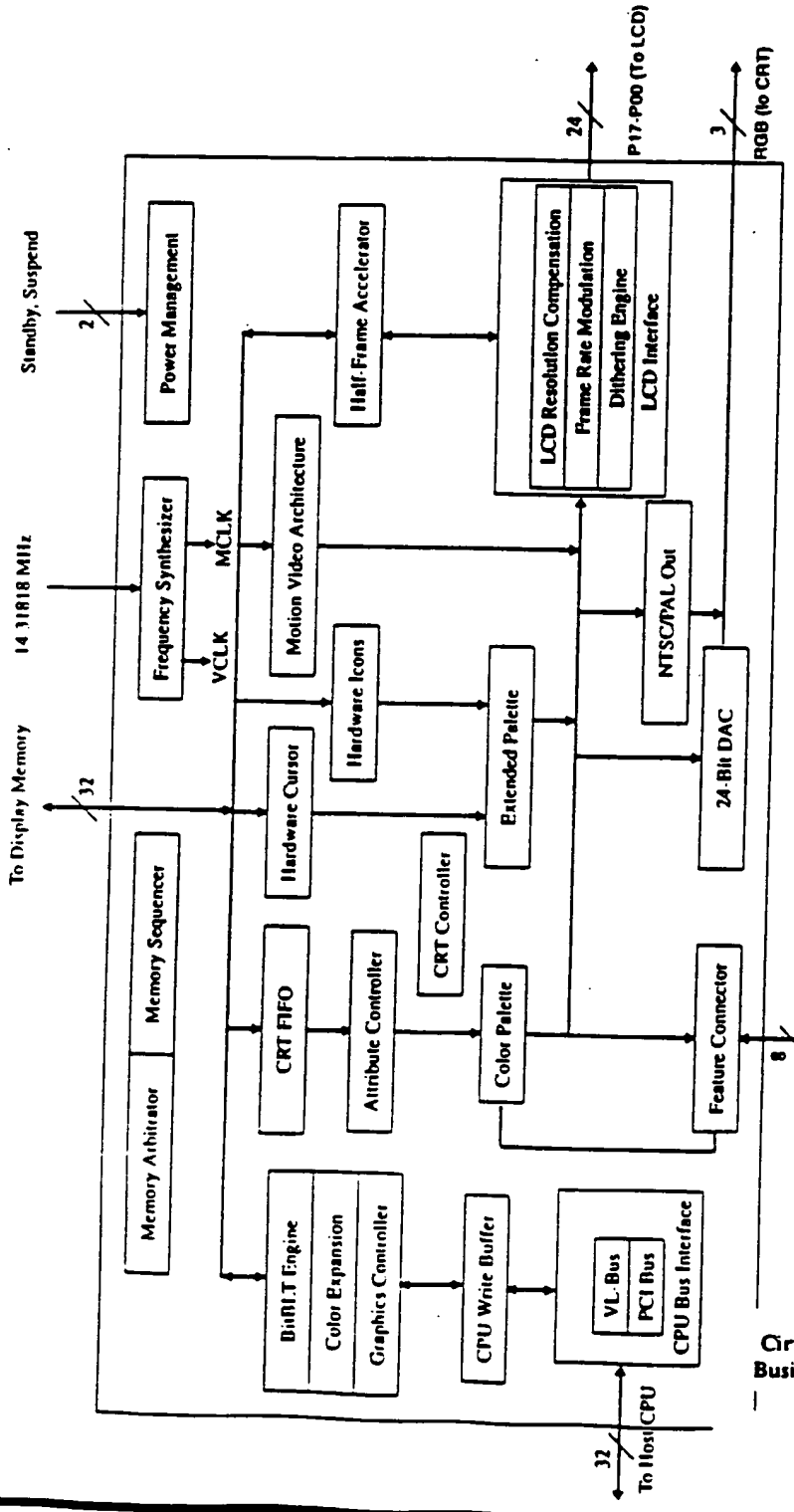


Figure 3–1. CL-GD7542 Block Diagram

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3.2.2 CPU Write Buffer

The CPU Write Buffer contains a queue of CPU write accesses to display memory that have not been executed due to memory arbitration. Maintaining this queue of write accesses allows the CL-GD7542 to release the CPU bus as soon as it has recorded the address and data. The CL-GD7542 therefore executes the operation when display memory is available, increasing CPU performance. For all text and graphics modes, the CL-GD7542's Write Buffer depth is two 32-bit or four 16-bit levels. The CL-GD7542 has the capability to page CPU cycles if they are accumulated in the write buffer.

3.2.3 Graphics Controller

The Graphics Controller operates in either text or graphics modes and performs the following major functions:

- Provides the host CPU a read/write access path to display memory
- Controls all four memory planes in planar modes
- Allows data to be manipulated prior to being written to display memory
- Formats data for use in various backward compatibility modes
- Provides color read comparators for use in color painting modes
- Reads/writes 32-bit words through the 32-bit display memory interface

The Graphics Controller directs data from the display memory to the CPU. Figure 3–2 and Figure 3–3 illustrate typical write and read operations, respectively.

For a write operation, the data from the CPU bus are combined with the data from the Set/Reset Logic in the CPU, depending on the Write mode. In addition, the data may be combined with the contents of the read latches, and some bits or planes may be masked (prevented from being changed) by using the Bit Mask Register. For more information, refer to the Graphics Controller registers in Section 6.5.

3.2.4 Color Expansion

Color expansion is the automatic conversion of a monochrome bit map (which typically defines a character, icon, or pattern) into foreground and background color values. These values are then written into display memory and held in a CL-GD7542 register.

Color Expansion improves CPU write performance by optimizing use of the available host bandwidth via expanding single bits across the bus into complete 8- or 16-bit pixels.

When color expansion is used, only monochrome bit maps must be transmitted across the bus. Each bit of the monochrome map is converted into 8-bit or 16-bit pixel modes. The bus traffic is reduced by a factor of 8 to 16, making it possible to use nearly all of the available display memory bandwidth.

3.2.5 Bit Block Transfer (BitBLT) Engine

The BitBLT (Bit Boundary Block Transfer) engine moves a rectangle of data either within display memory, or between system memory and display memory, with minimal CPU intervention. The BitBLT engine can also perform pattern fills (filling an area with a repeating pattern), raster operations (combining the source bytes with the destination bytes using various logic operations), and color expansion/ transparency.

The CL-GD7542's BitBLT engine provides 16 two-operand ROPs (Raster Operations) to move data in packed-pixel modes from the source area to the destination area. This operation occurs in packed-pixel modes with 8-bit or 16-bit pixel transfers. The transfers from CPU are always taken in four-byte increments. For screen-system transfers, the BitBLT operation acts as a read cache. The BitBLT accelerates Graphics User Interfaces (GUIs), such as Microsoft Windows 3.1, Windows NT, and OS/2 2.1. Refer to Appendix A1 "BitBLT Engine" for more information.

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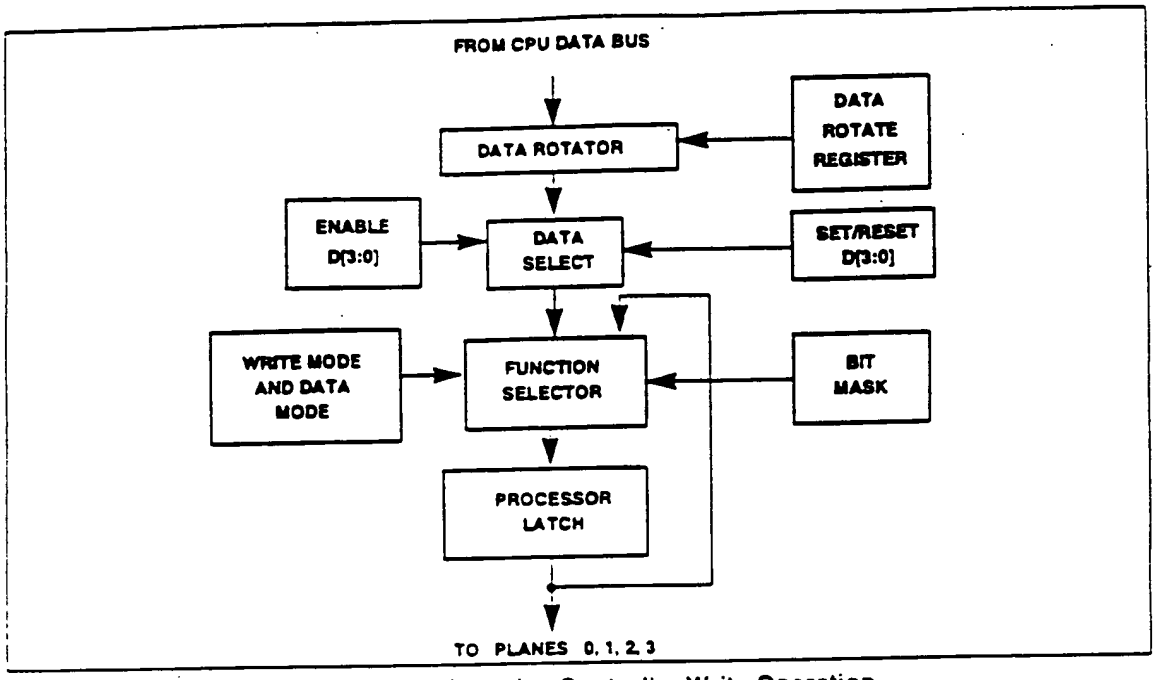


Figure 3–2. Graphics Controller Write Operation

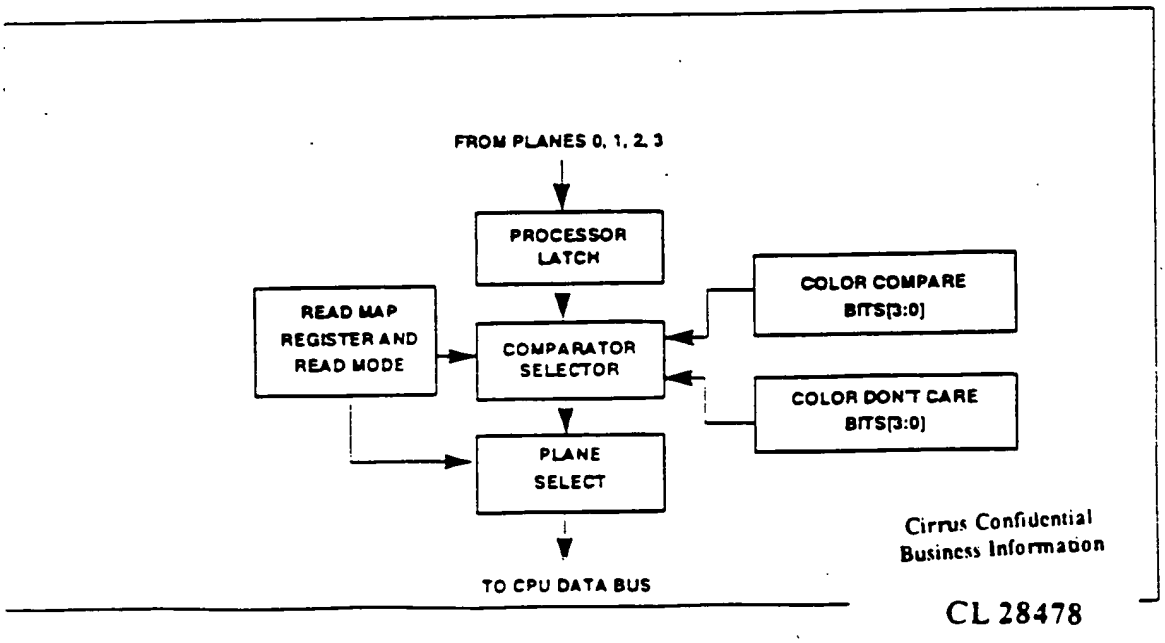


Figure 3–3. Graphics Controller Read Operation

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3.2.6 Memory Arbitrator

The Memory Arbitrator allocates bandwidth to the following functions, which compete for the limited bandwidth of display memory:

- CPU access
- Display refresh
- DRAM refresh
- BitBLT
- Half-Frame Accelerator (for dual-scan STN LCDs)
- Hardware Cursor
- Hardware Icons

DRAM refresh is handled invisibly by allocating a selectable number of CAS*-before-RAS* refresh cycles at the beginning of each scanline. Cycles are allocated to display refresh and CPU/BitBLT according to the FIFO-control parameters, with priority given to display refresh.

3.2.7 Memory Sequencer

The Memory Sequencer generates all necessary timing and control signals for display memory. This includes RAS*, CAS*, and multiplexed-address timing, as well as WE* and OE* timing. The Sequencer generates CAS*-before-RAS* refresh, random-read, random-early-write, fast-page-mode read, and early-write cycles. The Memory Sequencer generates multiple-CAS* or multiple-WE* signals, depending on the memory type being used. The CL-GD7542 supports the following memory configurations, which have a 32-bit-wide memory interface:

- Two 256K x 16 DRAMs for 1-MByte display memory
- Four 256K x 16 DRAMs for a 2-MByte display memory
- Four 512K x 8 DRAMs (symmetric only) for a 2-MByte display memory

The CL-GD7542 supports both dual-CAS# and dual-WE# 256K x 16 DRAMs.

Refer to Appendix A6 "Memory Configurations" for more information.

The Memory Sequencer ensures that the necessary display refresh transfer cycles and dynamic memory refresh cycles are executed and that the remaining memory cycles are made available for CPU read/write operations.

The CL-GD7542 fully supports all the standard IBM VGA memory organizations, along with the following extended video memory modes:

- 2-color packed-pixel modes (1-bit/pixel) in linear 32-bit words or VGA-style 8-bit words
- 16-color planar mode (4 bits/pixel)
- 16-color packed-pixel modes (4 bits/pixel), which is useful for PowerPC applications
- 256-color packed-pixel modes (8 bits/pixel)
- Direct-Color (32K or 64K colors) packed-pixel modes (16 bits/pixel)
- Mixed 32K- and 256-color packed-pixel modes (15 bits/pixel)
- True-Color 16.8M-color packed-pixel modes (24 bits/pixel)

In true packed-pixel addressing, consecutive pixels are stored at consecutive addresses. This is in contrast with VGA chain-4 addressing, a type of addressing that stores consecutive pixels at every fourth byte address in display memory. For more information, refer to Appendix A13 "Extended Video Modes Programming" and Appendix A5 "True Color Modes".

3.2.8 CRT FIFO Register

The CRT FIFO (First-In, First-Out) Register allows the Memory Sequencer to execute display memory accesses needed for display refresh at maximum memory speed, rather than at the display refresh rate. This register makes it possible to take advantage of DRAM's fast-page mode operation. The CRT FIFO Register is 16 words deep and 32 bits wide.

3.2.9 Attribute Controller Registers

The Attribute Controller Registers format the display for the screen. They perform the following:

- serialization of memory data
- display color selection
- text blinking
- underlining in both text and graphics modes

The Attribute Controller Registers are described in Section 6.6.

Figure 3–4 is a functional block diagram of the Attribute Controller.

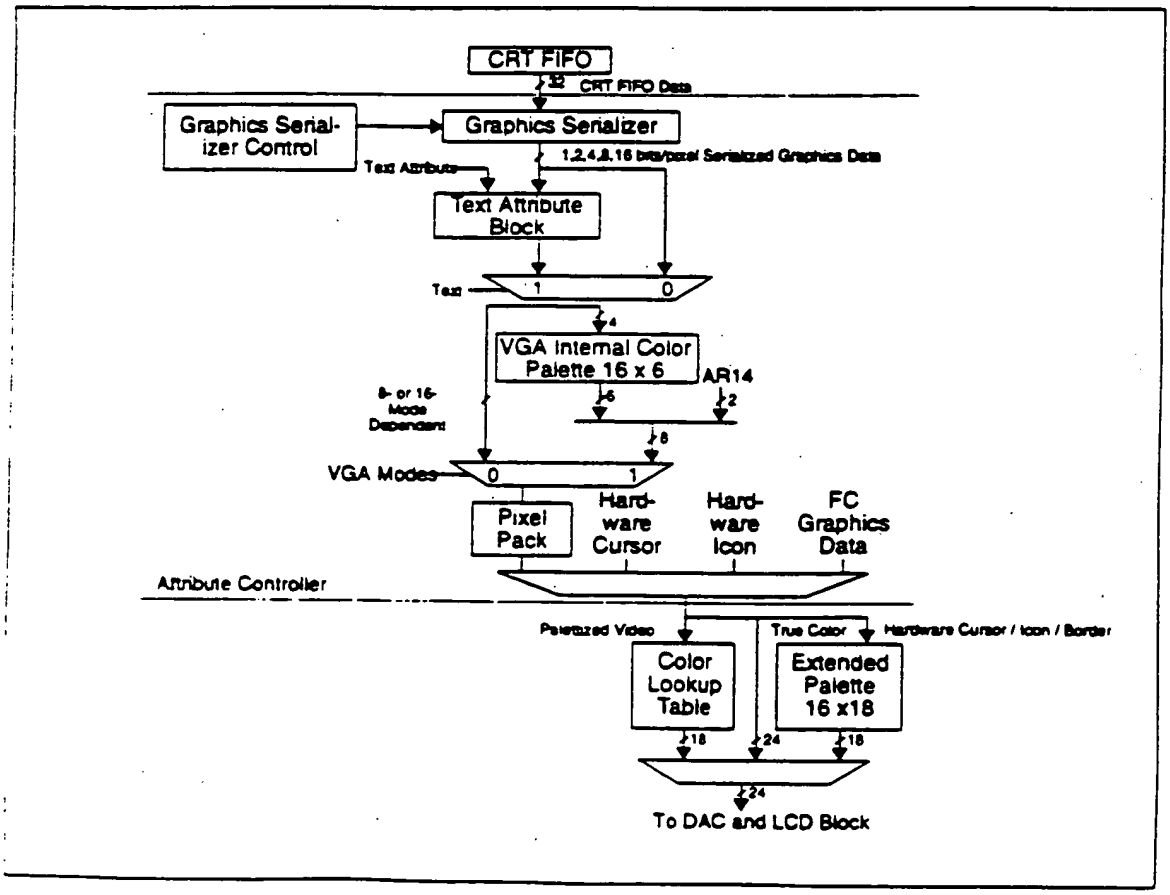


Figure 3–4. Attribute Controller Functional Block Diagram

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3.2.10 CRT Controller Registers

The CRT Controller (CRTC) Registers generate horizontal and vertical synchronization signals (HSYNC and VSYNC) for the CRT display. The CRTC Registers also generate the BLANK# signals required by the Palette DAC. In addition, they support both standard VGA-compatible modes and extended modes and provide for the following:

- configuration options, including user-configurable horizontal/vertical timing and polarity)
- cursor positioning
- horizontal scanlines
- pixel and byte panning
- split-screen capability and smooth scrolling

Figure 3–5 is a functional block diagram of the CRT controller.

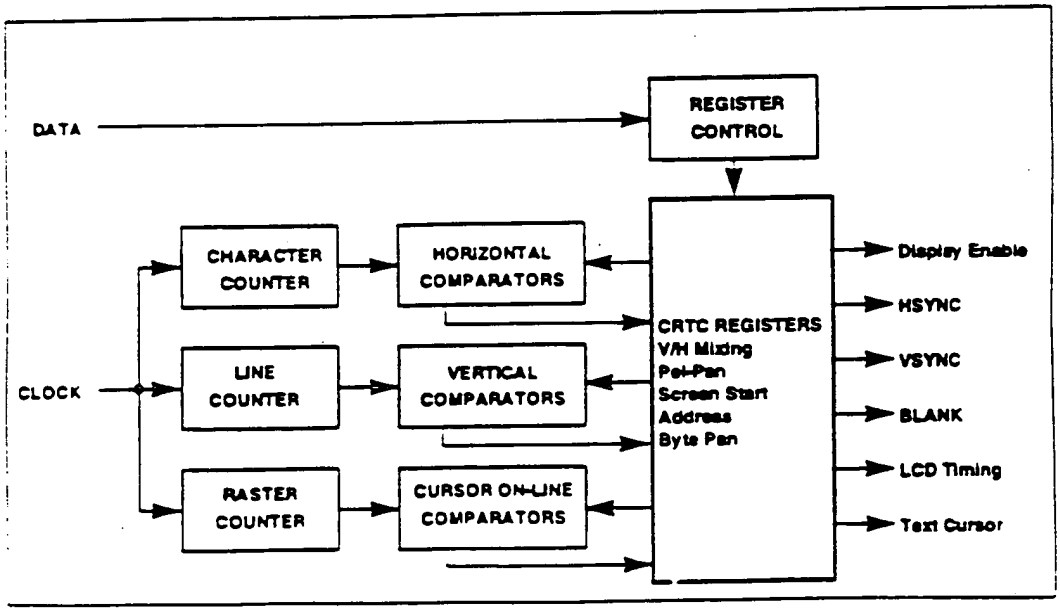


Figure 3–5. CRT Controller Functional Block Diagram

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In addition to supporting standard VGA text modes, the CL-GD7542 supports the following text modes: 132 x 25, 132 x 43, and 132 x 50.

In addition to supporting standard graphics modes, the CL-GD7542 supports the following graphics modes:

- For CRTs:
  - 1280 x 1024 interlaced, up to 16 colors
  - 1024 x 768 non-interlaced, up to 256 colors
- For CRTs and LCDs (non-interlaced)
  - 800 x 600, up to 64K colors
  - 640 x 480, up to 16.8M colors

SimulSCAN™, the simultaneous display capability, is supported at resolutions of 640 x 480 or 800 x 600. For a complete listing of all modes supported by the CL-GD7542, refer to Chapter 4.

Up to 1024 x 768 16-bit/pixel modes (that is, 5-5-5 or 5-6-5 R-G-B direct-color modes) are supported with either a 1X VCLK (pixel rate is equal to VCLK) or with a 2X VCLK (pixel rate is equal to twice the VCLK). The 640 x 480 24-bit/pixel modes (8-8-8, the R-G-B true-color modes) are supported with a 3X VCLK (that is, the pixel rate is equal to three times the VCLK).

3.2.11 Hardware Cursor

The hardware cursor replaces the software mouse pointer commonly used by GUI applications. The hardware cursor eliminates the need for application software to save and restore the display data as the mouse pointer position changes. The application software typically initializes the hardware cursor once, and from that point it needs only to update the cursor (x,y) position to move the cursor on the display.

The hardware cursor offers a smoothly moving mouse pointer with improved performance, as compared to a software cursor. The hardware cursor is always displayed on top of graphics, or video, or the hardware icons.

The hardware cursor consists of either 64 x 64 two-bit pixels or 32 x 32 two-bit pixels. Each pixel in the hardware cursor may be either transparent or one of two colors from an 18-bit palette.

The hardware cursor's palette is stored in the Extended Palette, such that it may be different from the VGA color palette.The first bit of each pixel in the hardware cursor defines whether or not the pixel is transparent. If the pixel is not transparent, the second bit defines the pixel's color. The second bit selects one of two 18-bit colors in the Extended Palette.

The following types of 2-bit hardware cursor patterns can be loaded into upper display memory:

- 64 x 64 hardware cursor patterns (up to 8 patterns)
- 32 x 32 hardware cursor patterns (up to 32 patterns)

After the hardware cursor patterns are loaded into upper display memory, application programs can quickly select one pattern as the active cursor pattern. The hardware cursor is available in all modes except text modes and mode 13. Note the hardware cursor is not supported in 640 x 480 24-bit/pixel modes. For more information, refer to Appendix A2 "Hardware Cursor".

3.2.12 Hardware Pop-up Icons

The CL-GD7542 provides hardware pop-up icons for displaying small, on-screen symbols that indicate system status (for example, a battery "fuel gauge"). These hardware icons are stored in upper display memory and can be displayed at the touch of a key. The hardware icons are independent of the graphics mode being used.

The CL-GD7542 supports two hardware icon modes:

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- Hardware Icon Mode 1.
  Up to four icons, each 64 x 64 pixels in size, can be displayed simultaneously in a vertical column. Each icon is independently controlled for color (up to 4 colors or 3 colors plus transparency). Each icon can be expanded either horizontally by pixel doubling, vertically by scanline doubling, or both horizontally or vertically to a maximum size of 128 x 128 pixels per icon.

- When one of the icons is doubled vertically, that icon extends down, which forces all other icons down.
- When one of the icons is doubled horizontally, that icon expands to the right of the display.
- Each of the four icons is allocated two memory maps. (A total of eight hardware icon memory maps can be stored in display memory.)

- Hardware Icon Mode 2.
  One 64 x 64 pixel hardware icon, from a menu of eight hardware icon memory maps, can be displayed. Each icon is independently controlled for color (up to 4 colors or 3 colors plus transparency) and for all other icon attributes (such as blink, horizontal and vertical doubling, icon enable, and memory map selection).

Hardware icon(s) are supported in all text and graphics modes, except 24-bit/pixel modes with a 3X clock, 16-bit/pixel modes with a 2X clock, and interlaced modes.

Hardware icon(s) are independent of the hardware cursor. When both a hardware cursor and hardware icon(s) are displayed, the hardware cursor passes on top of the hardware icon(s).

The CL-GD7542 priority of display overlays is as follows:

- Hardware cursor - always displayed on top
- Hardware icon
- MotionVideo™ Window data, or VGA graphics, or text data

3.2.13 Color Palette

The CL-GD7542 Color Palette consists of a 256 18-bit-word Color Lookup Table (CLUT). Each 18-bit word consists of three 6-bit values, one for each primary color (Red, Green, and Blue). The 18-bit word defines one of 2^{18} or 262,144 (referred to as "256K") colors.

The CLUT converts an 8-bit color code that specifies the color of a pixel into an 18-bit value, such that 256 simultaneous colors are displayed from a palette of 256K colors. Refer to Figure 3–6.

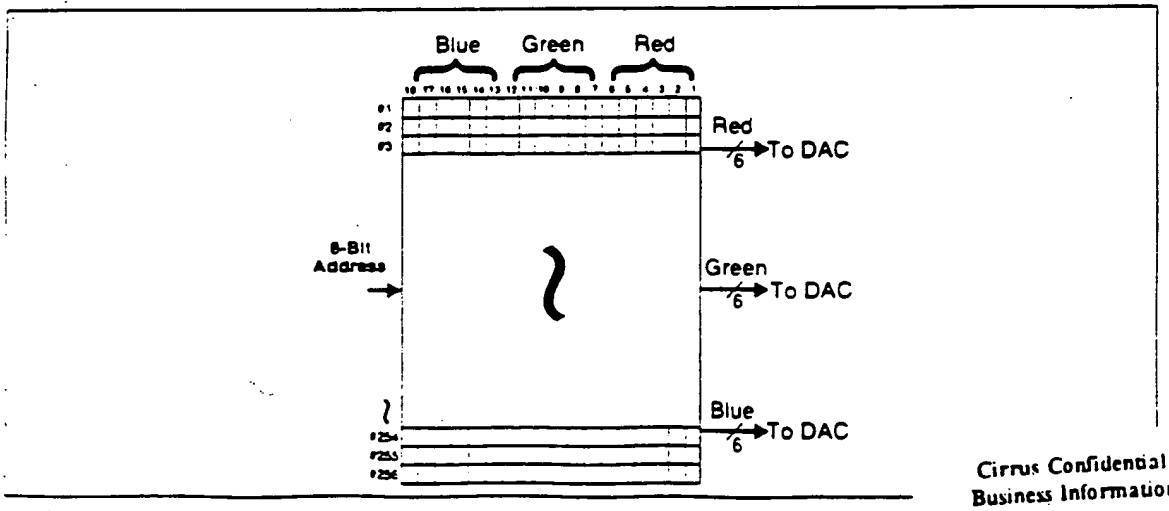


Figure 3–6. Color Lookup Table

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CL 28483

The contents of the CLUT are accessed via its 8-bit-wide host interface. An 8-bit address value applied to the pixel-address inputs defines the memory location for reading an 18-bit color data word from the CLUT.

An internal synchronizing circuit allows the color value accesses to be completely asynchronous to the pixel video operation. Special display operations, such as flashing objects and overlays, are possible because the palette incorporates a pixel word mask to allow the incoming pixel address to be altered. As a result, changes to the contents of the CLUT can be made immediately.

The CLUT has anti-sparkle circuitry to reduce random noise on the display during CPU accesses to the palette.

Direct-Color and True-Color Modes

In addition to graphics modes that use the 256 x18 CLUT, the CL-GD7542 supports the following Direct-Color and True-Color modes, which are useful in graphics and multimedia applications:

- 5-5-5 RGB 32K Direct-Color Mode.
  This mode bypasses the CLUT. Each pixel is represented by 15 bits, consisting of five bits each of Red, Green, and Blue color information to provide 32,768 (2^{15}) simultaneously displayed colors.
- 5-6-5 RGB 64K Direct-Color Mode.
  This mode bypasses the CLUT. Each pixel is represented by 16 bits, consisting of five bits of Red, six bits of Green, and 5-bits of Blue color information to provide 65,536 (2^{16}) simultaneously displayed colors.
- 8-8-8 RGB 16.8M True-Color Mode.
  This mode bypasses the CLUT. Each pixel is represented by 24 bits, consisting of one byte each of Red, Green, and Blue color information to provide 16,777,216 (2^{24}) simultaneously displayed colors.
- Mixed-Color Mode.
  This mode combines 256-color packed-pixel modes (which use the CLUT) and 5-5-5 RGB 32K-color modes (which bypass the CLUT).

  Each pixel consists of 16 bits. The pixel data bit [15] is used to select between the 5-5-5 RGB mode and the standard palette mode on a pixel-by-pixel basis.

For a block diagram showing the above-mentioned modes bypassing the CLUT, refer to Figure 3–7. For more information on true-color modes, refer to Appendix A5 "True-Color Modes".

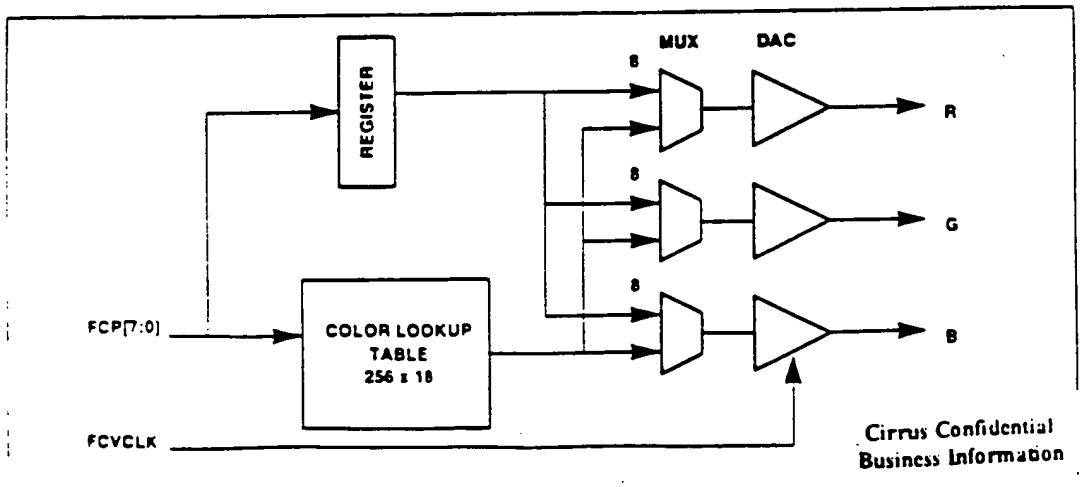


Figure 3–7. 256-Color Direct-Color Palette DAC

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Monochrome STN LCDs

On monochrome STN LCDs, the CL-GD7542 produces up to 256 gray scales. (For more information on gray scales, refer to Section 3.2.20 and Section 3.2.23.)

For graphics modes, these outputs -- the 6-6-6 RGB (from the CLUT), the 5-5-5 RGB, 5-6-5 RGB, and the 8-8-8 RGB – are converted to either 64 or 256 gray scales. The conversion to gray scales takes place by programming register CR1E[7:6] for one of the following three options:

- NTSC weighting
  (30% Red + 59% Green + 11% Blue)
- Green-only
- Attribute controller (6-bits)

For text modes, pixel data is converted into gray scales as follows:

- 4-bit pixel data (4 bits for foreground/background color) is directly converted into 16 gray scales.
- 6-bit pixel data (the lower 6 of 8 bits packed-pixel) is directly converted into 64 gray scales.

The CL-GD7542 also provides the following types of text contrast enhancements:

- General Contrast Enhancement:
  - If the background color is *greater* than the foreground color, the foreground color is set to 0, and the background color remains unchanged.
  - If the background color is *less* than the foreground color, the background color is set to 0, and the foreground color remains unchanged.
- Foreground-Only Contrast Enhancement:
  - If the background color is *greater* than the foreground color, the foreground color is set to 0 and the background color remains unchanged.
  - If the background color is *less* than the foreground color, the foreground color is set to 7 and the background color remains unchanged.

The CL-GD7542 provides reverse video:

- Reverse video for text modes is provided by programming register CR1E[5].
- Reverse video for graphics modes is provided by programming register CR1E[4].

3.2.14 Extended Palette RAM

The CL-GD7542's Extended Palette RAM provides 18-bit/pixel data (6-6-6 RGB) for the following functions:

- Hardware cursor
- Hardware icon
- Overscan border color

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As shown in Table 3–1, the Extended Palette RAM enables the colors of the hardware cursor, hardware icons, and the border to be programmed independently from the standard 256 x 18 VGA Color Lookup Table.

Table 3–1. Extended Palette RAM

I/O Address	Physical RAM Location	Function
X0h	256	Hardware cursor background color
XFh	257	Hardware cursor foreground color
X2h	258	Fix color of overscan (the border)
X3h	259	Hardware icon color #0 (Not for 3 colors + transparent mode)
X4h	260	Hardware icon color #1
X5h	261	Hardware icon color #2
X6h	262	Hardware icon color #3
XCh	268	Used by Video BIOS
XDh	269	Used by Video BIOS
XEh	270	Used by Video BIOS

3.2.15 Triple DAC

The DAC includes three 8-bit digital-to-analog converters (DACs). The DAC outputs drive the Red, Green, and Blue color video inputs to the CRT. The DAC outputs are designed to produce a 0.7-volt peak-white amplitude when supplied with a reference current (IREF). The IREF current is supplied with the circuit shown in the IREF pin description in Chapter 2. For all IREF values and output loading:

- $V_{Black\ Level}$ = 0 volts
- $V_{Maximum\ White}$ = 0.7 volts

Two sense methods — analog and digital — can be used to detect the type of CRT monitor that is connected.

With the analog sense method, the CL-GD7542 places specific color values on the RGB lines and then compares the resulting voltage level against a known internal reference voltage.

Extended graphics modes are capable of 75-Hz vertical refresh rates in a non-interlaced format.

- With the core voltage CVDD = 5.0V, the DACs operate up to 85 MHz and support the non-interlaced refresh rates shown in Table 3–2.
- With the core voltage CVDD = 3.3V, the DACs operate up to 65 MHz and support the non-interlaced refresh rates shown in Table 3–2.

For information on CRT-only video modes, refer to Section 4.1.

Table 3–2. Refresh Rates for CRTs in SimulSCAN Mode

Panel Type	Bits/Pixel	Refresh Rate for CRTs in SimulSCAN Mode					
		Case 1. CRTs in SimulSCAN Mode with Single-Scan STNs[a]		Case 2. CRTs in SimulSCAN Mode with Dual-Scan Color STNs[a]		Case 3. CRTs in SimulSCAN Mode with Dual-Scan Mono STNs[a]	
		50-MHz MCLK	45-MHz MCLK	50-MHz MCLK	45-MHz MCLK	50-MHz MCLK	45-MHz MCLK
640 x 480	8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	75 Hz	75 Hz
640 x 480	16 bpp	75 Hz	75 Hz	70 Hz	60 Hz	75 Hz	71 Hz
640 x 480	24 bpp	60 Hz	56 Hz	48 Hz	44 Hz	56 Hz	56 Hz
640 x 480	80-character text	75 Hz	75 Hz	75 Hz	72 Hz	75 Hz	75 Hz
800 x 600	8 bpp	75 Hz	75 Hz	65 Hz	61 Hz	75 Hz	75 Hz
800 x 600	16 bpp	58 Hz	55 Hz	45 Hz	39 Hz	54 Hz	47 Hz
800 x 600	80-character text[b]	60 Hz	60 Hz	54 Hz	56 Hz	58 Hz	58 Hz
1024 x 768	8 bpp	71 Hz	66 Hz	Not supported			
1024 x 768	16 bpp	Not supported					

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a. In Case 1, the refresh rate is given for CRTs that are used in SimulSCAN mode with single-scan STNs.
In Case 2, when CRTs are used in SimulSCAN mode with dual-scan color STNs, the dual-scan STN LCDs have double the CRT refresh rates shown in the table.
For LCDs not in the SimulSCAN mode, it is possible to achieve higher refresh rates by reducing the non-display time.

b. Character cells are 10 dots wide, whether or not the text is expanded.

3.2.16 MotionVideo™ Architecture

The MotionVideo™ Architecture (MVA™) provides the following video multimedia features:

- Cost-effective, high-quality video-playback hardware acceleration for file formats
- Video playback of other file formats (for example MPEG, the Motion Picture Experts Group format) via a software driver that is compatible with the Device Control Interface (DCI)

Video playback using a VGA controller *without* MVA has a number of limitations:

- The video playback's pixel color depth must be the same as the pixel color depth of the surrounding graphics. For a 24-bit/pixel video playback window, the entire 640 x 480 or 800 x 600 display must operate in 24-bit/pixel modes.
- Pixel performance on a 640 x 480 24-bit/pixel display is very slow, because bandwidth is limited by the 32-bit display memory interface.
- With a 32-bit display memory interface, 800 x 600 and 1024 x 768 24-bit/pixel resolutions are not possible. The display memory interface would require 2 to 3 MBytes of display memory, with a 64-bit wide display memory interface, which is not economical in mainstream notebooks.
- Mixing video and graphics functions such as zooming in software introduces additional overhead and does not alleviate the display memory bottleneck.

When playing back video while using a VGA controller *without* the MVA advantage, the above limitations result in the following disadvantages:

- the video playback window's pixel color depth is low (typically 8 bits per pixel)
- the screen resolution is small (typically 160 x 120 or 320 x 240)
- the frame rate is low (typically 15 frames/second)
- the graphics performance is sluggish
- the display memory requirements are high

3.2.16.1 MotionVideo™ Window

MVA creates a MotionVideo Window that utilizes off-screen memory and which is positioned on top of the VGA graphics mode data. (The hardware icons and hardware cursor are displayed on top of the MotionVideo Window).

The MotionVideo Window functions as an overlay image that can be positioned anywhere on the display. Position and size of the MotionVideo™ Window are programmable via registers CR3X, with 8-pixel horizontal resolution and 1-scanline vertical resolution.

The MotionVideo Window can be displayed with SimulSCAN on both CRT monitors and the following LCDs:

- 640 x 480
- 800 x 600

With MVA, the display memory becomes a multi-format display memory. As a result, as listed below, different color pixel depths and data formats can be mixed in the MotionVideo™ Window display.

- The MotionVideo Window's color pixel depth is independent of the color pixel depth of the surrounding graphics.
  - For example, a MotionVideo Window may operate in a 24-bits/pixel mode, while the surrounding graphics operate in a 8-bits/pixel or 4-bits/pixel mode (even in planar modes).
- 640 x 480 Single-Scan Color/Mono LCDs
- 640 x 480 Dual-Scan Color/Mono LCDs
- 800 x 600 Single-Scan Color/Mono LCDs
- 800 x 600 Dual-Scan Color/Mono LCDs
- The MotionVideo Window's data format is independent of the data format of the surrounding graphics.
  - For example, 4:2:2 YUV video data can be stored with 4-bit or 8-bit RGB graphics data in the display memory. (The 4:2:2 YUV format is compressed, since 4:2:2 uses an average of 16-bits/pixel to provide the same color quality as 24-bit/pixel RGB modes.)

This mixing of color pixel depth modes and data formats provides high-quality video playback, along with high-performance graphics, while minimizing display memory requirements.

The MotionVideo Window's video data is stored in MotionVideo Memory, a contiguous portion of off-screen display memory. As shown in Figure 3–8, MotionVideo Memory is located as follows:

- *above* graphics memory (where pixel data for standard and extended VGA modes is stored).
- *in* the half-frame accelerator if and only if a dual-scan LCD is used.
- *below* the last 16KB of display memory (where data for the hardware cursor and the hardware icons is stored.

Off-screen display memory is not required when the MotionVideo Window and surrounding graphics use the same pixel color depth and format.

During display refresh, data is accessed from either MotionVideo Memory or Graphics Memory on a pixel-by-pixel basis.

Note that no double accesses to display memory are required, alleviating the display memory bandwidth bottleneck.

Any data format supported by MVA can be displayed. Furthermore, new data formats can be added as needed.

The MotionVideo Window (MVW) supports the following color space formats:

- 24-bit/pixel RGB 8-8-8
- 16-bit/pixel 4:2:2 YUV linear (Y0UY1V)
- 16-bit/pixel RGB 5-6-5
- 16-bit/pixel RGB 5-5-5
- 8-bit/pixel RGB 3:3:2 through the palette
- 8-bit/pixel RGB 3-3-2 (3:3:2) direct

For a description of 16-bit/pixel and 24-bit/pixel RGB formats, refer to Section 3.2.13.

The MVA optimizes display memory bandwidth while minimizing display memory requirements. As a result, high-quality MVWs may be displayed with high-resolution graphics modes by using only 1 MByte of display memory.

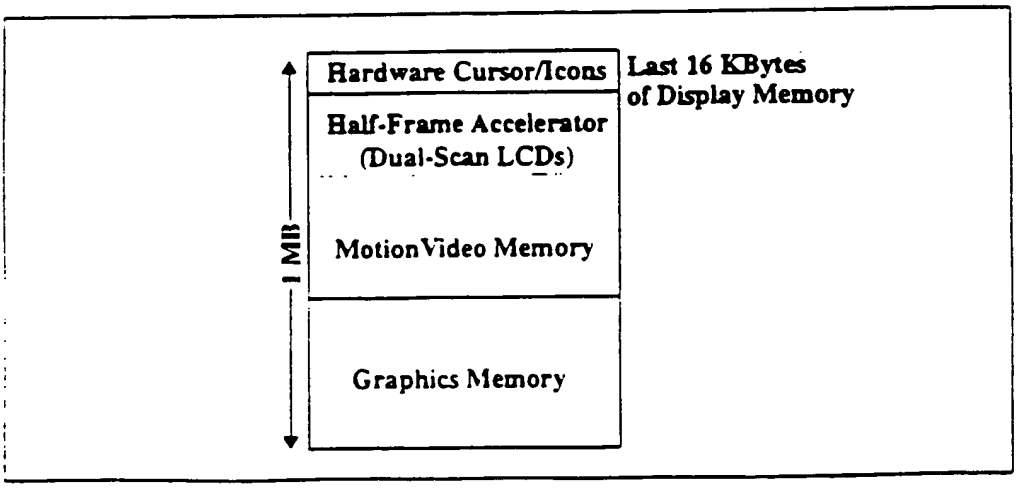


Figure 3–8. MotionVideo™ Memory, Stored as Part of Display Memory

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Table 3–3 shows the graphics display modes that are possible when using various combinations of MotionVideo Windows and when up to 1 MByte of display memory is available. Note that:

- With a 640 x 480 graphics display mode (on either a color TFT LCD, STN LCD, or a CRT) the following MVWs may be displayed:
  - A 640 x 480 (full-screen) MVW, with 8, 16, or 24 bits/pixel format. Surrounding graphics display modes (SGDMs) may be 4, 8, or 16 bits/pixel.
  - A 320 x 240 MVW, with any bits/pixel format. SGDMs may be 4, 8, 16, or 24 bits/pixel.
- With an 800 x 600 color graphics display mode (on either a color TFT LCD or a CRT), the following MVWs may be displayed:
  - A 640 x 480 MVW, with 8 bits/pixel format. SGDMs may be 4 or 8 bits/pixel.
  - A 640 x 480 MVW, with 16 bits/pixel format. SGDMs may be 4 bits/pixel.
  - A 320 x 240 MVW, with 8 or 16 bits/pixel. SGDMs may be 4 or 8 bits/pixel.
  - MVWs with SGDMs of 24 bits/pixel are not possible because of the display memory size and the 32-bit memory interface.
- With a 800 x 600 color dual-scan STN LCD, MVWs may not be displayed with 800 x 600 single-scan displays since a portion of the display memory is used for the Half-Frame Accelerator.
- With a 1024 x 768 color graphics display mode, the following MVWs may be displayed:
  - A 640 x 480 MVW, with 8 bits/pixel. SGDMs may be 4 bits/pixel.
  - A 320 x 240 MVW, with 8 bits/pixel. SGDMs may be 4 or 8 bits/pixel.

The MVW's pixel color depth corresponds to the formats above. The MVWs resolution is for the source data. Using hardware "zooming," this resolution may be doubled horizontally and vertically on the display. For more information, refer to Section 3.2.16.2.

Table 3-3. MotionVideo™ Window / Graphics Modes Possible with 1-MByte Display Memory

Type of LCD Display or CRT Monitor	Graphics Display Modes					MotionVideo Window			
	Resolution	(Bits Per Pixel)				Resolution	(Bits Per Pixel)		
		4	8	16	24		8	16	24
Color TFT LCD	640 x 480	Full-screen MVW				640 x 480	✓	✓	✓
		✓	✓	✓	✓	320 x 240	✓	✓	✓
Color Dual-Scan STN LCD		Full-screen MVW				640 x 480	✓	✓	✓
		✓	✓	✓	✓	320 x 240	✓	✓	✓
Color TFT LCD	800 x 600	Full-screen MVW				800 x 600	✓	✓	
		✓	✓			640 x 480	✓		
		✓					✓	✓	
		✓	✓	✓		320 x 240			
		✓	✓				✓	✓	
Color Dual-Scan STN LCD		Full-screen MVW				800 x 600	✓		
		✓	✓			640 x 480	✓		
		✓					✓	✓	
		✓	✓			320 x 240	✓	✓	
CRT Monitor	1024 x 768	Full-screen MVW				1024 x 768	✓		
		✓	✓			640 x 480			
		✓					✓		
		✓	✓			320 x 240	✓		

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Table 3–4 shows combinations of MVWs (resolutions and color depths) and surrounding graphics modes (resolutions and color depths) available for various displays that have 2 MBytes of display memory. With 2 MBytes of display memory, a MVW up to 800 x 600 16-bits/pixel can be combined with 800 x 600 16-bit/pixel graphics. A MVW up to 640 x480 16-bits/pixel can be combined with 1024x768 8-bit/pixel graphics. In addition, 2 MBytes of display memory enables the software drivers to optimize performance by using 64 KBytes to 256 KBytes for cacheing.

Table 3–4. MotionVideo Window / Graphics Modes Possible with 2-MByte Display Memory

Type of LCD Display or CRT Monitor	Graphics Display Modes					MotionVideo Window			
	Resolution	(Bits Per Pixel)				Resolution	(Bits Per Pixel)		
		4	8	16	24		8	16	24
Color TFT LCD	640 x 480	Full-screen MVW				640 x 480	✓	✓	✓
		✓	✓	✓	✓	320 x 240	✓	✓	✓
Color Dual-Scan STN LCD		Full-screen MVW				640 x 480	✓	✓	✓
		✓	✓	✓	✓	320 x 240	✓	✓	✓
Color TFT LCD	800 x 600	Full-screen MVW				800 x 600	✓	✓	
		✓	✓	✓		640 x 480	✓	✓	
		✓	✓	✓		320 x 240	✓	✓	
Color Dual-Scan STN LCD		Full-screen MVW				800 x 600	✓		
		✓	✓	✓		640 x 480	✓	✓	
		✓	✓	✓		320 x 240	✓	✓	
CRT Monitor	1024 x 768	Full-screen MVW				1024 x 768	✓		
		✓	✓			640 x 480	✓		
		✓	✓			320 x 240	✓		

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MVWs may use several aspect ratios, and they are not limited to a 4:3 aspect ratio. However, one MVW limitation is the amount of available display memory for MotionVideo™ Memory, as shown in the equation below.

MVWM = DMEM - GMEM - ACEL - 16 KBytes

Where:

- MVWM = MotionVideo window memory
- DMEM = Total available memory
- GMEM = Memory required for graphics
- ACEL = Memory required to support the half-frame accelerator required for dual-scan STN panels
- 16 KBytes = Memory reserved for hardware cursor and icon

MVA, which can be used in full-screen configurations, enables the creation of special graphics modes (such as, 24-bit/pixel with a 1X dot clock).

3.2.16.2 Hardware Zooming

As explained in Table 3–5, hardware zooming provides a programmable 2X magnification by doubling pixels either horizontally only, vertically only, or both horizontally and vertically simultaneously.

Table 3–5. Programming for Hardware Zoom

Type of MVW Hardware Zoom	CR3C
Horizontal pixel doubling	CR3C[7] = 1
Vertical pixel doubling	CR3C[6] = 1
Horizontal and vertical pixel doubling	CR3C[7] = 1, and CR3C[6] = 1

3.2.16.3 YUV to RGB Color Space Converter

The integrated YUV-to-RGB Color Space Converter supports two types of YUV-to-RGB algorithms, which are selected by register CR36[6]:

- Format 1 (Standard):
  - R = Y + 1.375V
  - G = Y - 0.375U - 0.75V
  - B = Y + 1.75U
- Format 2:
  - R = Y + V
  - G = Y - 0.25U - 0.5V
  - B = Y+ U

Register CR36[5] determines whether the YUV-to-RGB conversion uses the 2's complement U,V formats (which is useful for Philips SAA15B and SAA9051 TV decoders) or excess 128 format.

3.2.16.4 Video Playback

The MVA provides a MotionVideo Window, consisting of one of the color space formats in Section 3.2.16.1, on top of standard/extended VGA modes. The MotionVideo Window's pixel color depth may be different from the pixel color depth of the surrounding graphics. The internal color space converter may be used to expand 4:2:2 YUV data to 24-bit RGB.

For video playback, the hardware zoom feature may be used to double the MotionVideo Window horizontally, vertically, or both horizontally and vertically, or to fill the display's full resolution.

File Formats

The MVA may be used to accelerate the playback of files in a MotionVideo™ Window. The files would be stored in MotionVideo Memory in a 5-5-5 file format with 320 x 240 resolution.

If a data format is 4:2:2 YUV, then during display refresh, the internal color space converter converts the 4:2:2 format to 24-bit/pixel RGB.

If the display color resolution is less than 24 bits/pixel, the MVA dithering algorithm may be employed by programming registers CR4D and CR4E to increase the displayed pixel color depth to 24-bits/pixel, independently of the graphics color resolution.

By programming registers CR33 through CR39, the MotionVideo Window may be re-positioned anywhere on the display. By programming register CR3C, the 320 x 240 MotionVideo™ Window may

be expanded so that the 320 x 240 window may be doubled to 640 x 480 on 800 x 600 LCDs.

The pixel depth of the MotionVideo Window may be different from the pixel depth of the surrounding graphics.

Figure 3–9 shows a 320 x 240 video clip (5-5-5 RGB) that is displayed as a 640 x 480 15-bit/pixel MotionVideo Window on a 256-color 800 x 600 display, which can be accomplished using just one MByte of display memory.

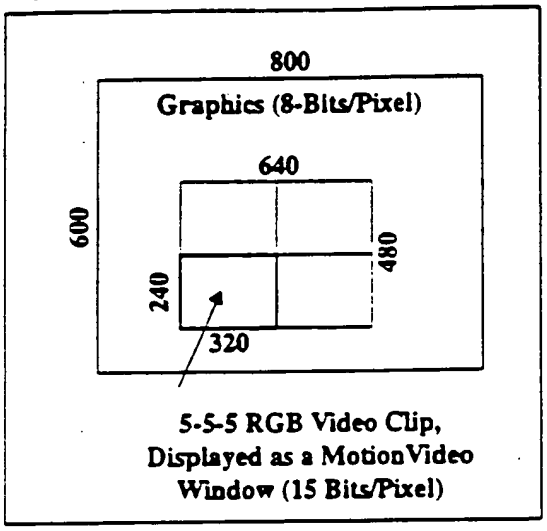


Figure 3–9. MotionVideo Window

3.2.17 Feature Connector

The CL-GD7542 provides the functionality of a standard VGA Feature Connector. The CL-GD7542's Feature Connector includes the following pins:

- FCP[7:0]: bi-directional 8-bit data port
- FCDCLK: dot clock output
- FCVCLK: video clock input
- FCESYNC#: enable syncs input, to enable the HSYNC, VSYNC, and FCBLANK# outputs
- FCBLANK#: either a blanking signal output, or an input that forces RGB outputs to zero current
- OVRW#: Overlay Window output

The CL-GD7542 supports the Feature Connector, such that video data may be input and displayed as an overlay video window. The Baseline Output Mode (8-bit indexed, one pixel per clock), is directly supported. The CL-GD7542 supports 8-bit/pixel indexed data (FC extended mode).

The 8-bit data is input either by using both phases of the clock or by using a 2X clock. An 8-bit value, stored in the Color Key Compare Register GRC, is compared to the video data input from FCP[7:0] on a pixel-by-pixel basis. A match will cause the pixel's graphics data to be replaced with the video data input.

3.2.18 NTSC/PAL Out

The CL-GD7542 outputs digital RGB data in an interlaced format to an external analog TV encoder, such as Analog Devices AD720 or Motorola MC1377. Only a minimum amount of additional logic circuitry is required. With the addition of an analog encoder, a portable computer can output the following signals, for use with a standard TV monitor or video cassette recorder (VCR):

- NTSC (National Television Standards Committee) signals
- PAL (phase-altering line) signals

The CL-GD7542 will operate in a locked interlaced mode and will use the LCD support shadowing mechanism (which shadows the Horizontal and Vertical CRTC registers) to prevent the application from changing the CRTC setup. Even the dot clock frequency will be locked. Horizontal and vertical display enable will be open to the application.

The NTSC/PAL output will operate in the standard VGA modes. The CL-GD7542 outputs analog RGB, composite sync signals, a NTSC/PAL standard select signal, and TV-On (a power management signal).

Due to TV image limitations, graphics mode 13 and text mode 0 provide the best display quality.

3.2.19 Half-Frame Accelerator

The CL-GD7542 integrates a Half-Frame Accelerator, required by dual-scan LCDs. With the Half-Frame Accelerator, a dual-scan LCD can run at a twice the CRT's refresh rate. The CL-GD7542 provides simultaneous CRT and LCD display operation (SimulScan™) for the following dual-scan LCDs:

- 640 x 480 STN/TFT dual-scan LCDs: the Half-Frame Accelerator provides all the standard VGA modes and extended video modes up to 640 x 480
- 800 x 600 STN/TFT dual-scan LCDs: the Half-Frame Accelerator provides all the standard VGA modes and extended video modes up to 800 x 600

3.2.20 LCD Interface

The CL-GD7542 directly interfaces with a variety of LCDs (and CRTs as well, for SimulSCAN operations). These LCDs include the following:

- Monochrome 640 x 480 dual-scan and single-scan STN LCDs
- Color 640 x 480 and 800 x 600 dual-scan and single-scan STN LCDs (with 8-bit and 16-bit interfaces)
- Color 640 x 480 and 800 x 600 TFT LCDs with the following interfaces:
  - 9-bit (3 bits each for Red, Green, Blue)
  - 12-bit (4 bits each for Red, Green, Blue)
  - 18-bit (6 bits each for Red, Green, Blue)
  - 24-bit (8 bits each for Red, Green, Blue)

3.2.21 LCD Resolution Compensation

With its LCD Resolution Compensation, the CL-GD7542 allows a spectrum of PC applications, originally written for analog CRT monitors that use various VGA modes, to run transparently on LCDs.

The LCD Resolution Compensation feature is necessary, in that unlike CRTs, LCDs have a fixed horizontal and vertical resolution. As a result, when a PC application is selected, VGA modes that are concurrently selected may use a resolution that is lower than the fixed resolution of the LCD. Consequently, unless LCD Resolution Compensation is used, a section of the LCD is left blank.

For example, when VGA text mode 3, which consists of 400 lines, is displayed on a 640 x 480 LCD that does not have use of LCD Resolution Compensation, 80 blank lines remain at the bottom of the LCD. (For a list of various horizontal and vertical resolutions for standard VGA modes, refer to Chapter 4.)

To remove blank space, the CL-GD7542 LCD Resolution Compensation presents these options:

- Automatic expansion of VGA text modes
- Custom fonts to replace standard VGA fonts
- Horizontal centering of displayed lines
- Horizontal expansion of VGA graphics modes
- Vertical centering of displayed lines
- Vertical expansion of VGA graphics modes

Resolution Compensation for 640 x 480 LCDs

For 640 x 480 LCDs, the CL-GD7542 provides the following LCD Resolution Compensation options to display lower-resolution VGA text and graphics:

- Auto-Text Expansion.
  Auto-Text Expansion of a VGA font makes the font consistent across the LCD and eliminates any breaks or artifacts in fonts that connect to adjacent fonts.
  - The 9-pixel-wide VGA fonts (used in the popular VGA text modes 3 and 7) are horizontally displayed as 8-pixel-wide-fonts. As a result, 80 characters fill all 640 pixels across.

  The following methods vertically expand VGA character fonts to 19 pixels. As a result, 475 lines of the LCD's 480 vertical lines are filled.

  - The 8 x 8 (200-line) VGA fonts are double-scanned, vertically expanding the font to equal 16 pixel lines. An extra top pixel line and two extra bottom pixel lines are added to each character row of the font, further vertically expanding the font to equal 19 pixel lines.
  - For 8 x 14 (350-line) VGA fonts, two extra top pixel lines and three extra bottom pixel lines

are added to each character row to vertically expand the font to 19 pixel lines.

- For the 8 x 16 (400-line) VGA fonts, an extra top pixel line and two extra bottom pixel lines are added to each character row to vertically expand the font to 19 pixel lines.

- Custom Fonts.
  Standard VGA fonts (8 x 8, 8 x 14, and 9 x 16) may be replaced with a custom 8 x 19 font to fill 640 x 475 pixels on a 640 x 480 LCD.

- Vertical Centering of Displayed Lines.
  - If Auto-Text Expansion or a custom font is used, the 475 lines that result can be vertically centered on the 480-line LCD.
  - If Auto-Text Expansion or a custom font is not used, 200-, 350-, or 400-line VGA text or graphics modes can also be vertically centered on the 480-line LCD.

- Vertical Graphics Expansion.
  On a 640 x 480 LCD, Vertical Graphics Expansion may be used to run PC application programs that use lower-resolution VGA graphics modes.
  - The 200-line VGA graphics modes are vertically expanded to 475 lines by expanding every 8 lines to 19 lines, using a pattern of 2,2,3,2,2,3,2,3 (double-scan and triple-scan).
  - The 350-line VGA graphics modes are vertically expanded to 475 lines by expanding every 14 lines to 19 lines using a pattern of 1,1,2,1,1,2,1,2,1,1,2,1,1,2 (single-scan and double-scan).

  Popular Graphics User Interface-based applications, such as Windows or OS/2, employ a CL-GD7542 driver that selects the proper VGA graphics mode (such as 2-, 16-, 256-, 32K-, 64K-, or 16.8M-color modes) to run application programs at the full resolution of the 640 x 480 LCD.

Resolution Compensation for 800 x 600 LCDs

For 800 x 600 LCDs, the CL-GD7542 provides the following LCD Resolution Compensation options to display lower-resolution VGA text and graphics:

- Auto-Text Expansion.
  Auto-Text Expansion of a VGA font makes the font consistent across the LCD and eliminates any breaks or artifacts in fonts that connect to adjacent fonts.
  - The 9-pixel-wide VGA fonts (used in the popular VGA text modes 3 and 7) are horizontally displayed as 10-pixel-wide fonts, by replicating the last pixel once. As a result, 80 characters fill all 800 pixels across.

  The following methods vertically expand the VGA character fonts.
  - The 8 x 8 (200-line) VGA fonts are triple-scanned, vertically expanding the font to equal 24 pixel lines. As a result, all of the LCD's 600 vertical lines are filled.
  - For the 8 x 14 (350-line) VGA fonts, every odd scanline is replicated to vertically expand the font to 21 lines. As a result, 525 lines of the LCD's 600 vertical lines are filled.
  - For the 8 x 16 (400-line) VGA fonts, every odd scanline is replicated to vertically expand the font to 24 lines. As a result, all of the LCD's 600 vertical lines are filled.

- Custom Fonts.
  Standard VGA fonts (8 x 8, 8 x 14, and 9 x 16) may be replaced with a custom 10 x 24 font to fill all 800 x 600 pixels on a 800 x 600 LCD.

- Horizontal Centering of Display Lines.
  - VGA text modes that are 720 pixels wide can be horizontally centered, leaving 40 blank pixels each on the left and right sides of the 800 x 600 LCD display.
  - VGA text modes that are 640 pixels wide can be horizontally centered, leaving 80 blank pixels each on the left and right sides of the 800 x 600 LCD display.

- Horizontal Graphics Expansion.
  VGA graphics modes that are 640 pixels wide can be horizontally expanded to 800 pixels by replicating every fourth pixel. (However, currently this expansion is not available for VGA graphics modes that have either 2X dot clocks with 16-bits/pixel or 3X dot clocks with 24-bits/pixel).
- Vertical Centering of Displayed Lines.
  - If Auto-Text Expansion or Vertical Graphics Expansion is used, the 525 lines that result can be vertically centered on the 600-line LCD.
  - If Auto-Text Expansion is not used, the 200-, 350-, or 400-line VGA text or graphics modes can also be vertically centered on the 600-line LCD.
- Vertical Graphics Expansion.
  On a 800 x 600 LCD, Vertical Graphics Expansion may be used to run PC application programs that use lower-resolution VGA graphics modes.
  - The 350-line VGA graphics modes are vertically expanded to 525 lines by replicating all odd scanlines.
  - The 400-line VGA graphics modes are vertically expanded to 600 lines by replicating all odd scanlines.
  - The 480-line VGA graphics modes are vertically expanded to 600 lines by replicating every fourth scanline.

  Popular Graphics User Interface-based applications, such as Windows or OS/2, employ a CL-GD7542 driver that selects the proper VGA graphics mode (such as 2-, 16-, 256-, 32K-, or 64K-color modes) to run the application programs at the full resolution of the 800 x 600 LCD.

3.2.22 Frame Rate Modulation

The CL-GD7542 employs a new, improved frame rate modulation (FRM) algorithm to create gray scales on monochrome and color STN LCDs. Over multiple frames in time, the FRM algorithm modulates the "on" and "off" times of individual pixels in the LCD, such that the eye integrates the superimposed pixels as perceptible gray scales.

Proprietary techniques reduce or eliminate entirely the gray scales' artifacts (for example, flicker, noise and pattern motion). On state-of-the-art STN LCDs with fast response times of approximately 100 ms, the result is an outstanding display quality.

The CL-GD7542 provides three FRM options:

- 16-frame FRM.
  This FRM option modulates the pixel over 16 frames in time to create 16 shades for each red, green, and blue (RGB) primary color, for 4,096 (16^3) colors total.

  This option is intended to support STN LCDs currently available and in development, including STN LCDs with very fast response times of approximately 100 ms. This algorithm allows masking of undesirable gray scales (that is, those that exhibit flicker or pattern motion).
  - By setting RBX[4], gray scales 7 and 9 can be converted to gray scales 6 and 8, respectively.
  - By setting RBX[3], gray scales 1 and 15 can be converted to gray scales 0 and 16, respectively.
  - If two gray scales are masked, the FRM algorithm produces 2,744 (14^3) colors.
  - If four gray scales are masked, the FRM algorithm produces 1,728 (12^3) colors.

- 8-frame FRM.
  This FRM option modulates the pixel over 8 frames in time to create 8 shades for each RGB primary color, for 512 (8^3) colors total.

  This option is intended to reduce flicker and "submarining" (that is, the temporary disappearance of the mouse pointer) on future STN LCDs that may have response times that are too fast for the 16-frame FRM option.

- 4-frame FRM.
  This FRM option modulates the pixel over 4 frames in time to create 4 shades for each RGB primary color, for 64 (4^3) colors total.

  This option is intended to reduce flicker and "submarining" (that is, the temporary disappearance of the mouse pointer) on future STN LCDs that may have response times too fast for both the 16- and 8-frame FRM options.

In summary, the FRM algorithm produces 2, 3, or 4 bits of color depth for each RGB primary color on STN LCDs.

- To add up to 6 bits of color depth to each primary color, the CL-GD7542's Dithering Engine may be used with an FRM algorithm.
- To add up to 8 bits of color depth to each primary color (or 256 gray scales for each primary color) for a total of 16.8M colors, the CL-GD7542's Dithering Engine may be used with only a 4-frame FRM algorithm.

3.2.23 Dithering Engine

The CL-GD7542's Dithering Engine increases the number of perceived colors displayed on the LCD and/or CRT, relative to what the display can physically produce without dithering.

A proprietary intercalating spatial dithering technique preserves the spatial resolution of the displayed image. For example, when a 640 x 480 resolution image is dithered, its resolution is maintained, instead of being reduced to 320 x 240.

The Dithering Engine works by automatically selecting a dithering pattern. As shown in Table 3–6, an increase in the dithering pattern increases the number of displayed bits per RGB primary color, depending upon the image's color depth.

Table 3–6. Effective Dithering Patterns

Effective Dithering Pattern	Increased Number of Displayed Bits per RGB Primary Color
2 x 1 Pattern	1 bit
2 x 2 Pattern	2 bits
4 x 2 Pattern	3 bits
4 x 4 Pattern	4 bits
8 x 4 Pattern	5 bits
8 x 8 Pattern	6 bits

The Dithering Engine may automatically add up to 6 bits per primary color, and it may be used for color and monochrome STN LCDs and TFT LCDs. (By programming register CR4C, this automatic feature may be overridden, and the number of bits per primary color limited to a programmable number.)

As shown in Figure 3–1 in Section 3.2, in the data path, the Dithering Engine is after the LCD Resolution Compensation, such that dithering is applied to the expanded image.

The Dithering Engine contains two separate dithering registers:

- Dithering register for standard/extended VGA modes
- Dithering register for MotionVideo™ Window

To render the appropriate colors, the CL-GD7542 dynamically switches dithering between surrounding graphics and the MotionVideo Window. (For more information on the MotionVideo™ Window, refer to Section 3.2.16.1.)

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Table 3–7 shows the number of gray scales that may be displayed on a monochrome STN LCD, by using a combination of the various FRM and dithering options.

As shown in the table, the 4-frame frame-rate-modulation option produces only four gray scales (2 bits/pixel), which are insufficient for displaying 32-, 64-, or 256-gray scale images.

The various dithering options may automatically add up to 6 bits/pixel depending upon the displayed image's color depth.

- To display a 32-gray-scale image (5 bits), the Dithering Engine automatically adds 3 bits to the 2 bits produced by FRM.
- To display a 64-gray-scale image (6 bits), the Dithering Engine automatically adds 4 bits to the 2 bits produced by the FRM.
- To display a 256-gray-scale image (8-bits), the Dithering Engine automatically adds 6 bits to the 2 bits produced by FRM.

Table 3–7. Number of Gray Scales On Mono STN LCDs

Frame-Rate-Modulation Option	Effective Dithering		Resulting Image on Mono STN LCD That Has:		
	Pattern	No. of Bits	32 Gray Scales (5 bits)	64 Gray Scales (6 bits)	256 Gray Scales (8 bits)
4 frames (2 bits)	None	0	4 (2^2)		
	2 x 1	1	8 (2^3)		
	2 x 2	2	16 (2^4)		
	4 x 2	3	32 (2^5)		
	4 x 4	4	32 (2^5)	64 (2^6)	
	8 x 4	5		64 (2^6)	128 (2^7)
	8 x 8	6			256 (2^8)
8 frames (3 bits)	None	0	8 (2^3)		
	2 x 1	1	16 (2^4)		
	2 x 2	2	32 (2^5)		
	4 x 2	3	32 (2^5)	64 (2^6)	
	4 x 4	4		64 (2^6)	128 (2^7)
	4 x 8	5			256 (2^8)
16 frames (4 bits)	None	0	16 (2^4)		
	2 x 1	1	32 (2^5)		
	2 x 2	2	32 (2^5)	64 (2^6)	
	4 x 2	3		64 (2^6)	128 (2^7)
	4 x 4	4			256 (2^8)

Table 3–8 shows the number of displayed colors on a color STN LCD, with various FRM and dithering options. As shown in Table 3–8, each FRM/dithering option produces the same number of color shades per primary color as gray scales for monochrome LCDs shown in Table 3–7.

Note that the total number of colors is equal to 3X the number of color per primary color RGB.

For example, a 4-frame FRM and 8 x 8 dithering pattern produces 2^8 (256) gray scales on monochrome STN LCDs and 2^{24} (16.8M colors) on color STN LCD.

Table 3–8. Number of Colors On Color STN LCDs

Primary Color RGB			Resulting Image on on Color STN LCD That Has:		
Frame-Rate-Modulation Option	Generated by LCD: Dithering Pattern	Generated by LCD: No. of Bits	32 colors (15 bits)	256K colors (18 bits)	16.8M colors (24 bits)
4 frames (2 bits)	None	0	64 (2^6)		
	2 x 1	1	512 (2^9)		
	2 x 2	2	4K (2^{12})		
	4 x 2	3	32K (2^{15})		
	4 x 4	4	32K (2^{15})	256K (2^{18})	
	8 x 4	5		256K (2^{18})	2M (2^{21})
	8 x 8	6			16.8M (2^{24})
8 frames (3 bits)	None	0	512 (2^9)		
	2 x 1	1	4K (2^{12})		
	2 x 2	2	32K (2^{15})		
	4 x 2	3	32K (2^{15})	256K (2^{18})	
	4 x 4	4		256K (2^{18})	2M (2^{21})
	4 x 8	5			16.8M (2^{24})
16 frames (4 bits)	None	0	4K (2^{12})		
	2 x 1	1	32K (2^{15})		
	2 x 2	2	32K (2^{15})	256K (2^{18})	
	4 x 2	3		256K (2^{18})	2M (2^{21})
	4 x 4	4			16.8M (2^{24})

Table 3–9 shows the number of colors various dithering patterns produce on 512-color TFT LCDs. If an image using the standard VGA 18-bit color palette is displayed on a 512-color TFT LCD (that is, which has only a 9-bit color palette), significant banding or contour lines are readily apparent.

Table 3–9. Number of Colors On 512-Color TFT LCDs

Primary Color RGB Generated by LCD		Resulting Image on Color TFT LCD That Has:		
Dithering Pattern	No. of Bits	32K colors (15 bits)	256K colors (18 bits)	16.8M colors (24 bits)
None	0	512 (2^9)		
2 x 1	1	4K (2^{12})		
2 x 2	2	32K (2^{15})	32K (2^{15})	
4 x 2	3		256K (2^{18})	256K (2^{18})
4 x 4	4			2M (2^{21})
8 x 4	5			16.8M (2^{24})

Consequently, the Dithering Engine automatically employs a 4 x 2 pattern to increase the number of displayed colors from the 3 bits per primary color that the LCD produces to the full 6 bits per primary color to meet the 18-bit VGA color palette requirement upon the displayed image's color depth.

- To display a 32-gray-scale image (5 bits), the Dithering Engine automatically adds 3 bits to the 2 bits produced by FRM.
- To display a 64-gray-scale image (6 bits), the Dithering Engine automatically adds 4 bits to the 2 bits produced by FRM.
- To display a 256-gray-scale image (8 bits), the Dithering Engine automatically adds 6 bits to the 2 bits produced by FRM.

The number of bits the Dithering Engine needs to add is reduced when either a 8-frame FRM or a 16-frame FRM is used.

Table 3–10 shows the number of colors various dithering patterns produce on 4K-color TFT LCDs.

Table 3–10. Number of Colors On 4K-Color TFT LCDs

Primary Color RGB Generated By LCD		Resulting Image on Color TFT LCD That Has:		
Dithering Pattern	No. of Bits	32K colors (15 bits)	256K colors (18 bits)	16.8M colors (24 bits)
None	0	4K (2^{12})		
2 x 1	1	32K (2^{15})		
2 x 2	2	32K (2^{15})	256K (2^{18})	
4 x 2	3		256K (2^{18})	2M (2^{21})
4 x 4	4			16.8M (2^{24})

Table 3–11 shows the number of colors that dithering patterns produce on 256K-color TFT LCDs.

Table 3–11. Number of Colors On 256K-Color TFT LCDs

Primary Color RGB		Resulting Image on Color TFT LCD That Has:		
Dithering Pattern	No. of Bits	32K colors (15 bits)	256K colors (18 bits)	16.8M colors (24 bits)
None	0	32K (2^{15})	256K (2^{18})	256K (2^{18})
2 x 1	1			2M (2^{21})
2 x 2	2			16.8M (2^{24})

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3.2.24 Frequency Synthesizer

The Frequency Synthesizer generates all clock frequencies for VGA and extended modes operation. Using a single reference frequency of 14.31818 MHz that is supplied from an external TTL-level source, the Frequency Synthesizer generates two fully programmable clocks – the memory clock (MCLK) and the video clock (VCLK).

Refer to Figure 3–10 for the Frequency Synthesizer Functional Diagram.

- MCLK
  - MCLK (the memory clock) generates all clocks needed for memory timing signals (for example, RAS*, CAS*, etc.).
  - MCLK must be optimized for the speed of the display memory used.
  - MCLK frequencies are programmed with SR1F.
  - For optimal selection of DRAM speeds, the CL-GD7542 supports MCLKs up to 45 MHz at 3.3V or 50 MHz at 5.0V.
- VCLK
  - VCLK (the video clock), is the fundamental video timing clock which generates all clocks needed for video display timing signals (for example, HSYNC and VSYNC) and for the pixel clock.
  - VCLK must be changed to support various display resolutions and refresh rates.
  - The VCLK frequencies are programmed with registers SRB through SRE and SR1B through SR1F.
  - The CL-GD7542 supports VCLKs up to 65 MHz at 3.3V or 80 MHz at 5.0V.

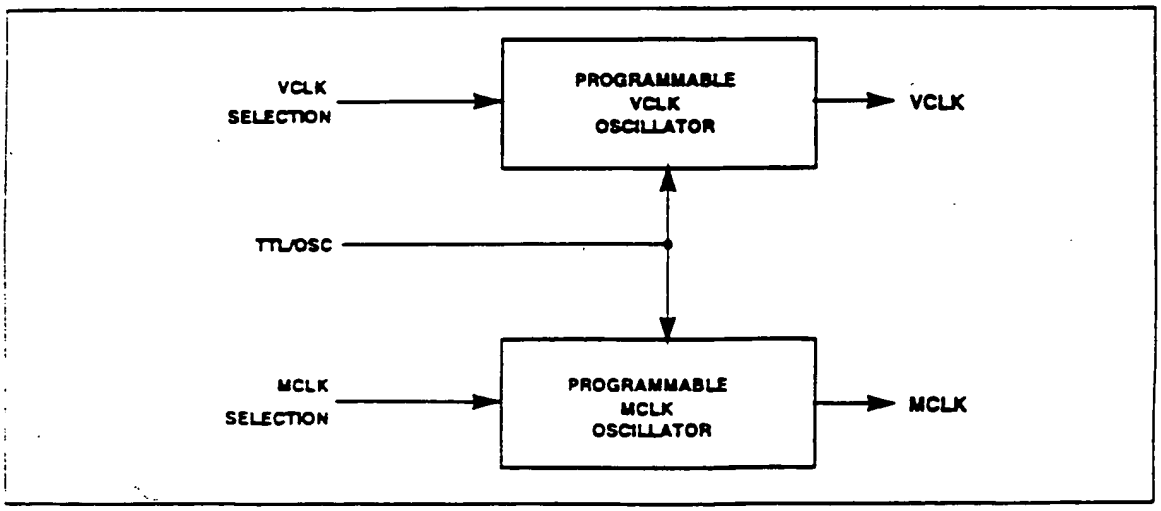


Figure 3–10. Programmable Dual-Frequency Synthesizer Functional Diagram

3.2.25 Power Management

The CL-GD7542 supports a variety of power management techniques to maximize battery life, including:

- LCD-only power savings.
  During LCD-only operations, the video DAC (including its monitor sense comparators) is powered down, and the video clock (VCLK) may be reduced to a level that still minimizes flicker.
- LCD power-up/down sequence control.
  To protect the LCD, the FPVEE and FPVCC output signals control the LCD's power-up and power-down sequence. [Damage can occur if VEE (the LCD's high-voltage power) is applied without VDD (the LCD's logic power)]. The FPBL output signal controls the LCD's backlight enable.
- Mixed-voltage interfaces.
  The host bus, display memory, LCD, and CRT interfaces can each be implemented at either 3.3V or 5V. The voltages used for each interface may be mixed in any combination.
- Standby Mode.
  This mode reduces power consumption by turning off the display while allowing application programs to continue to run normally in the background.

  Standby is entered via the Standby pin, by using the internal Standby Counter, or by programming a register.

  During Standby, using the proper power sequencing, the LCD and CRT are turned off, the video clock (VCLK) is stopped, and the video DAC is powered down. The CPU can still access and modify the display memory and palette.

  The Standby Mode is exited as it is entered, via the Standby pin, by using the internal Standby Counter, or by programming a register.
- Suspend Mode.
  This mode reduces power consumption when the system remains inactive for a relatively long period of time, while maintaining the contents of the controller's registers, palette, and display memory. Unlike Standby mode, however, during the Suspend Mode, applications are suspended and do not continue to run normally in the background.

  Hardware-controlled Suspend is entered via the Suspend Pin. Software-controlled Suspend is entered by setting register CR20[3].

  In contrast to Hardware-controlled Suspend, Software-controlled Suspend allows the CPU to access the internal registers, which requires an active clock and I/O capability, and therefore, more power.

  During Hardware-controlled Suspend, the display is turned off, the video (VCLK) and memory (MCLK) clocks are both stopped, and CPU accesses to the display memory, palette, and I/O registers cease.

  The controller configures display memory for self-refresh or uses the 32-kHz clock for memory refresh.

  Hardware-controlled Suspend is exited via the Suspend Pin. When Suspend Mode is exited, any application programs that were previously running can be quickly re-started from the point at which they suspended.
- VESA Display Power Management.
  The CL-GD7542 supports the VESA Display Power Management Specification for CRT power management to allow systems to comply with the U.S. Environmental Protection Agency's Energy Star Computer qualifications.

For more information, refer to Appendix A9. "Power-Management Solutions".

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3.3 Performance

The CL-GD7542 is designed with the following performance-enhancing features:

- BitBLT Engine.
  The BitBLT Engine is used to accelerate Graphics User Interfaces (GUIs), such as Microsoft Windows.
- Bus Interface Choices.
  The CL-GD7542 provides a choice of bus interfaces for optimum performance:
  - 32-bit VESA VL-Bus
  - '486 local-bus interface
  - PCI bus interface
- CPU Interfaces to I/O registers and memory.
  For increased performance, the CL-GD7542 supports the following CPU interfaces:
  - 32-bit CPU interface to display memory, for faster CPU host access to memory for all modes, including planar modes
  - 16-bit CPU interface to I/O Registers, for faster CPU host access to the registers
- Extended-Write Modes.
  - For faster CPU write performance, the extended-write modes can be used on 8 pixels at a time in 8- or 16-bit/pixel graphics modes that have packed-pixel addressing.
  - These write modes can be used for faster text writing, pattern filling, and block-moving operations in graphics modes.

  For more information, refer to Appendix A4 "Color Expansion and Extended-Write Modes".
- Hardware Cursor.
  GUI performance can be improved by using either the 32 x 32 or the 64 x 64 Hardware Cursor.
- Memory Data Fast Access.
  For faster access to display memory, the CL-GD7542 supports the following:
  - a 32-bit display memory data bus.
  - DRAM Fast-page Mode operations
- Video FIFO.
  Video FIFO minimizes memory contention.
- Zero-wait-state performance.
  For faster CPU access for writes to display memory, the CL-GD7542 provides zero-wait-state performance and a CPU Write Buffer.

3.4 RAMDAC Operation

3.4.1 Writing to the Color Lookup Table

To write a color definition to the Lookup Table, a value specifying an address location in the Lookup Table is first written to the Write Mode Address Register. The color values for the Red, Green, and Blue intensities are then written in succession to the Color Value Register. After the Blue data bits are latched, the new color data bits are then written into the Lookup Table at the defined address, and the CL-GD7542 automatically increments the Address Register.

Since the CL-GD7542 increments the Address Register after each transfer of data to the Lookup Table, it is best to write a set of consecutive locations at once. The start address of the set of locations is first written to the Write Mode Address Register. The color data bits for each address location are then sequentially written to the Color Value Register. After each CPU host transfer of three bytes of color data, the CL-GD7542 automatically writes data to the Lookup Table and increments the Address Register.

3.4.2 Reading from the Color Lookup Table

To read color data from the Lookup Table, a value specifying the address location of the data is written to the Read Mode Address Register. After the address is latched, the data bits from this location are automatically read out to the Color Value Register, and the CL-GD7542 automatically increments the Address Register.

The color intensity values are then read from the Color Value Register by a sequence of three read (RD*) commands. After the Blue value is transferred out, new data bits are read from the Lookup Table's current address to the Color Value Register, which causes the CL-GD7542 to automatically increment the Address Register again.

If the CL-GD7542 loads the Address Register with a new starting address while an unfinished sequence is in progress, the system resets and starts a new sequence. This action occurs for both read and write operations.

3.5 Programmable Core Voltage

To optimize graphics performance and power consumption, the CL-GD7542 supports selective switching of the core VDD between 3.3V and 5V, based upon the video mode that is being used.

3.5.1 3.3V Core Voltage

When the CL-GD7542 is operating at 3.3V, the CL-GD7542's memory clock operates up to 45 MHz, which is sufficient for the following pixel modes:

- 1024 x 768 4-bit/pixel
- 800 x 600 8-bit/pixel
- 640 x 480 16-bit/pixel

The core VDD and Analog VDDs must always be at the same voltage.

3.5.2 5.0V Core Voltage

When the CL-GD7542 is operating at 5.0V, the CL-GD7542's memory clock should be at 50 MHz to maximize performance in the following pixel modes:

- 1024 x 768 8-bit/pixel
- 800 x 600 16-bit/pixel
- 640 x 480 24-bit/pixel modes

The core VDD and Analog VDDs (which must always be at the same voltage) should be 5V with a 50 MHz memory clock.

3.6 Compatibility

The CL-GD7542 includes all registers and data paths required for standard VGA controllers. It also supports the following extended VGA modes:

- 1024 x 768 with 256 colors (interlaced and non-interlaced modes)
- 1280 x 1024 with 256 colors (interlaced modes)

Additionally, various 132-column text modes are supported.

3.7 Extension Registers

While expanding or centering VGA modes on 640 x 480 or 800 x 600 LCDs, the appropriate VGA registers are shadowed, for VGA compatibility.

3.8 Testability

The CL-GD7542 chip is testable by using Pin-Scan Testing and a Signal Generator.

Pin-scan testing tests the signal state of every pin on the chip. Any pins that are not connected to the board, or which are shorted to a neighboring pin or trace will be detected. For more information, refer to Appendix A11, "Pin-Scan Testing."

The Signature Generator allows the entire system, including display memory, to be tested at speed. For more information, refer to Appendix A10, "Signature Generator".

3.9 Configuration Inputs

To configure the chip for operation, the CL-GD7542 uses a combination of hardware and software configurations.

3.9.1 Hardware Configuration Inputs

Pull-up resistors are used on some of the memory data pins, which are read during the low-to-high transition of the Reset# pulse or when the External Pull-Up Reset register SR24[3] is toggled.

- 32-bit PCI Bus.
  This configuration selects the 32-bit PCI bus with Min-grant timing of 8 PCI CLKs (-250 ns at 33 MHz).
- 32-bit PCI Bus with Min-Grant Extended.
  This configuration selects the 32-bit PCI bus, but with Min-grant timing extended from 8 PCI CLKs (-250 ns at 33 MHz) to 16 PCI CLKs (-500 ns at 33MHz), allowing burst write mode capability.
- Enable Feature Connector.
  This configuration uses the appropriate pins for the Feature Connector video port. (Refer to Pin Descriptions in Chapter 1. and Chapter 2. for the affected pins).

- Sleep Address Select.
  This configuration selects either I/O address 46E8h or 3C3h (the default) as the sleep address.
- VESA VL-Bus with 50-MHz MCLK.
  This configuration sets the VL-Bus for >33 MHz local bus operation.

If no resistors are present, the above pins are read as low because of the internal pull-down resistors. The status of these inputs is stored in registers SR22 and SR24.

Three hardware switch inputs (SW[2:0]) are read during each horizontal retrace period. These inputs are used by the BIOS to monitor external activities that can affect the chip operation. The status of these three inputs is stored in SR24[2:0].

3.9.2 Software Configuration Inputs

A software programmable register, SR23, is used to select the desired function of some multi-function pins as defined below:

- ACTI / FCEVIDEO# / SBYI Select.
  Registers SR23[6] and SR24[7] configure the ACTI / FCEVIDEO# / SBYI input (pin 86) as either the Activity Sense input or the hardware-controlled Standby input.
- BLI / SUSPI Enable.
  Registers SR23[5] and SR24[7] configure the BLI / SUSPI input (pin 87) as either the Hardware-Controlled Suspend input or the Backlight Input control.
- FCDCLK Output Select.
  Register SR24[4] is used to output either the VCLK or PCLK0 on the FCDCLK pin.
- FCVCLK Enable.
  Register SR23[7] selects whether FCVCLK is sent to the DAC only or is also used for VCLK generation.
- VCLK Output Enable.
  Registers SR23[4] and SR24[7] either make the VCLK output pin low or output the internal VCLK on the FCDCLK / VCLK output (pin 103).

For more configuration information, refer to Appendix A14, "Configuration Notes" and Section 2.7.

3.10 Software Support

The CL-GD7542 supports big-endian word swapping, which allows it to load either x86 little-endian data or PowerPC big-endian data into display memory, depending upon the application requirements.

A VGA BIOS, which is fully compatible with the standard IBM VGA BIOS and the Interrupt 10h video service functions, is available from Cirrus Logic and third-party BIOS vendors.

The Cirrus Logic CL-GD7542 VGA BIOS is a high-quality, feature-rich firmware product designed to take maximum advantage of the CL-GD7542 controller, especially in the areas of display quality, power management, and graphics performance. The key features of the VGA BIOS are:

- Super VGA-compatible BIOS
- Supports SimulSCAN operation (simultaneous LCD and CRT display)
- Supports the power-management modes
- Supports display-enhancement features
- Can be integrated with the system BIOS
- Supports switchless configuration
- Can be customized without source code through use of utility programs such as OEMSI
- Provides VESA-compatible modes and 1.2-function support for Video BIOS Extensions (VBE)
- Supports multiple monitor refresh rates

The CL-GD7542 VGA controller and BIOS can be implemented as an adapter board or placed directly on the system board. The VESA local bus BIOS can be located at C000h or E000h. There is a separate BIOS for PCI bus implementations.

The core BIOS requires 32 KBytes. Extra functionality, such as EGA-compatible fonts, can be located in a 16-KByte optional BIOS. This optional BIOS may be either appended to the core BIOS (for VL-bus or PCI bus implementations) or loaded into the same segment as the core BIOS (for VL-bus implementations). For system implementations which do not have ROM space for the 16-KByte optional BIOS, a TSR is provided to support the extra functionality in DOS environments.

3.10.1 Software Support for OEMs

Cirrus Logic provides the following CL-GD7542 software utilities for OEM development use:

- CL_STEST.
  This utility is a DOS-based screen-testing utility that provides for the following:
  - CL_STEST enables the user to display and adjust the position and RGB color of a variety of patterns (including color bars, lines and rectangles) to test the display's quality.
  - CL_STEST may operate with pixel resolutions of:
    - 640 x 400
    - 640 x 480
    - 800 x 600
    - 1024 x 768
- CLPanel.
  This utility is a DOS-based LCD-parameter optimization utility that provides for the following:
  - Via a serial link to an external monitor, CLPanel enables a variety of LCD parameters to be adjusted.
  - CLPanel may be used to view a variety of display test images and bit-map (BMP) images.
  - CLPanel may be used to switch the active display between LCD, CRT, or SimulScan modes.
- CLRegs.
  This utility is a DOS-based VGA-controller register viewer/editor utility that provides for the following:
  - CLRegs enables users to easily view and edit the CL-GD7542's standard VGA and extension registers and color palette.
  - The CLRegs Help screen provides a brief explanation of each bit in each register.
  - CLRegs enables register values to be changed by typing in a new hex value or toggling individual bits.
  - CLRegs also displays a variety of the CL-GD7542's configuration data, including the status of the CRT Controller, the graphics mode being used, information about the video BIOS, and hardware cursor information.
- CLView.
  This utility is a DOS-based image-viewing utility that provides for the following:
  - CLView loads the following types of image files: BMP, Graphics Interchange Format (GIF), TGA, or PCX.
  - The CLView's full-screen menu lists all current BMP, GIF, TGA, or PCX image files.
  - By pressing a CLView function key, each image's width, height, bits per pixels, number of colors, and file size can be displayed.
  - CLView allows image files to be marked for inclusion in a slide show.
  - CLView may be used to switch the active display between LCD, CRT, or SimulScan modes.
- OEMSI.
  This utility is a Cirrus Logic BIOS-customization utility for OEM development use.

3.10.2 Software Support for End Users

Cirrus Logic provides the following CL-GD7542 software utilities for distribution to end users:

- CL_Mode.
  CL_Mode is a DOS-based graphics-mode utility and display-configuration utility.
  - CL_Mode's user-friendly VGA Configuration menu enables users to turn "on" and "off" a variety of graphics configuration options, including the following:
    - automatic text expansion
    - bold fonts
    - power-management options
    - reverse video
    - shading of graphics and text
    - text enhancement
    - vertical position of display
  - CL_Mode's Monitor Type Setup menu enables users to set CRT monitor resolution and refresh rate.
  - CL_Mode's Video Modes Preview menu en-

ables users to display the various VGA modes.
  - New settings of the above options enabled by the user can be updated in the AUTOEXEC.BAT file by this program.
- CLVESA.
  This utility is a Terminate-and-Stay-Resident (TSR) utility that supports the VESA BIOS extensions.
- CSwitcher.
  This utility is a video-configuration TSR.
- SETRES.
  This utility is a Windows application for defining the resolution and bit depth of the CL-GD7542 Windows Driver.
  - SETRES enables users to set the CRT resolution to: 640 x 480, 800 x 600, 1024 x 768, or 1280 x 1024
  - SETRES enables users to select bit depth used on either the CRT or LCD, such as: 16, 256, 64K, or 16.8M.
  - SETRES enables users to turn the Hardware Cursor "on" and "off".
  - SETRES enables users to make the font size normal or large.
- WinMode.
  This utility is a Windows application for video-mode configurations.
- WinPanel.
  This utility is very similar in operation to CL_MODE, and performs the same basic functions in the Windows environment.
  - WinPanel enables users to turn "on" and "off" a variety of graphics configuration options, including:
    - automatic text expansion
    - bold fonts
    - power-management options (such as the timer intervals for Standby mode or backlight)
    - reverse video
    - shading of graphics and text
    - text enhancement
    - vertical position of display
  - WinPanel allows users to select between LCD, CRT, or SimulScan display options.
  - WinPanel allows users to set high-refresh rates for CRT monitors.
  - New settings of the above options enabled by the user can be updated in the AUTOEXEC.BAT file by this program.

3.11 Package

The CL-GD7542 is available in a standard EIAJ 208-pin QFP package with a 28 x 28 mm body size and 0.5 mm lead pitch.

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4. CL-GD7542 Video Mode Tables

This chapter lists tables for configuring the CL-GD7542 for various CRT and flat-panel video modes. For detailed information on specific LCD flat panels that the CL-GD7542 can drive, refer to the CL-GD7542 *Panel Interface Guide* for details.

NOTE: The parameters detailed in the tables of Chapter 4 define standard capabilities of the CL-GD7542 when it is used with the Cirrus Logic Video BIOS. Consult with the appropriate BIOS vendor for information about the modes and parameters supported by those video BIOSes that are not from Cirrus Logic.

4.1 Video Modes: CRT-Only

This section lists IBM Standard VGA and Cirrus Logic Extended CRT-only video modes.

4.1.1 IBM® Standard VGA CRT-Only Video Modes

The IBM® Standard VGA video BIOS supports the CRT-only video modes listed in Table 4–1.

Table 4–1. IBM® Standard VGA CRT-Only Video Modes

Mode Number (hex)	Number of Colors	Characters x Rows	Character Cell (pixels)	Screen Format (pixels)	Display Mode	Video Clock (MHz)	Horizontal Freq. (kHz)	Vertical Frequency (Hz)	Minimum MCLK (MHz)
0, 1	16/256K	40 x 25	9 x 16	360 x 400	Text	28	31.5	70	36
2, 3	16/256K	80 x 25	9 x 16	720 x 400	Text	28	31.5	70	36
4, 5	4/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70	36
6	2/256K	80 x 25	8 x 8	640 x 200	Graphics	25	31.5	70	36
7	Mono.	80 x 25	9 x 16	720 x 400	Text	28	31.5	70	36
D	16/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70	36
E	16/256K	80 x 25	8 x 8	640 x 200	Graphics	25	31.5	70	36
F	Mono.	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70	36
10	16/256K	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70	36
11	2/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	36
12	16/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	36
12[a]	16/256K	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	72	36
13	256/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70	36

a Modes denoted by (a) are IBM® Standard VGA modes that have been enhanced by Cirrus Logic for a higher vertical frequency.

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4.1.2 Cirrus Logic Extended CRT-Only Video Modes

The Cirrus Logic video BIOS supports the extended CRT-only video modes listed in Table 4–2. (Columns one and two compare the hex number of the Cirrus Logic extended CRT-only video mode with the hex number of the equivalent VESA CRT-only video mode.)

- If the BIOS used is not the Cirrus Logic BIOS, modes may differ.
- Some video modes are not supported by all monitors.
- For the monitor type that is selected, the best-quality vertical refresh rate will be used automatically.

Table 4–2. Cirrus Logic Extended CRT-Only Video Modes

Mode No. (hex)	VESA No. (hex)	Number of Colors	Characters x Rows	Chara. Cell (pixels)	Screen Format (pixels)	Display Mode	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	Min. MCLK (MHz)[g]
11[a]	–	2/256	80 x 30	6 x 16	640 x 480	Graphics	31.5	37.9	75[a]	36
12[a]	–	16/256	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	75[a]	36
tbd[b]	–	16/256	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	36
16[b]	–	16/256	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	75	36
14	–	16/256K	132 x 25	8 x 16	1056 x 400	Text	41.5	31.5	70	45
54	10A	16/256K	132 x 43	8 x 8	1056 x 350	Text	41.5	31.5	70	45
55	109	16/256K	132 x 25	8 x 14	1056 x 350	Text	41.5	31.5	70	45
58, 6A[c]	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	36	35.2	56	40
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.8	60	40
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	50	48.1	72	45
tbd[b]	–	16/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.8	60	40
17[b]	–	16/256K	100 x 37	8 x 16	800 x 600	Graphics	50	48.1	75	45
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	36	35.2	56	40
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.9	60	45
5C[a]	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	50[a]	48.1	72	40
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60	45
5D[c]	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	44.9	35.5	87[c]	40
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	75	56	70	50
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	77	58	75	50
tbd[b]	–	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60	45
18[b]	–	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	77	58	75	50
5E	100	256/256K	80 x 25	8 x 16	640 x 400	Graphics	25	31.5	70	36
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	36
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	72	36
60[b]	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	44.9	35.5	87[c]	40
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60	45
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	75	56	70	50

Table 4–2. Cirrus Logic Extended CRT-Only Video Modes (Continued)

Mode No. (hex)	VESA No. (hex)	Number of Colors	Characters x Rows	Chars. Cell (pixels)	Screen Format (pixels)	Display Mode	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	Min. MCLK (MHz)[g]
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	77	58	75	50
64	111	64K	–	–	640 x 480	Graphics	25	31.5	60	45
64	111	64K	–	–	640 x 480	Graphics	31.5	37.9	75	45
65	114	64K	–	–	800 x 600	Graphics	36	35.2	56	50
65	114	64K	–	–	800 x 600	Graphics	40	37.8	60	45
66[e]	110	32K[e]	–	–	640 x 480	Graphics	25	31.5	60	45
66[e]	110	32K[e]	–	–	640 x 480	Graphics	31.5	37.9	75	45
67[e]	113	32K[e]	–	–	800 x 600	Graphics	36	31.5	56	50
6C[c]	106	16/256K	160 x 64	8 x 16	1280 x 1024	Graphics	75	48	87[c]	50
6C[c]	–	256/256K	160 x 64	8 x 16	1280 x 1024	Graphics	75	48	87[c]	50
71	112	16M	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60	50
74[c]	–	64K	–	–	1024 x 768	Graphics	44.9	35.5	87[c]	45
tbd[f]	–	16/256	80 x 25	8 x 8	640 x 200	Text	13.5	tbd	tbd	45
tbd[f]	–	16/256	80 x 30	8 x 16	640 x 480	Graphics	13.5	tbd	tbd	45
tbd[f]	–	256/256K	80 x 30	8 x 16	640 x 480	Graphics	13.5	tbd	tbd	45

a. Modes denoted by (a) are IBM® Standard VGA modes that have been enhanced by Cirrus Logic for a higher vertical frequency.

b. Modes denoted by (b) are 4-bit-per-pixel packed-pixel modes.

c. All modes with (Vertical Frequency = 87 Hz) are interlaced modes.

d. Application programs should use mode 6A, rather than mode 58, to retain compatibility with other VGA BIOS products.

e. Modes denoted by (e) are true-color packed-pixel mode.

f. Modes denoted by (f) are interlaced modes for NTSC-OUT functions.

g. The value of the minimum MCLK frequency defined in this column defines the lowest clock frequency at which the controller may be run without any adverse effects to the function of the controller. Better benchmark performance may be achieved with an MCLK frequency other than the frequency specified in this column.

h. These modes are NOT available when the controller is operated with a core VDD of 3.3VDC. For the full operational range of the clocks at 3.3VDC, refer to Chapter 7, for the electrical specification section of this document.

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4.2 Video Modes: LCD Only

This section lists IBM Standard VGA and Cirrus Logic Extended LCD-only video modes.

4.2.1 IBM® Standard VGA LCD-Only Video Modes

The IBM® Standard VGA BIOS supports the LCD-only video modes listed in Table 4–3.

Table 4–3. IBM® Standard VGA LCD-Only Video Modes

Mode No. (hex)	Mono. STN No. of Shades	Color STN No. of Colors	Color TFT No. of Colors	Characters x Rows	Character Cell (pixels)	Screen Format (pixels)	Display Mode	Expanded Panel (pixels)
0, 1	16/16	16/256K	16/256K	40 x 25	8 x 16	360 x 400	Text	640 x 475
2, 3	16/16	16/256K	16/256K	80 x 25	8 x 16	720 x 400	Text	36
4, 5	4/64	4/256K	4/256K	40 x 25	8 x 8	320 x 200	Graphics	36
6	2/16	2/256K	2/256K	80 x 25	8 x 8	640 x 200	Graphics	36
7	2/16	Mono.	Mono.	80 x 25	8 x 16	720 x 400	Text	36
D	16/64	16/256K	16/256K	40 x 25	8 x 8	320 x 200	Graphics	36
E	16/16	16/256K	16/256K	80 x 25	8 x 8	640 x 200	Graphics	36
F	2/16	Mono.	Mono.	80 x 25	8 x 14	640 x 350	Graphics	36
10	16/16	16/256K	16/256K	80 x 25	8 x 14	640 x 350	Graphics	36
11	2/16	2/256K	2/256K	80 x 30	8 x 16	640 x 480	Graphics	640 x 480
12	16/16	16/256K	16/256K	80 x 30	8 x 16	640 x 480	Graphics	640 x 480
13	64/256K	256/256K	256/256K	40 x 25	8 x 8	320 x 200	Graphics	640 x 475

4.2.2 Cirrus Logic Extended LCD-Only Video Modes

The extended LCD-only video modes listed in Table 4–4 are supported by the Cirrus Logic video BIOS. (Columns one and two compare the hex number of the Cirrus Logic extended LCD-only video mode with the hex number of the equivalent VESA LCD-only video mode.)

- If the BIOS used is not the Cirrus Logic BIOS, modes may differ.
- Some video modes are not supported by all monitors.
- For the monitor type that is selected, the best-quality vertical refresh rate will be used automatically.

Table 4–4. Cirrus Logic Extended LCD-Only Video Modes

Mode No. (hex)	VESA No. (hex)	Number of Colors	Characters x Rows	Chara. Cell (pixels)	Screen Format (pixels)	Graphics Panel Type	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	Min. MCLK (MHz)[d]
16[a]	–	16/256K	80 x 30	8 x 16	640 x 480	STN/TFT	31.5	tbd	tbd	36
58, 6A[b]	102	16/256K	100 x 37	8 x 16	800 x 600	STN/TFT	40	tbd	tbd	40
17	–	16/256K	100 x 37	8 x 16	800 x 600	STN/TFT	50	tbd	tbd	45
5C	103	256/256K	100 x 37	8 x 16	800 x 600	STN/TFT	40	tbd	tbd	40
5E	100	256/256K	80 x 25	8 x 16	640 x 400	STN/TFT	25	tbd	tbd	36
5F	101	256/256K	80 x 30	8 x 16	640 x 480	STN/TFT	31.5	tbd	tbd	36
64	111	64K	–	–	640 x 480	TFT	25	tbd	tbd	50
65	114	64K	–	–	800 x 600	TFT	36	tbd	tbd	50
66[c]	110	32K[c]	–	–	640 x 480	TFT	25	tbd	tbd	50
67[c]	113	32K[c]	–	–	800 x 600	TFT	36	tbd	tbd	50
71	112	16M	80 x 30	8 x 16	640 x 480	TFT	25	tbd	tbd	50

a. Modes denoted by (a) are 4-bit-per-pixel packed-pixel modes.

b. Application programs should use mode 6A, rather than mode 58, to retain compatibility with other VGA BIOS products.

c. Modes denoted by (c) are true-color packed-pixel mode.

d. The value of the minimum MCLK frequency defined in this column defines the lowest clock frequency at which the controller may be run without any adverse effects to the function of the controller. Better benchmark performance may be achieved with an MCLK frequency other than the frequency specified in this column.

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4.3 Video Modes: SimulSCAN

This section lists IBM Standard VGA and Cirrus Logic Extended SimulSCAN video modes.

4.3.1 IBM® Standard VGA SimulSCAN Video Modes

The IBM® Standard VGA video BIOS supports the SimulSCAN video modes listed in Table 4–5.

Table 4–5. IBM® Standard VGA SimulSCAN Video Modes

Mode No. (hex)	Mono. STN No. of Shades	Color STN No. of Colors	Color TFT No. of Colors	Characters x Rows	Character Cell (pixels)	Screen Format (pixels)	Display Mode	Expanded Panel (pixels)
0, 1	16/16	16/256K	16/256K	40 x 25	8 x 16	360 x 400	Text	640 x 475
2, 3	16/16	16/256K	16/256K	80 x 25	8 x 16	720 x 400	Text	640 x 475
4, 5	4/64	4/256K	4/256K	40 x 25	8 x 8	320 x 200	Graphics	640 x 475
6	2/16	2/256K	2/256K	80 x 25	8 x 8	640 x 200	Graphics	640 x 475
7	2/16	Mono.	Mono.	80 x 25	8 x 16	720 x 400	Text	640 x 475
D	16/64	16/256K	16/256K	40 x 25	8 x 8	320 x 200	Graphics	640 x 475
E	16/16	16/256K	16/256K	80 x 25	8 x 8	640 x 200	Graphics	640 x 475
F	2/16	Mono.	Mono.	80 x 25	8 x 14	640 x 350	Graphics	640 x 475
10	16/16	16/256K	16/256K	80 x 25	8 x 14	640 x 350	Graphics	640 x 475
11	2/16	2/256K	2/256K	80 x 30	8 x 16	640 x 480	Graphics	640 x 480
12	16/16	16/256K	16/256K	80 x 30	8 x 16	640 x 480	Graphics	640 x 480
13	64/256K	256/256K	256/256K	40 x 25	8 x 8	320 x 200	Graphics	640 x 480

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4.3.2 Cirrus Logic Extended SimulSCAN Video Modes

The extended SimulSCAN video modes listed in Table 4–6 are supported by the Cirrus Logic video BIOS. (Columns one and two compare the hex number of the Cirrus Logic extended SimulSCAN video mode with the hex number of the equivalent VESA SimulSCAN video mode.)

- If the BIOS used is not the Cirrus Logic BIOS, modes may differ.
- Some video modes are not supported by all monitors.
- For the monitor type that is selected, the best-quality vertical refresh rate will be used automatically.

Table 4–6. Cirrus Logic Extended SimulSCAN Video Modes

Mode No. (hex)	VESA No. (hex)	Number of Colors	Characters x Rows	Chara. Cell (pixels)	Screen Format (pixels)	Graphics Panel Type	Video Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	Min. MCLK (MHz)[e]
16[a]	–	16/256K	80 x 30	8 x 16	640 x 480	STN/TFT	25	tbd	tbd	40
58, 6A[b]	102	16/256K	100 x 37	8 x 16	800 x 600	STN/TFT	40	tbd	tbd	45
17	–	16/256K	100 x 37	8 x 16	800 x 600	STN/TFT	40	tbd	tbd	45
5C	103	256/256K	100 x 37	8 x 16	800 x 600	STN/TFT	40	tbd	tbd	45
5E	100	256/256K	80 x 25	8 x 16	640 x 400	STN/TFT	25	tbd	tbd	40
5F	101	256/256K	80 x 30	8 x 16	640 x 480	STN/TFT	25	tbd	tbd	45
64	111	64K	–	–	640 x 480	TFT	25	tbd	tbd	50
65[d]	114	64K	–	–	800 x 600	TFT	36	tbd	tbd	50[d]
66[c]	110	32K[c]	–	–	640 x 480	TFT	25	tbd	tbd	50
67[c,d]	113	32K[c]	–	–	800 x 600	TFT	36	tbd	tbd	50[d]
71[d]	112	16M	80 x 30	8 x 16	640 x 480	TFT	25[f]	tbd	tbd	50[d]

a. Modes denoted by (a) are 4-bit-per-pixel packed-pixel modes.

b. Application programs should use mode 6A, rather than mode 58, to retain compatibility with other VGA BIOS products.

c. Modes denoted by (c) are true-color packed-pixel mode.

d. Modes denoted by (d) indicate that dual-scan color LCDs do not support SimulSCAN on these modes.

e. The value of the minimum MCLK frequency defined in this column defines the lowest clock frequency at which the controller may be run without any adverse effects to the function of the controller. Better benchmark performance may be achieved with an MCLK frequency other than the frequency specified in this column.

f. These modes are NOT available when the controller is operated with a core VDD of 3.3VDC. For the full operational range of the clocks at 3.3VDC, refer to the Electrical Specification section of this document.

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5. VGA Register Port Map

Table 5–1. VGA Register Port Map

Address	Port	Port Type
94	POS 102 Access Control (3C3 Sleep)	
102	POS 102 Register	
3B4	CRT Controller Index — Monochrome	Read/Write
3B5	CRT Controller Data — Monochrome	Read/Write
3BA	Feature Control — Monochrome	Write
	Input Status Register 1 — Monochrome	Read
3C0	Attribute Controller Index / Data	Write
3C1	Attribute Controller Index / Data	Read
3C2	Miscellaneous Output	Write
	Input Status Register 0	Read
3C3	Motherboard Sleep	Read/Write
3C4	Sequencer Index	Read/Write
3C5	Sequencer Data	Read/Write
3C6	Video DAC Pixel Mask (R/W), Hidden DAC Register	Read/Write
3C7	Pixel Address Read mode	Write
	DAC State	Read
3C8	Pixel Mask Write Mode	Read/Write
3C9	Pixel Data	Read/Write
3CA	Feature Control Readback	Read
3CC	Miscellaneous Output Readback	Read
3CE	Graphics Controller Index	Read/Write
3CF	Graphics Controller Data	Read/Write
3D4	CRT Controller Index — Color	Read/Write
3D5	CRT Controller Data — Color	Read/Write
3DA	Feature Control — Color	Write
	Input Status Register 1 — Color	Read
46E8	Adapter Sleep	Read/Write

6. CL-GD7542 Registers

6.1 Register Summary

6.1.1 Introduction to Registers

The registers in this chapter include standard VGA registers, as well as extension registers added by Cirrus Logic.

6.1.2 Summary of External/General Registers in Section 6.2

The External and General Registers in the CL-GD7542 are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
MISC	Miscellaneous Output Register	–	3C2 (Write)	103
MISC	Miscellaneous Output Register	–	3CC (Read)	103
FC	Feature Control Register	–	3?A (Write)	106
FC	Feature Control Register	–	3CA (Read)	106
FEAT	Input Status Register 0	–	3C2	107
STAT	Input Status Register 1	–	3?A	108
3C3	Sleep-Mode Register	–	3C3	112
3C6	Pixel Mask Register	–	3C6	110
3C7	Pixel Address Read Mode Register	–	3C7 (Write)	111
3C7	DAC State Register	–	3C7 (Read)	112
3C8	Pixel Address Write Mode Register	–	3C8	113
3C9	Pixel Data Register	–	3C9	114
PCI00	PCI Device/Vendor ID Register	–	00	115
PCI04	PCI Command Register	–	04	116
PCI04	PCI Status Register	–	04	117
PCI10	PCI Base Address Register	–	10	118
PCI3C	PCI Interrupt Line and Interrupt Pin Register	–	3C	119
46E8	Alternate Sleep-Mode Register	–	46E8	112

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

6.1.3 Summary of Sequencer Registers in Section 6.3

The CL-GD7542 Sequencer Registers are summarized in the following table. Note that there are Extension Registers that are accessed using the Sequencer Ports.

Abbreviation	Register Name	Index	Port	Page
SRX	Sequencer Index Register	–	3C4	123
SR0	Reset Register	0	3C5	125
SR1	Clocking Mode Register	1	3C5	126
SR2	Plane Mask Register	2	3C5	128
SR3	Character Map Select Register	3	3C5	129
SR4	Memory Mode Register	4	3C5	131

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6.1.4 Summary of CRT Controller Registers in Section 6.4

The CL-GD7542 VGA CRT Controller Registers are summarized in the following table. Note that there are Extension Registers that are accessed using the VGA CRT Controller Ports.

Abbreviation	Register Name	Index	Port	Page
CRX	CRTC Index Register	–	3?4	135
CR0	Horizontal Total Register	0	3?5	136
CR1	Horizontal Display End Register	1	3?5	139
CR2	Horizontal Blanking Start Register	2	3?5	140
CR3	Horizontal Blanking End Register	3	3?5	141
CR4	Horizontal Sync Start Register	4	3?5	143
CR5	Horizontal Sync End Register	5	3?5	144
CR6	Vertical Total Register	6	3?5	146
CR7	Overflow Register	7	3?5	147
CR8	Screen A Preset Row Scan Register	8	3?5	148
CR9	Character Cell Height Register	9	3?5	149
CRA	Text Cursor Start Register	A	3?5	150
CRB	Text Cursor End Register	B	3?5	151
CRC	Screen A Start Address High Register	C	3?5	152
CRD	Screen A Start Address Low Register	D	3?5	153
CRE	Text Cursor Location High Register	E	3?5	154
CRF	Text Cursor Location Low Register	F	3?5	155
CR10	Vertical Sync Start Register	10	3?5	156
CR11	Vertical Sync End Register	11	3?5	157
CR12	Vertical Display End Register	12	3?5	159
CR13	Offset Register	13	3?5	160
CR14	Underline Row Scanline Register	14	3?5	161
CR15	Vertical Blanking Start Register	15	3?5	162
CR16	Vertical Blanking End Register	16	3?5	163
CR17	Mode Control Register	17	3?5	164
CR18	Line Compare Register	18	3?5	166
CR22	Graphics Data Latches Read-back Register	22	3?5	167
CR24	Attribute Controller Toggle Read-back Register	24	3?5	168
CR26	Attribute Controller Index Read-back Register	26	3?5	169

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

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6.1.5 Summary of Graphics Controller Registers in Section 6.5

The CL-GD7542 Graphics Controller Registers are summarized in the following table. Note that there are Extension Registers that are accessed using the Graphics Controller Port.

Abbreviation	Register Name	Index	Port	Page
GRX	Graphics Controller Index Register	–	3CE	173
GR0	Set/Reset Register	0	3CF	174
GR1	Set/Reset Enable Register	1	3CF	175
GR2	Color Compare Register	2	3CF	176
GR3	Data Rotate Register	3	3CF	177
GR4	Read Map Select Register	4	3CF	178
GR5	Mode Register	5	3CF	179
GR6	Miscellaneous Register	6	3CF	183
GR7	Color Don't Care Register	7	3CF	184
GR8	Bit Mask Register	8	3CF	185

6.1.6 Summary of Attribute Controller Registers in Section 6.6

The CL-GD7542 Attribute Controller Registers are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
ARX	Attribute Controller Index Register	–	3C0/3C1	189
AR0-ARF	Attribute Controller Palette Registers	0:F	3C0/3C1	190
AR10	Attribute Controller Mode Register	10	3C0/3C1	191
AR11	Overscan (Border) Color Register	11	3C0/3C1	193
AR12	Color Plane Enable Register	12	3C0/3C1	194
AR13	Pixel Panning Register	13	3C0/3C1	196
AR14	Color Select Register	14	3C0/3C1	197

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6.1.7 Summary of Extension Registers in Section 6.7

The CL-GD7542 Extension Registers are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
SR6	Unlock All Extensions Register	6	3C5	201
SR7	Extended Sequencer Mode Register	7	3C5	202
SR8	Miscellaneous Control Register	8	3C5	205
SR9	Scratch-Pad 0 Register	9	3C5	206
SRA	Scratch-Pad 1 Register	A	3C5	206
SRB	VCLK0 Numerator Register	B	3C5	207
SRC	VCLK1 Numerator Register	C	3C5	207
SRD	VCLK2 Numerator Register	D	3C5	207
SRE	VCLK3 Numerator Register	E	3C5	207
SRF	DRAM Control Register	F	3C5	209
SR10	Graphics Cursor and Icon Horizontal Position Register	10	3C5	211
SR11	Graphics Cursor and Icon Vertical Position Register	11	3C5	213
SR12	Video Data Path Control Register	12	3C5	214
SR13	Graphics Cursor Pattern Address Offset Register	13	3C5	217
SR14	Scratch-Pad 2 Register	14	3C5	218
SR15	Scratch-Pad 3 Register	15	3C5	218
SR16	Performance Tuning Register	16	3C5	219
SR18	Signature Generator Control Register	18	3C5	221
SR19	Signature Generator Result Low Byte Register	19	3C5	223
SR1A	Signature Generator Result High Byte Register	1A	3C5	224
SR1B	VCLK0 Denominator and Post-Scalar Value Register	1B	3C5	225
SR1C	VCLK1 Denominator and Post-Scalar Value Register	1C	3C5	225
SR1D	VCLK2 Denominator and Post-Scalar Value Register	1D	3C5	225
SR1E	VCLK3 Denominator and Post-Scalar Value Register	1E	3C5	225
SR1F	MCLK Frequency and VCLK Source Select Register	1F	3C5	226
SR20	Miscellaneous Control Register	20	3C5	227
SR21	Dual-scan Color Control Register	21	3C5	228
SR22	Hardware Configuration Register	22	3C5	229
SR23	Software Configuration #1 Register	23	3C5	231
SR24	LCD Type Switch and FC Enable Register	24	3C5	233
SR25	Timer-Software Reset and Hardware Configuration Register	25	3C5	235
SR26	Shader Signature — Least-Significant Byte	26	3C5	237
SR27	Shader Signature — Most-Significant Byte	27	3C5	238
SR2A	Hardware Icon #0 Control	2A	3C5	239
SR2B	Hardware Icon #1 Control	2B	3C5	240
SR2C	Hardware Icon #2 and Miscellaneous PCI Control	2C	3C5	242
SR2D	Hardware Icon #3 and HIMEM Select Control	2D	3C5	247
SR2E	Graphics-Cursor Horizontal-Position Extension	2E	3C5	245
SR2F	Half-Frame-Accelerator Threshold	2F	3C5	247

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6.1.7 Summary of Extension Registers in Section 6.7 (cont.)

The CL-GD7542 Extension Registers are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
	Graphic-Controller Extension Registers			
GR9	Offset Register 0	9	3CF	248
GRA	Offset Register 1	A	3CF	250
GRB	Graphics Controller Mode Extensions Register	B	3CF	251
GRC	Color Key Compare Register	C	3CF	253
GRD	Color Key Compare Mask Register	D	3CF	254
GRE	PCI-Burst and Green-PC Control Register	E	3CF	256
GR10	16-bit Pixel Background Color High Byte Register	10	3CF	257
GR11	16-bit Pixel Foreground Color High Byte Register	11	3CF	258
GR20	BLT Width Low Register	20	3CF	259
GR21	BLT Width High Register	21	3CF	260
GR22	BLT Height Low Register	22	3CF	261
GR23	BLT Height High Register	23	3CF	262
GR24	BLT Destination Pitch Low Register	24	3CF	263
GR25	BLT Destination Pitch High Register	25	3CF	264
GR26	BLT Source Pitch Low Register	26	3CF	265
GR27	BLT Source Pitch High Register	27	3CF	266
GR28	BLT Destination Start Low Register	28	3CF	267
GR29	BLT Destination Start Mid Register	29	3CF	268
GR2A	BLT Destination Start High Register	2A	3CF	269
GR2C	BLT Source Start Low Register	2C	3CF	270
GR2D	BLT Source Start Mid Register	2D	3CF	271
GR2E	BLT Source Start High Register	2E	3CF	272
GR30	BLT Mode Register	30	3CF	273
GR31	BLT Start/Status Register	31	3CF	276
GR32	BLT Raster Operation Register	32	3CF	277
GR34	BLT Transparent Color Select Low Register	34	3CF	278
GR35	BLT Transparent Color Select High Register	35	3CF	279
GR38	BLT Source Transparent Color Mask Low Register	38	3CF	315
GR39	BLT Source Transparent Color Mask High Register	39	3CF	281

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6.1.7 Summary of Extension Registers in Section 6.7 (cont.)

Abbreviation	Register Name	Index	Port	Page
	Control Extension Registers			
CR19	Interlace End	19	3?5	282
CR1A	Miscellaneous Control	1A	3?5	283
CR1B	Extended Display Controls	1B	3?5	285
CR1D	Overlay Mode Controls	1D	3?5	287
CR1E	LCDShading	1E	3?5	288
CR1F	LCD Modulation Control	1F	3?5	290
CR20	Power Management	20	3?5	292
CR21	Power-down Timers	21	3?5	294
CR23	FPVCC, FPBL, SUSPEND-Debounce Control	23	3?5	296
CR25	MFG Revision Register	25	3?5	298
CR27	ID Register	27	3?5	307
CR29	CL-GD7542 Configuration Status	29	3?5	308
CR2C	LCD Interface	2C	3?5	301
CR2D	LCD Display Control	2D	3?5	304
CR2E	High-resolution LCD Control	2E	3?5	306
CR2F	Drivers and BIOS Revision Register	2F	3?5	307
CR30	TV-OUT Control	30	3?5	308
	MotionVideo™ Window (MVW) Control Registers			
CR33	MVW Horizontal XS and XW Overflow	33	3?5	310
CR34	MVW Horizontal-Start XS	34	3?5	308
CR35	MVW Horizontal-Width XW	35	3?5	312
CR36	MVW Vertical-Position High and YUV to RGB Convert	36	3?5	313
CR37	MVW Vertical Position Start YS	37	3?5	314
CR38	MVW Vertical Position End YE	38	3?5	315
CR39	MVW Surrounding Address Offset	39	3?5	316
CR3A	MVW Memory-Address Start	3A	3?5	317
CR3B	MVW Memory-Address Offset	3B	3?5	318
CR3C	MVW Zoom, Enable and Encoding Format	3C	3?5	319
CR3D	MVW Horizontal Size	3D	3?5	320

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

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6.1.7 Summary of Extension Registers in Section 6.7 (cont.)

Abbreviation	Register Name	Index	Port	Page
	LCD Horizontal-Timing Control Registers			
CR40	LCD Horizontal-Display-Enable Start – No Centering	40	3?5	321
CR41	LCD HDE Start Register to Center 720 Dots	41	3?5	323
CR42	LCD HDE Start Register to Center 640 Dots	42	3?5	324
CR43	LCD Dot-Clock Skew-Control	43	3?5	325
CR44	LCD Horizontal-Width	44	3?5	327
CR47	TFT Horizontal Position	47	3?5	324
CR48	TFT-HSYNC and LCD-Height Overflow	48	3?5	324
CR49	Vertical Size for Upper-half of Dual-scan STN LCDs	49	3?5	324
CR4A	Vertical Size for LCD LCDs	4A	3?5	324
CR4B	Reserved for Scratch Pad	4B	3?5	324
CR4C	Input-Resolution Override for Dithering	4C	3?5	324
CR4D	Output Resolution for Dithering	4D	3?5	324
CR4E	MVA Input-Resolution Override for Dithering	4E	3?5	337
HDR	Hidden DAC Register	–	3C6	339
	LCD Timing Registers			
R2X	LFS Vertical Counter Value Compare (not centered)	2	3?5	343
R3X	LFS Vertical Counter Value Compare (centered)	3	3?5	345
R4X	LFS Vertical Counter Value Compare (centered)	4	3?5	346
R5X	LFS Vertical Counter Value Compare (centered)	5	3?5	347
R6X	Overflow (msb) Bits for LFS Signal Compare	6	3?5	348
R7X	LCD Signal Control for Color TFT LCDs	7	3?5	350
R8X	STN Color LCD Data Format	8	3?5	351
R9X	TFT LCD Data Format	9	3?5	352
RBX	Shade Conversion and Extra Line Clock Insert	B	3?5	357
RCX	LFS Vertical Position for 600-Line Modes	C	3?5	354
RDX	LCD Timing – LFS Vertical Position #6	D	3?5	347
REX	Overflow Bits for RCX and RDX	E	3?5	357
	Horizontal-Timing Shadow Registers			
R0Y	Horizontal Timing Shadow Register	0	3?5	357
R2Y	Horizontal Timing Shadow Register	2	3?5	357
R3Y	Horizontal Timing Shadow Register	3	3?5	357
R4Y	Horizontal Timing Shadow Register	4	3?5	357
R5Y	Horizontal Timing Shadow Register	5	3?5	357
R0Z	Horizontal Timing Shadow Register	0	3?5	357
R2Z	Horizontal Timing Shadow Register	2	3?5	357
R3Z	Horizontal Timing Shadow Register	3	3?5	357
R4Z	Horizontal Timing Shadow Register	4	3?5	357
R5Z	Horizontal Timing Shadow Register	5	3?5	357

NOTES: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.
The RnX register are indexed through settings of CR2D.
The R0Y–R5Y registers and the R0Z–R5Z registers are indexed through settings of CR2C.

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6.2 External /General Registers

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6.2.1 MISC: Miscellaneous Output Register

I/O Port Address: 3C2 (Write) 3CC (Read)

Index: –

Bit	Description	Reset State
7	Vertical Sync Polarity	0
6	Horizontal Sync Polarity	0
5	Page Select	0
4	Reserved	
3	Clock Select [1]	0
2	Clock Select [0]	0
1	Enable Display Memory	0
0	CRTC I/O Address	0

This standard VGA register has an assortment of bits that have nothing in common.

Bit 7 — Vertical Sync Polarity:
When this bit is programmed to:
- 0, Vertical Sync is normally low, and a high indicates beginning sync time.
- 1, Vertical Sync is normally high, and a low indicates beginning sync time.

Bit 6 — Horizontal Sync Polarity:
- When this bit is programmed to:
  - — 0, Horizontal Sync is normally low. A high indicates beginning sync time.
  - — 1, Horizontal Sync is normally high. A low indicates beginning sync time.
- For some monitors, the combined polarity of Vertical and Horizontal Sync is used to indicate the number of scanlines per frame, as shown in the table.
- When Extension Register CR20[5] = 1 and MISC[7:6] = 00, the value of MISC[7:6] is redefined from Reserved to an 800 x 600 LCD.

MISC		Vertical Size	Vertical Overscan	Vertical Total =
[7] Vertical Sync Polarity	[6] Horizontal Sync Polarity	(Scanlines appearing on screen)	(Scanlines appearing off screen)	(Vertical Size + Vertical Overscan)
0 (+)	0 (+)	Reserved	Reserved	Reserved
0 (+)	1 (–)	400	14	414
1 (–)	0 (+)	350	12	362
1 (–)	1 (–)	480	16	496

Continued on next page.

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6.2.1 MISC: Miscellaneous Output Register *(cont.)*

Bit — **Description**

5 — **Page Select:**
When SR4[2] (the odd/even bit of the Sequencer Memory Mode Register) is 1, MISC[5] affects how display memory addresses are selected.
- When SR4[2] = 1, and this bit = 0, only odd memory locations are selected.
- When SR4[2] = 1, and this bit = 1, only even memory locations are selected.
- This bit takes effect for video modes 6, D, E, 11, and 12.
- This bit is ignored if either of the following are true:
  - — Graphics Controller Register GR6[1] = 1.
  - — Sequencer Register SR4[3] = 1.

4 — **Reserved**

3:2 — **Clock Select:**
As shown in the following table, this field is used with Sequencer Register bits and Extension Register bits to choose a clock source for the CL-GD7542.

SR22 [3]	SR23 [7]	MISC [3]	MISC [2]	SR1F [6]	SR1E [0]	Clock Source to CL-GD7542
0	0	0	0	0	X	SR08 (N) / SR1B (D) [a]
0[b]	X	X	X	0	X	OSC if TV-Out Enabled
X	X	X	X	1	0	MCLK
X	X	X	X	1	1	MCLK ÷ 2 [c]
0	0	0	1	0	X	SR0C (N) / SR1C (D) [a]
0	0	1	0	0	X	SR0D (N) / SR1D (D) [a]
0	0	1	1	0	X	SR0E (N) / SR1E (D) [a]
0	1	0	X	0	X	FCVCLK to only DAC
0	1	1	X	0	X	FCVCLK to both DAC and CRTC
1	1	0	X	0	X	OSC (Pin)

[a] These are Numerator/Denominator Registers. For information on programming alternative frequencies, refer to Appendix A7.
[b] True only if CR30[3] =1 and SR25[4] = 1.
[c] True only if SR12[4] = 1.

1 — **Enable Display Memory:**
When this bit is programmed to:
- 0, the CL-GD7542 will not respond to any accesses to display memory.
- 1, the CL-GD7542 will respond normally to accesses to display memory.

Continued on next page.

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6.2.1 MISC: Miscellaneous Output Register *(cont.)*

Bit	Description
0	**CRTC I/O Address:** This bit selects either Monochrome or Color I/O addresses.

MISC[0]	Mode	Input Status / Feature Control	CRTC Index	CRTC Data
0	Monochrome	3BA	3B4	3B5
1	Color	3DA	3D4	3D5

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6.2.2 FC: Feature Control Register

I/O Port Address: 3?A (Write) 3CA (Read)

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	CRT VSYNC Control	0
2	Reserved	
1	Reserved	
0	Reserved	

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is one of the original IBM PC registers. Nearly all the bits are no longer used.

Bit	Description
7:4	Reserved
3	**CRT VSYNC Control:** This bit is normally used for CRTs that have a internal vertical display enable signal pin. Program this bit: • to 0 to keep the CRT VSYNC signal unchanged and to maintain IBM compatibility. • to 1 to logically OR the CRT VSYNC signal with the CL-GD7542 internal vertical display enable signal prior to going to the VSYNC pin.
2:0	Reserved

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6.2.3 FEAT: Input Status Register 0

I/O Port Address: 3C2

Index: –

Bit	Description	Reset State
7	Vertical Interrupt Request Pending	0
6	Reserved	
5	Reserved	
4	DAC Switch Sensing	0
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

The bits in this read-only register are nearly all undefined.

Bit	Description
7	**Vertical Interrupt Request Pending:** When this bit: • = 1, there is a vertical interrupt request pending. • = 0, there is no vertical interrupt request pending. For more information on the CL-GD7542 vertical interrupt system, refer to CRT Controller Register CR11.
5	Reserved
4	**DAC Switch Sensing:** This read-only bit is used to report the on-off status of one of four analog comparator RAMDAC sense switches, as selected by MISC[3:2]. This bit: • = 1 when the selected DAC sense switch is on. • = 0 when the selected DAC sense switch is off.
3:0	Reserved

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6.2.4 STAT: Input Status Register 1

I/O Port Address: 3?A

Index: –

Bit	Description	Reset State
7	Peserved	
6	Reserved	
5	Diagnostic [1]	0
4	Diagnostic [0]	0
3	Vertical Retrace	0
2	Reserved	
1	Reserved	
0	Video Display Enable	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register contains some status bits.

Bit 7:6 — Reserved

Bit 5:4 — Diagnostic [1:0]:
For diagnostic purposes, these bits indicate the state of two of the eight outputs of the Attribute Controller Register AR12[5:4], as indicated in the following table:

AR12		STAT	
[5]	[4]	[5]	[4]
0	0	FP[2] Red	FP[0] Blue
0	1	FP[3] Secondary Blue	FP[1] Green
1	0	FP[5] Secondary Red	FP[4] Secondary Green
1	1	FP[7]	FP[6]

If the Attribute Controller Register AR12[3:2] or Extension Register CR1A[3:2] set the FP[7:0] bits to act as inputs, the STAT[5:4] bits can reflect the input data on FP[7:0].

Bit 3 — Vertical Retrace:
A 1 on this bit indicates that vertical retrace is in progress.

Bit 2:1 — Reserved

Bit 0 — Video Display Enable:
When this bit:

- = 0, video data bits are being serialized and displayed.
- = 1, vertical or horizontal blanking is active.

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6.2.5 3C3 Sleep Mode Register

I/O Port Address: 3C3

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Sleep Mode Readback	1
0	Sleep Mode Write / Readback	1

The CL-GD7542 may be put into the sleep mode in one of several ways.

1. Sleep Mode Method 1:
   This 3C3 Sleep Mode Register is normally recommended for motherboard applications.
2. Sleep Mode Method 2:
   When the S46 / MD[21] pin has an external pull-up resistor attached, the alternate Sleep Mode Register, 46E8, is selected. (The 3C3 Sleep Mode Register is then inactive.)
3. Sleep Mode Method 3:
   The sleep mode may also be activated when the SLEEP# input pin is low.

Bit	Description
7:2	Reserved
1	**Sleep Mode Readback** This bit is read-only. When 3C3[0]: • = 1, this bit is also 1. • = 0, this bit is also 0.
0	**Sleep Mode Write / Readback:** This read/write bit is normally 1. When this bit: • = 1, the CL-GD7542 is active and can respond to normal bus and display activity. • = 0, the CL-GD7542 turns off the interface to the display memory, the interface to the CPU I/O, and the displays. • is cleared to 0, no other chip accesses, except those to 3C3, are allowed until this bit is set to a 1.

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6.2.6 3C6 Pixel Mask Register

I/O Port Address: 3C6

Index: –

Bit	Description	Reset State
7	Pixel Mask Register Bit [7]	0
6	Pixel Mask Register Bit [6]	0
5	Pixel Mask Register Bit [5]	0
4	Pixel Mask Register Bit [4]	0
3	Pixel Mask Register Bit [3]	0
2	Pixel Mask Register Bit [2]	0
1	Pixel Mask Register Bit [1]	0
0	Pixel Mask Register Bit [0]	0

The bits in this read-only register form the Pixel Mask for the Palette DAC. Typically, the Cirrus Logic BIOS programs all these bits to 1. This same 3C6 address is used to access the Hidden DAC Register, described in this manual's Extension Registers (Section 6.7).

Bit	Description
7:0	**Pixel Mask [7:0]:** This field is the Pixel Mask for the Palette DAC. When a bit in this field is programmed to 0, the corresponding bit in the pixel data is ignored in looking up an entry in the Color Lookup Table.

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6.2.7 3C7: Pixel Address Read Mode Register (Write Only)

I/O Port Address: 3C7

Index: –

Bit	Description	Reset State
7	Pixel Address Bit (Read Mode) [7]	0
6	Pixel Address Bit (Read Mode) [6]	0
5	Pixel Address Bit (Read Mode) [5]	0
4	Pixel Address Bit (Read Mode) [4]	0
3	Pixel Address Bit (Read Mode) [3]	0
2	Pixel Address Bit (Read Mode) [2]	0
1	Pixel Address Bit (Read Mode) [1]	0
0	Pixel Address Bit (Read Mode) [0]	0

The bits in this write-only register form the Pixel Address (Read Mode) for the Palette DAC. This Pixel Address is then used to specify the Color Lookup Table entry that is to be read.

Bit	Description
7:0	**Pixel Address (Read Mode) [7:0]:** This field is the Pixel Address (Read Mode) for an entry in the Color Lookup Table. At the conclusion of every third read of the Pixel Data Register (3C9), this address is incremented by one.

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6.2.8 3C7: DAC State Register (Read Only)

I/O Port Address: 3C7

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	DAC State [1]	0
0	DAC State [0]	0

The bits in this read-only register indicate whether a read or a write to the Color Lookup Table occurred last.

Bit	Description
7:2	Reserved
1:0	**DAC State [1:0]:** This two-bit field indicates which pixel address register was accessed last. • Both bits in this field will always be the same digit. • When the bits: — are 00, a write operation is in progress, meaning that the last accessed register for the Color Lookup Table was the Pixel Address Write Register. — are 11, a read operation is in progress, meaning that the last accessed register for the Color Lookup Table was the Pixel Address Read Register.

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6.2.9 3C8: Pixel Address Write Mode Register

I/O Port Address: 3C8

Index: –

Bit	Description	Reset State
7	Pixel Address Bit (Write Mode) [7]	0
6	Pixel Address Bit (Write Mode) [6]	0
5	Pixel Address Bit (Write Mode) [5]	0
4	Pixel Address Bit (Write Mode) [4]	0
3	Pixel Address Bit (Write Mode) [3]	0
2	Pixel Address Bit (Write Mode) [2]	0
1	Pixel Address Bit (Write Mode) [1]	0
0	Pixel Address Bit (Write Mode) [0]	0

The bits in this registers form the Pixel Address (Write Mode) for the Palette DAC. This Pixel Address is then used to specify the Color Lookup Table entry that is to be written.

Bit	Description
7:0	**Pixel Address (Write Mode) [7:0]:** This field is the Pixel Address (Write Mode) for an entry in the Color Lookup Table. At the conclusion of every third write to the Pixel Data Register (3C9), this address is incremented by one.

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6.2.10 3C9: Pixel Data Register

I/O Port Address: 3C9

Index: –

Bit	Description	Reset State
7	Pixel Data Register Bit [7]	0
6	Pixel Data Register Bit [6]	0
5	Pixel Data Register Bit [5]	0
4	Pixel Data Register Bit [4]	0
3	Pixel Data Register Bit [3]	0
2	Pixel Data Register Bit [2]	0
1	Pixel Data Register Bit [1]	0
0	Pixel Data Register Bit [0]	0

This register contains the Pixel Data for the palette DAC.

Bit	Description
7:0	**Pixel Data [7:0]:** These read/write register bits store the Pixel Data for the Palette DAC. Writing to this register. • Prior to writing to this register, register 3C8 (the Pixel Address Write Mode Register) is written with the first or only pixel address. • Three values, corresponding to the Red, Green, and Blue values for the pixel, are then written to this address. • Following the third write, values are transferred to the Color Lookup Table. • The Pixel Address is incremented, in case new values for the next pixel address are to be written. Reading from this register. • Prior to reading from this register, register 3C7 (the Pixel Address Read Mode Register) is written with the first or only pixel address. • Three values, corresponding to the Red, Green, and Blue values for the pixel, are then read from this address. • Following the third read, the Pixel Address is incremented, in case new values for the next pixel address are to be read.

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6.2.11 PCI00: PCI Device ID / PCI Vendor ID Register

PCI Configuration Address: 00 Index: –

Bit	Description	Reset State
31	PCI Device ID [15]	0
30	PCI Device ID [14]	0
29	PCI Device ID [13]	0
28	PCI Device ID [12]	1
27	PCI Device ID [11]	0
26	PCI Device ID [10]	0
25	PCI Device ID [9]	1
24	PCI Device ID [8]	0
23	PCI Device ID [7]	0
22	PCI Device ID [6]	0
21	PCI Device ID [5]	0
20	PCI Device ID [4]	0
19	PCI Device ID [3]	0
18	PCI Device ID [2]	0
17	PCI Device ID [1]	0
16	PCI Device ID [0]	0
15	PCI Vendor ID [15]	0
14	PCI Vendor ID [14]	0
13	PCI Vendor ID [13]	0
12	PCI Vendor ID [12]	1
11	PCI Vendor ID [11]	0
10	PCI Vendor ID [10]	0
9	PCI Vendor ID [9]	0
8	PCI Vendor ID [8]	0
7	PCI Vendor ID [7]	0
6	PCI Vendor ID [6]	0
5	PCI Vendor ID [5]	0
4	PCI Vendor ID [4]	1
3	PCI Vendor ID [3]	0
2	PCI Vendor ID [2]	0
1	PCI Vendor ID [1]	1
0	PCI Vendor ID [0]	1

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This register is accessible and effective only if the CL-GD7542 is configured for PCI bus. It contains the PCI Device ID and the PCI Vendor ID required for PCI compliance.

Bit	Description
31:16	**PCI Device ID [15:0]:** When the CL-GD7542 is configured for PCI bus, this read-only field returns 1200 hex, the PCI device ID assigned to the CL-GD7542 by Cirrus Logic, Inc.
15:0	**PCI Vendor ID [15:0]:** When the CL-GD7542 is configured for PCI bus, this read-only field returns 1013 hex, the PCI vendor ID assigned to Cirrus Logic, Inc. by the PCI Special Interest Group.

6.2.12 PCI04: PCI Command Register

PCI Configuration Address: 04 Index: –

Bit	Description	Reset State
15	Reserved	
14	Reserved	
13	Reserved	
12	Reserved	
11	Reserved	
10	Reserved	
9	Reserved	
8	Reserved	
7	Reserved	
6	Reserved	
5	Enable PCI DAC Shadowing	0
4	Reserved	
3	Reserved	
2	Reserved	
1	Enable Memory Accesses	0
0	Enable I/O Accesses	0

This 16-bit register is accessible and effective only if the CL-GD7542 is configured for PCI Bus. It consists of the least-significant two bytes of the PCI Status / PCI Command Register.

Bit	Description
15:6	Reserved: These bits are reserved and must be programmed to a 0.
5:	**Enable PCI DAC Shadowing:** When the CL-GD7542 is configured for PCI Bus and this bit is programmed to a 1: • PCI DAC shadowing is enabled. • Read accesses are executed normally. • Write accesses to the CL-GD7542 are executed, in that data bits are latched in the appropriate Palette Register. However, the CL-GD7542 will not acknowledge the access.
4:2	Reserved: These bits are reserved and must be programmed to a 0.
1	**Enable Memory Accesses:** When the CL-GD7542 is configured for PCI Bus and this bit is programmed to: • 1, memory accesses are enabled on the CL-GD7542. • 0, memory accesses are not enabled on the CL-GD7542.
0	**Enable I/O Accesses:** When the CL-GD7542 is configured for PCI Bus and this bit is programmed to: • 1, I/O accesses are enabled on the CL-GD7542. • 0, I/O accesses are not enabled on the CL-GD7542. Regardless of state of this bit, I/O accesses to PCI configuration registers (PC100, PC104, PC110, and PC13C) are always enabled.

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6.2.13 PCI04: PCI Status Register

PCI Configuration Address: 04

Index: –

Bit	Description	Reset State
31	Reserved	
30	Reserved	
29	Reserved	
28	Reserved	
27	Reserved	
26	DEVSEL# Timing [1]	0
25	DEVSEL# Timing [0]	0
24	Reserved	
23	Reserved	
22	Reserved	
21	Reserved	
20	Reserved	
19	Reserved	
18	Reserved	
17	Reserved	
16	Reserved	

This 16-bit register, which is accessible and effective only if the CL-GD7542 is configured for PCI Bus, consists of the most-significant two bytes of the PCI Status / PCI Command Register.

Bit	Description
31:27	Reserved
26:25	**DEVSEL# Timing [1:0]:** When the CL-GD7542 is configured for PCI bus, this read-only field always returns the value 00 to indicate fast DEVSEL# timing.
24:16	Reserved

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6.2.14 PCI10: PCI Base Address Register

PCI Configuration Address: 10 Hex

Index: –

Bit	Description	Reset State
31	PCI Base Address for Display Memory [31]	0
30	PCI Base Address for Display Memory [30]	0
29	PCI Base Address for Display Memory [29]	0
28	PCI Base Address for Display Memory [28]	0
27	PCI Base Address for Display Memory [27]	0
26	PCI Base Address for Display Memory [26]	0
25	PCI Base Address for Display Memory [25]	0
24	PCI Base Address for Display Memory [24]	0
23:1	Reserved	
0	Memory / I/O Indicator	0

This 32-bit register, which is accessible and effective only when the CL-GD7542 is configured for PCI bus, contains the PCI Base Address for display memory.

Bit	Description
31:24	**PCI Base Address for Display Memory [31:24]:** When the CL-GD7542 is configured for PCI bus, this field contains the base address of the contiguous 16-Mbyte display memory block reserved for the CL-GD7542.
23:1	Reserved
0	**Memory / I/O Indicator:** When the CL-GD7542 is configured for PCI bus, this bit is used to indicate the type of address space requested, either memory or I/O. • When this bit: — is 0, a memory address space is requested. — is 1, an I/O address space is requested. • For the PCI BIOS, this bit is read/write. • For the VGA BIOS, this bit is read only.

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6.2.15 PCI3C: PCI Interrupt Pin and PCI Interrupt Line Register

PCI Configuration Address: 3C Hex

Index: –

Bit	Description	Reset State
15	PCI Interrupt Pin [7]	0
14	PCI Interrupt Pin [6]	0
13	PCI Interrupt Pin [5]	0
12	PCI Interrupt Pin [4]	0
11	PCI Interrupt Pin [3]	0
10	PCI Interrupt Pin [2]	0
9	PCI Interrupt Pin [1]	0
8	PCI Interrupt Pin [0]	1
7	PCI Interrupt Line [7]	0
6	PCI Interrupt Line [6]	0
5	PCI Interrupt Line [5]	0
4	PCI Interrupt Line [4]	0
3	PCI Interrupt Line [3]	0
2	PCI Interrupt Line [2]	0
1	PCI Interrupt Line [1]	0
0	PCI Interrupt Line [0]	0

This register, which is accessible and effective only when the CL-GD7542 is configured for PCI bus, contains data from the PCI Interrupt Pin and PCI Interrupt Line.

Bit	Description
15:8	**PCI Interrupt Pin [7:0]:** When the CL-GD7542 is configured for PCI bus, this read-only field contains the value 01 hex. This value indicates the CL-GD7542 INTR# interrupt request pin is connected to the PCI Bus INTA# interrupt request pin.
7:0	**PCI Interrupt Line [7:0]:** When the CL-GD7542 is configured for PCI bus, this read/write field contains an 8-bit value that has no direct effect on the CL-GD7542. This field is used to transfer an interrupt pointer from the PCI system BIOS to the CL-GD7542 VGA BIOS.

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6.2.16 46E8 Alternate Sleep Mode Register

I/O Port Address: 46E8

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Alternate Sleep Mode Select	1
2	Reserved	
1	Reserved	
0	Reserved	

This register is active only when the following two conditions are both filled:

1. There is a low-to-high transition of the Reset# signal.
2. There is an external pull-up resistor on the S46 / MD[21] pin, which disables the 3C3 Sleep Mode Register.

Unless both conditions are filled, register 3C3 is the sleep mode register.

Bit	Description
7:4	Reserved
3	**Alternate Sleep Mode Select:** When there is a pull-up resistor on the CL-GD7542 pin S46 / MD[21], and when this bit: • is 1, the CL-GD7542: — is enabled. — can respond to normal bus and video display activity. • is 0, the CL-GD7542: — is disabled and will not affect the video display activity. — will respond normally to BIOS access. — will not respond to accesses to I/O, except to those addressed to 46E8. — will not respond to any accesses to display memory.
2:0	Reserved

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6.3 Sequencer Registers

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6.3.1 SRX: Sequencer Index Register

I/O Port Address: 3C4

Index: –

Bit	Description	Reset State
7	Fine Position HW Cursor and HW Icon [2]	0
6	Fine Position HW Cursor and HW Icon [1]	0
5	Fine Position HW Cursor and HW Icon [0] / Sequencer Index [5]	0
4	Sequencer Index [4]	0
3	Sequencer Index [3]	0
2	Sequencer Index [2]	0
1	Sequencer Index [1]	0
0	Sequencer Index [0]	0

Depending on this register's index value, this register has one of two possible purposes:

1. The primary purpose is to extend the sequencer index from 3 bits to 6 bits. The index specifies which register in the CL-GD7542 sequencer block is to be accessed by the next I/O read or write to Address 3C5. An index number greater than 5 points to registers that are defined in this manual's Extension Registers in section 6.7.
2. The secondary purpose is to specify the fine position of the hardware cursor and the hardware icon, both horizontal and vertical.

Bit	Description
7:5	**Fine Positions for Hardware Cursor and Hardware Icon:** **Vertical Fine Position for Hardware Cursor and Hardware Icon [2:0]:** When Extension Register SR11 is programmed, bits SRX[7:5] define in scan-lines the vertical fine position of the hardware cursor and icon. **Horizontal Fine Position for Hardware Cursor and Hardware Icon [2:0]:** When Extension Register SR10 is programmed, bits SRX[7:5] define in dot clocks (pixels) the horizontal fine position of the hardware cursor and icon. For special modes requiring extra dot clocks for fine position adjustments, a fourth, most-significant bit has been added to Attribute Controller Registers SR2E and SR2A. • Hardware Cursor Bit: Extension Register SR2E[0] — For the horizontal fine position of the hardware cursor, SR2E[0] is an added fourth and most-significant bit. — This bit is used in horizontally expanded graphics modes. • Hardware Icon Bit: Extension Register SR2A[6] — For the horizontal fine position of the hardware icon, SR2A[6] is an added fourth and most-significant bit. — This bit is used in horizontally expanded graphics modes and for text modes with 9-dot and 10-dot fonts, such as 640 x 480 displays that are expanded to 800 x 600.

Continued on next page.

6.3.1 SRX: Sequencer Index Register *(cont.)*

Bit	Description
5:0	**Sequencer Index [5:0]:** • When writing to any CL-GD7542 sequencer index *except* 10h or 11h: — These bits become a 6-bit sequencer index field, SRX[5:0]. — The SRX[5:0] field selects the register to be accessed with the next I/O read or I/O write to I/O Port Address 3C5. • When writing *to* CL-GD7542 sequencer index 10h or 11h: — These bits become a 5-bit sequencer index field, SRX[4:0]. — The SRX[4:0] field selects the sequencer index, SRX[7:5], used to define the fine position for the hardware cursor and hardware icon. — Extension registers SR2A[6] and SR2E[0]) also define the fine position for the hardware cursor and hardware icon.

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6.3.2 SR0: Reset Register

I/O Port Address: 3C5

Index: 0

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Synchronous Reset	1
0	Asynchronous Reset	1

This register is used to reset the CL-GD7542 sequencer. These bits are for VGA-standard compatibility only, and after reset they need never be used.

Bit	Description
7:2	Reserved
1	**Synchronous Reset:** When this bit is programmed to: • 0, the sequencer is cleared and halted, which disables screen refresh and display memory refresh. • 1, and when SR0[0] = 1, the sequencer will operate normally.
0	**Asynchronous Reset:** When this bit is programmed to: • 0, the sequencer is cleared and halted, and SR3 is cleared. • 1, and when SR0[1] = 1, the sequencer will operate normally.

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6.3.3 SR1: Clocking Mode Register

I/O Port Address: 3C5

Index: 1

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Full Display Memory Bandwidth	0
4	Shift and Load 32 Data Bits	0
3	Dot Clock	0
2	Shift and Load 16 Data Bits	0
1	Reserved	
0	8/9 Dot Clock	0

This register is used to control some miscellaneous functions in the CL-GD7542 sequencer.

Bit	Description
7:6	Reserved
5	**Full Display Memory Bandwidth:** When this bit is programmed to: • 0, the CRT screen is turned on, and the CL-GD7542 operates normally. • 1, the CRT screen is turned off. In addition: — The CPU uses nearly 100% of the display memory bandwidth. — HSYNC and VSYNC continue normally. — The BLANK# signal goes active and stays active. — The refresh for the display memory will continue normally.
4	**Shift and Load 32 Data Bits:** This bit, in conjunction with SR1[2], controls how often 32-bit graphics controller display data shifters are loaded, according to the following table:

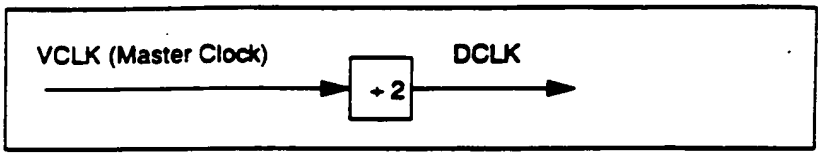
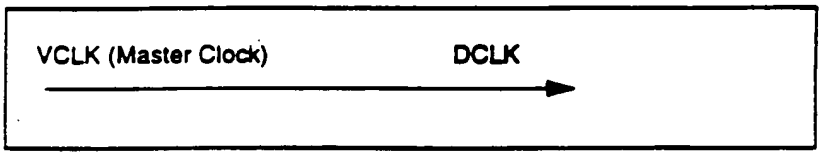
SR1		Data Shifters Loaded
[4]	[2]	
0	0	Every character clock
0	1	Every 2nd character clock
1	x	Every 4th character clock

Continued on next page.

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6.3.3 SR1: Clocking Mode Register *(cont.)*

Bit	Description
3	**Dot Clock:** When this bit is programmed to: • 1, VCLK (the Master Clock) is divided by 2 to generate DCLK, a dot clock that is half the frequency of the Master Clock. This dot clock is used for low-resolution video modes such as 0, 1, 4, 5, and D.  • 0, VCLK (the Master Clock) is not divided by 2. In this case, the clock that is used as the dot clock is the same frequency as the Master Clock. 
2	**Shift and Load 16 Data Bits:** This bit controls how often 16-bit graphics controller display data shifters are loaded. (Refer to the description of bit [4] of this register.)
1	Reserved
0	**8/9 Dot Clock:** When this bit is programmed to: • 0, then character clocks 8 dots wide are generated, used in all modes by mode 7, in which there are 320 or 640 horizontal dots. • 1, then character clocks 9 dots wide are generated, used in the monochrome mode 7, in which there are 720 horizontal dots.

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6.3.4 SR2: Plane Mask Register

I/O Port Address: 3C5

Index: 2

Bit	Description	Reset State
7	Enable Writing Pixel 7 / Reserved	0
6	Enable Writing Pixel 6 / Reserved	0
5	Enable Writing Pixel 5 / Reserved	0
4	Enable Writing Pixel 4 / Reserved	0
3	Enable Writing Pixel 3 / Bit-Map Plane 3 Enable	0
2	Enable Writing Pixel 2 / Bit-Map Plane 2 Enable	0
1	Enable Writing Pixel 1 / Bit-Map Plane 1 Enable	0
0	Enable Writing Pixel 0 / Bit-Map Plane 0 Enable	0

This register has two uses.
1. Its first use is to control the writing of up to eight pixels.
2. Its second use is to enable or disable writing to the four bit-map planes of display memory.

Bit	Description
7:0	**Enable Writing Pixel [7:0]:** • These bits can control whether individual pixel data bits [7:0] are written. • To enable an individual pixel, the corresponding Enable Writing Pixel bit must be set to 1, and *one* of the following conditions must be met: — Extended Write Mode 4 or Extended Write Mode 5 is selected with Graphics Controller Register bits GR5[2:0]. — Write Mode 1 is selected with Graphics Controller Register bits GR5[2:0], and Extension Register GRB[2] is set to 1. • This field is also used as a write protect for the BitBLT (bit block transfer) engine.
7:4	**Reserved:** These four bits are reserved when Extended Write Modes 4 and 5 are disabled (that is, Graphics Controller Register bits GR5[2] = 0), which would be the case for VGA-compatibility modes.
3:0	**Bit-Map Plane Enable [3:0]:** These four bits are used to control whether individual display memory bit-map planes [3:0] are written with Write Modes [3:0].

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6.3.5 SR3: Character Map Set Select Register

I/O Port Address: 3C5

Index: 3

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Secondary Character Map Set Select [0]	0
4	Primary Character Map Set Select [0]	0
3	Secondary Character Map Set Select [2]	0
2	Secondary Character Map Set Select [1]	0
1	Primary Character Map Set Select [2]	0
0	Primary Character Map Set Select [1]	0

This register is used to specify the primary and the secondary character map sets (fonts). This register applies only to text modes.

Bit	Description
7:6	Reserved
5, 3:2	**Secondary Character Map Set Select:** These three bits select from among the secondary character map sets, according to the following table:

SR3			Secondary Character Map Set	Address Offset (Kbytes)
[5]	[3]	[2]		
0	0	0	0	0
0	0	1	1	16
0	1	0	2	32
0	1	1	3	48
1	0	0	4	8
1	0	1	5	24
1	1	0	6	40
1	1	1	7	56

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6.3.5 SR3: Character Map Set Select Register *(cont.)*

Bit **Description**

4, 1:0 **Primary Character Map Set Select:**
These three bits select from among the primary character map sets, according to the following table:

SR3			Primary Character Map Set	Address Offset (Kbytes)
[4]	[1]	[0]		
0	0	0	0	0
0	0	1	1	16
0	1	0	2	32
0	1	1	3	48
1	0	0	4	8
1	0	1	5	24
1	1	0	6	40
1	1	1	7	56

NOTES:

(1) In text video display modes:
1. Character Map Plane 0 stores the ASCII text character code.
2. Character Map Plane 1 stores the attribute byte.
3. Character Map Plane 2 stores the character map set (the font).

(2) Bit 3 of the attribute byte normally controls the intensity of the foreground color.

This bit may be redefined to be a switch between character sets, allowing 512 displayable characters.

This switch is enabled whenever SR4[1] is a 1 *AND* there is a difference between the values of the Primary Character Map Set Select and the values of the Secondary Character Map Set Select.

(3) The format for the Character Map Plane 2 font address bits [15:0] is:
F2 F1 F0 C7 C6 C5 C4 C3 C2 C1 C0 R4 R3 R2 R1 R0
where:
F[2:0] is the character map set select
C[7:0] is the ASCII text character code
R[4:0] is the character row (the scanline in the character cell)

6.3.6 SR4: Memory Mode Register

I/O Port Address: 3C5

Index: 4

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Chain-4	0
2	Odd/Even Mode	0
1	Extended Memory	0
0	Reserved	

This register is used to control some miscellaneous functions in the CL-GD7542 sequencer.

Bit	Description
7:4	Reserved
3	**Chain-4:** When this bit is programmed to 1: • This bit takes priority over SR4[2] (Odd/Even Mode) and Graphics Controller Register GR5[4] (Odd/Even Addressing Mode). • Its effect is similar to SR4[2] (Odd/Even Mode), except both A0 and A1 are used. — Address A0 provides display memory Plane Select Bit [0]. — Address A1 provides display memory Plane Select Bit [1]. • The Graphics Controller Read Map Register (GR4) is ignored.
2	**Odd/Even Mode:** • When this bit is programmed to 0, the sequencer is in Odd/Even Mode. • This bit *must* be programmed to a 0 for text modes. • The value of this bit must track Graphics Controller Register GR5[4] (Odd/Even Addressing Mode), and the values must be opposite. — The even CPU addresses will access display memory planes 0 and 2. — The odd CPU addresses will access display memory planes 1 and 3. • This bit may be overridden by the SR4[3] bit.
1	**Extended Memory:** When this bit is programmed to: • 0, effective memory size is 64K, regardless of actual installed memory. (EGA modes require this to be the case.) • 1, effective memory size equals actual installed memory.
0	Reserved

6.4 CRT Controller Registers

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6.4.1 CRX: CRT Controller Index Register

I/O Port Address: 3?4

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	CRTC Index [5]	0
4	CRTC Index [4]	0
3	CRTC Index [3]	0
2	CRTC Index [2]	0
1	CRTC Index [1]	0
0	CRTC Index [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This index register is used to specify the register in the CRT Controller block to be accessed by the next I/O read or I/O write to Address 3?5. Registers at indices 19, 1A, 1B, 25, and 27 are described in this manual's section on the CL-GD7542 Extension Registers, in section 6.7.

Bit	Description
7:6	Reserved
5:0	**CRTC Index [5:0]:** The value resulting from these bits point to the register to be accessed in the next I/O read or I/O write to address 3?5. (Note that registers above 18 were never documented by IBM.)

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6.4.2 CR0: Horizontal Total Register

I/O Port Address: 3?5

Index: 0

Bit	Description	Reset State
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to specify the total number of character clocks per horizontal period.

Bit	Description
7:0	**Horizontal Total:** This 8-bit field specifies the total number of character clocks per horizontal period as follows: • The VCLK signal provides the character clock. (The character clock is derived from VCLK, according to the character width.) • The character counter counts the total number of character clocks. • The value in the character counter is then compared with the value in this register to provide the basic horizontal timing. • All horizontal and vertical timing is eventually derived from the basic horizontal timing in this register. The value of the horizontal total for this register may be calculated as follows: FROM: Total number of character clocks (from character counter) SUBTRACT: - 5 character clocks (for standard VGA compatibility) TO GET: = Horizontal total Example: If 80 characters are desired per horizontal scanline, then a value of 75 must be loaded into this register. Figure 6–1 indicates the way the horizontal and vertical timing is defined. • The horizontal timing is calculated in terms of character clock periods. • The vertical timing is calculated in terms of horizontal periods. Table 6–1 indicates how the various CRT Controller timing registers are extended.

Continued on next page.

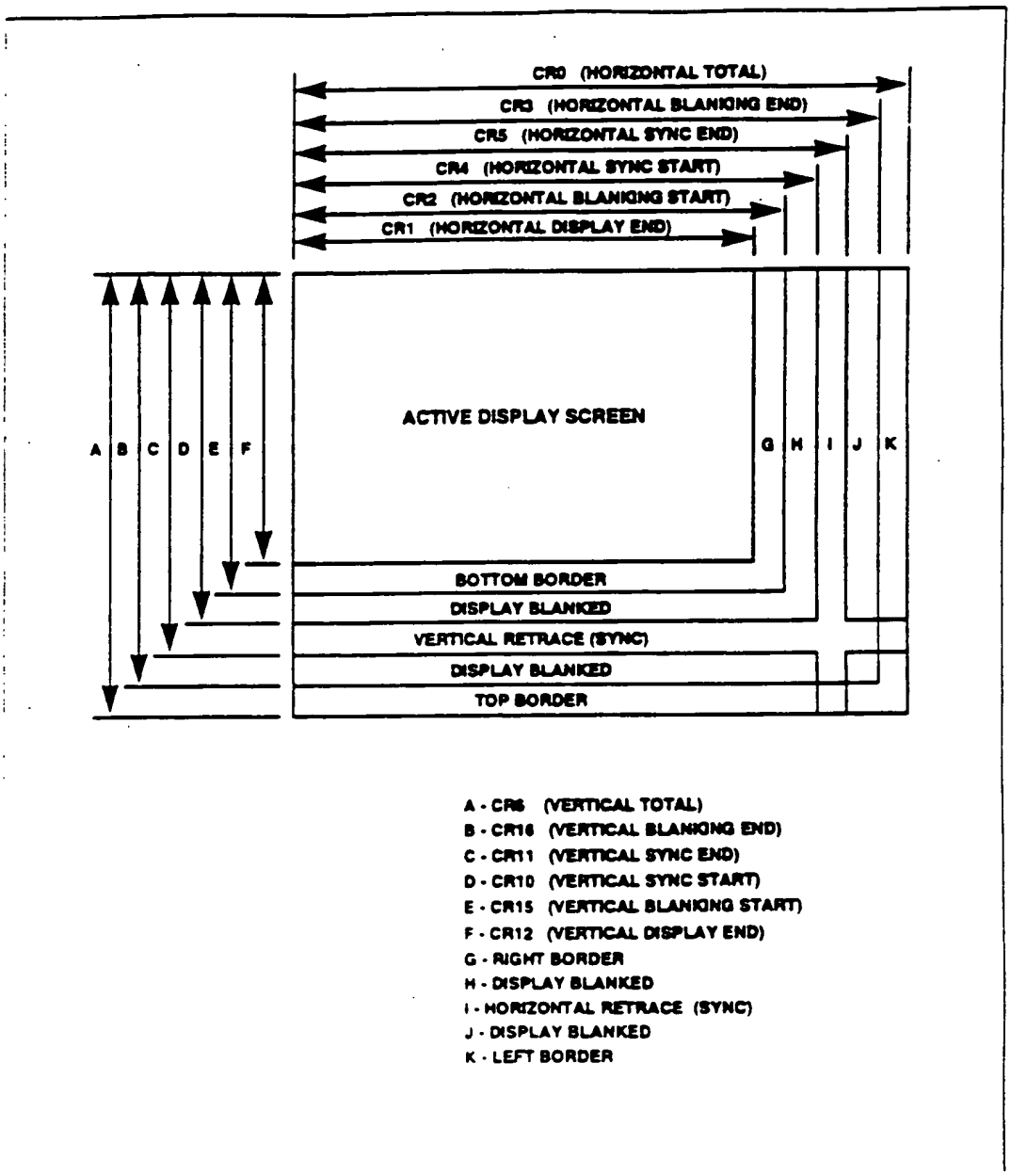


Figure 6–1. CRTC Timing Registers

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The following table is a guide to the location of the CRT controller timing registers and accompanying extension and overflow bits.

- An extension bit is a bit added by Cirrus Logic to the standard VGA controller bits.
- An overflow bit is a standard VGA controller bit that results from using more than eight bits to define a field.

Table 6–1. Summary of CRT Controller Timing Register Bits[a]

Parameter	CRT Controller Register Bit Position					
	[9]	[8]	[7]	[6]	[5]	[4:0]
H Total			**CR0[7]**	**CR0[6]**	**CR0[5]**	**CR0[4:0]**
H Display End			**CR1[7]**	**CR1[6]**	**CR1[5]**	**CR1[4:0]**
H Blanking Start			**CR2[7]**	**CR2[6]**	**CR2[5]**	**CR2[4:0]**
H Blanking End			**CR1A[5]**	**CR1A[4]**	**CR5[7]**	**CR3[4:0]**
H Sync Start			**CR4[7]**	**CR4[6]**	**CR4[5]**	**CR4[4:0]**
H Sync End						**CR5[4:0]**
V Total	**CR7[5]**	**CR7[0]**	**CR6[7]**	**CR6[6]**	**CR6[5]**	**CR6[4:0]**
V Sync Start	**CR7[7]**	**CR7[2]**	**CR10[7]**	**CR10[6]**	**CR10[5]**	**CR10[4:0]**
V Sync End						**CR11[3:0]**
V Display End	**CR7[6]**	**CR7[1]**	**CR12[7]**	**CR12[6]**	**CR12[5]**	**CR12[4:0]**
V Blanking Start	**CR9[5]**	**CR7[3]**	**CR15[7]**	**CR15[6]**	**CR15[5]**	**CR15[4:0]**
V Blanking End	**CR1A[7]**	**CR1A[6]**	**CR16[7]**	**CR16[6]**	**CR16[5]**	**CR16[4:0]**
Line Compare	**CR9[6]**	**CR7[4]**	**CR18[7]**	**CR18[6]**	**CR18[5]**	**CR18[4:0]**
Offset		**CR1B[4]**	**CR13[7]**	**CR13[6]**	**CR13[5]**	**CR13[4:0]**

a. Bits shown in **bold text** are extensions.

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6.4.3 CR1: Horizontal Display End Register

I/O Port Address: 3?5

Index: 1

Bit	Description	Reset State
7	Horizontal Display End [7]	0
6	Horizontal Display End [6]	0
5	Horizontal Display End [5]	0
4	Horizontal Display End [4]	0
3	Horizontal Display End [3]	0
2	Horizontal Display End [2]	0
1	Horizontal Display End [1]	0
0	Horizontal Display End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to specify the number of character clocks during horizontal display time.

Bit	Description
7:0	**Horizontal Display End [7:0]:** For the horizontal display time, this register specifies the number of character clocks, *minus 1*, as calculated for both text modes and graphics modes. • For text modes: CR1[7:0] = "Number of character clocks" – 1 Where number of character clocks = Number of characters • For graphics modes: CR1[7:0] = "Number of character clocks" – 1 Where number of character clocks = (Number of pixels/scanline) ÷ (Number of pixels/character clock) For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.4 CR2: Horizontal Blanking Start Register

I/O Port Address: 3?5

Index: 2

Bit	Description	Reset State
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to specify the character count where horizontal blanking starts.

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** This register specifies the character count at which horizontal blanking starts. • For text modes: Character count at which horizontal blanking starts = Number of characters • For graphics modes: Character count at which horizontal blanking starts = (Number of pixels/scanline) ÷ (Number of pixels/character clock) • For both text modes and graphics modes: The value programmed into CR2 must always be larger than the value programmed into CRT Controller Register CR1. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.5 CR3: Horizontal Blanking End Register

I/O Port Address: 3?5

Index: 3

Bit	Description	Reset State
7	Compatible Read	0
6	Display Enable Delay [1]	0
5	Display Enable Delay [0]	0
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to determine the horizontal blanking period width. Also, this register controls access to CRT Controller Registers CR10 and CR11 and the display enable delay.

Bit	Description
7	**Compatible Read:** When this bit: • = 0, CRT Controller Registers CR10 and CR11 are write-only registers. • = 1, CRT Controller Registers CR10 and CR11 are read/write registers.
6:5	**Display Enable Delay [1:0]:** This two-bit field is used to specify the number of character clocks that the display enable signal is delayed from the horizontal total. This delay is necessary to compensate for the accesses of the character code, attribute byte, font, etc. The following table indicates programming for the display enable signal delay:

CR3		Delay for Display Enable Signal (in number of character clocks)
[6]	[5]	
0	0	No delay
0	1	1 character clock (typical setting)
1	0	2 character clocks
1	1	3 character clocks

NOTE: If the delay is programmed too low, the left-most character will be repeated. If the delay is programmed too high, one or more characters will disappear at the left of each character row.

Continued on next page.

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6.4.5 CR3: Horizontal Blanking End Register *(cont.)*

Bit	Description
4:0	**Horizontal Blanking End [4:0]:** The horizontal blanking end field consists of these 5 bits (and as needed, a sixth bit in CR5[7]). This field determines the width of the horizontal blanking period. The least-significant five (or six) bits of the character counter are compared with the contents of this field. When a match occurs, the horizontal blanking period ends. The horizontal blanking end value to be programmed into this register may be calculated as follows: FROM: Horizontal blanking start (value programmed into CR2) SUBTRACT: − Horizontal blanking period (as desired) TO GET: = Horizontal blanking end • The horizontal blanking period: — must never be programmed to extend past the horizontal total. — is limited to 63 character-clock times. • The horizontal blanking end field is extended as follows: — CR5[7] is the horizontal blanking end field bit [5], which extends this field to 6 bits. — When either Extension Register CR1B[5] = 1 or Extension Register CR1B[7] = 1, Extension Register bits CR1A[5:4] further extend the horizontal blanking end field to eight bits with bits [7:6]. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.6 CR4: Horizontal Sync Start Register

I/O Port Address: 3?5

Index: 4

Bit	Description	Reset State
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the time at which horizontal sync becomes active.

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** This field specifies the character count at which the horizontal sync signal becomes active. Adjusting the value in this field moves the display horizontally on the screen. • The horizontal sync start must be programmed to a value either equal to or greater than horizontal display end. • The time from horizontal sync start to horizontal total must be either equal to or greater than four character-clock times. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.7 CR5: Horizontal Sync End Register

I/O Port Address: 3?5

Index: 5

Bit	Description	Reset State
7	Horizontal Blanking End [5]	0
6	Horizontal Sync Delay [1]	0
5	Horizontal Sync Delay [0]	0
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the position at which the horizontal sync pulse ends, effectively specifying the width of the pulse. In addition, this register contains an overflow bit and a field for the horizontal sync delay.

Bit	Description
7	**Horizontal Blanking End [5]:** This overflow bit increases by one bit the horizontal blanking end value of CR3[4:0].
6:5	**Horizontal Sync Delay [1:0]:** This two-bit field is used to specify the number of character clocks that the external horizontal sync pulse is delayed from the horizontal sync start position implied in CR4. In some video modes, this horizontal sync delay is necessary to allow internal timing signals that are triggered from horizontal sync start to begin, prior to display enable. The following table summarizes programming for the horizontal sync delay:

CR5		Delay for Horizontal Sync Pulse (in number of character clocks)
[6]	[5]	
0	0	No delay
0	1	1 character clock
1	0	2 character clocks
1	1	3 character clocks

Continued on next page.

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6.4.7 CR5: Horizontal Sync End Register *(cont.)*

Bit	Description
4:0	**Horizontal Sync End [4:0]:** This 5-bit field determines the width of the horizontal sync pulse. The least-significant five bits of the character counter are compared with the contents of this field. When a match occurs, the horizontal sync pulse ends. The horizontal sync end value to be programmed into this register may be calculated as follows: FROM: Horizontal sync start (value programmed in CR4) SUBTRACT: − Horizontal sync pulse width (as desired) TO GET: = Horizontal sync end The horizontal sync pulse: • has a width limited to 31 character-clock times. • must never be programmed to extend past the horizontal total of CR0. • must always end during the horizontal blanking period. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.8 CR6: Vertical Total Register

I/O Port Address: 3?5

Index: 6

Bit	Description	Reset State
7	Vertical Total [7]	0
6	Vertical Total [6]	0
5	Vertical Total [5]	0
4	Vertical Total [4]	0
3	Vertical Total [3]	0
2	Vertical Total [2]	0
1	Vertical Total [1]	0
0	Vertical Total [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the total number of scanlines per frame.

Bit	Description
7:0	**Vertical Total [7:0]:** This field is the least-significant eight bits of a ten-bit field that defines the total number of scanlines per frame. This field is extended with CR7[5] and CR7[0]. The value of the Vertical Total field to be programmed may be calculated as follows: FROM: Total number of horizontal scanlines SUBTRACT: - 2 scanlines TO GET: = Vertical Total field (total number of scanlines per frame) When the value in the scanline counter equals the value of the Vertical Total field, a vertical retrace period begins. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.9 CR7: Overflow Register

I/O Port Address: 3?5

Index: 7

Bit	Description	Reset State
7	Vertical Sync Start [9]	0
6	Vertical Display End [9]	0
5	Vertical Total [9]	0
4	Line Compare [8]	0
3	Vertical Blanking Start [8]	0
2	Vertical Sync Start [8]	0
1	Vertical Display End [8]	0
0	Vertical Total [8]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains bits that extend various vertical count fields. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

Bit	Description
7	**Vertical Sync Start [9]:** With CR7[2], this bit extends the vertical sync start field (CR10) to ten bits.
6	**Vertical Display End [9]:** With CR7[1], this bit extends the vertical display end field (CR12) to ten bits.
5	**Vertical Total [9]:** With CR7[0], this bit extends the vertical total field (CR6) to ten bits.
4	**Line Compare [8]:** With CR9[6], this bit extends the line compare field (CR18) to ten bits. This bit can always be written.
3	**Vertical Blanking Start [8]:** With CR9[5], this bit extends the vertical blanking start field (CR15) to ten bits.
2	**Vertical Sync Start [8]:** With CR7[7], this bit extends the vertical sync start field (CR10) to ten bits.
1	**Vertical Display End [8]:** With CR7[6], this bit extends the vertical display end field (CR12) to ten bits.
0	**Vertical Total [8]:** With CR7[5], this bit extends the vertical total field (CR6) to ten bits.

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6.4.10 CR8: Screen A Preset Row Scan Register

I/O Port Address: 3?5

Index: 8

Bit	Description	Reset State
7	Reserved	
6	Byte (Coarse) Panning [1]	0
5	Byte (Coarse) Panning [0]	0
4	Screen A Preset Row Scan [4]	0
3	Screen A Preset Row Scan [3]	0
2	Screen A Preset Row Scan [2]	0
1	Screen A Preset Row Scan [1]	0
0	Screen A Preset Row Scan [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the row scanline at which Screen A starts. This register also allows two types of scrolling:

- scrolling on a character row (scanline) basis (also called coarse panning)
- scanline (row) basis, also called fine scroll.
- In addition, this register specifies byte (coarse) panning.

Bit — **Description**

7 — Reserved

6:5 — **Byte (Coarse) Panning [1:0]:**
This two-bit field controls coarse panning. (For fine panning on a pixel-by-pixel basis, refer to Attribute Controller Register AR13.)

- This field can specify a coarse pan of up to 24 pixels, with 8-pixel resolution.
- Values for CR8[6:5] are interpreted as indicated in the following table:

CR8 [6]	CR8 [5]	Resulting Pan (in bytes)	Resulting Pan (in pixels)
0	0	0	0
0	1	1	8
1	0	2	16
1	1	3	24

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4:0 — **Screen A Preset Row Scan [4:0]:**
This field specifies the scanline at which the first character row will begin.

- This specification provides scrolling on a scanline basis (soft scrolling).
- The contents of this field should be changed only during vertical retrace.

6.4.11 CR9: Character Cell Height Register

I/O Port Address: 3?5

Index: 9

Bit	Description	Reset State
7	Control Scanline Double	0
6	Line Compare [9]	0
5	Vertical Blanking Start [9]	0
4	Character Cell Height [4]	0
3	Character Cell Height [3]	0
2	Character Cell Height [2]	0
1	Character Cell Height [1]	0
0	Character Cell Height [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the number of scanlines in the character cell. In addition, it contains two overflow bits and one control bit.

Bit	Description
7	**Control Scanline Double:** When this bit is 1, every scanline is displayed twice in succession. • Scanlines double for those specifications based on scanline counter addressing, such as Character Height, Cursor Start, Cursor End, and Cursor Underline location. • Typically, this bit is used to double a 200-scanline display to 400 scanlines. • The scanline doubling function is not available in interlaced video modes.
6	**Line Compare [9]:** With CR7[4], this bit extends the line compare field (CR18) to ten bits.
5	**Vertical Blanking Start [9]:** With CR7[3], this bit extends the vertical blanking start field (CR15) to ten bits.
4:0	**Character Cell Height [4:0]:** This field specifies the vertical size of the character cell in terms of scanlines. The value programmed into this field equals the actual size of the character cell (in scanlines), minus 1.

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6.4.12 CRA: Text Cursor Start Register

I/O Port Address: 3?5

Index: A

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Disable Text Cursor	0
4	Text Cursor Start [4]	0
3	Text Cursor Start [3]	0
2	Text Cursor Start [2]	0
1	Text Cursor Start [1]	0
0	Text Cursor Start [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains a bit that will disable the text cursor. In addition, this register specifies the scanline at which the text cursor is to start.

Bit	Description
7:6	Reserved
5	**Disable Text Cursor:** When this bit: • = 1, the text cursor will be disabled (that is, it will be removed). • = 0, the text cursor will function normally.
4:0	**Text Cursor Start [4:0]:** This field specifies the scanline within the character cell at which the text cursor is to start. When the Text Cursor Start value is: • less than the Text Cursor End value, no text cursor will display. • greater than the Text Cursor End value, no text cursor will display. • equal to the Text Cursor End value, the text cursor will display on a single scanline.

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6.4.13 CRB: Text Cursor End Register

I/O Port Address: 3?5

Index: B

Bit	Description	Reset State
7	Reserved	
6	Text Cursor Delay [1]	0
5	Text Cursor Delay [0]	0
4	Text Cursor End [4]	0
3	Text Cursor End [4]	0
2	Text Cursor End [4]	0
1	Text Cursor End [4]	0
0	Text Cursor End [4]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the scanline at which the text cursor is to end. It also contains a field that allows the text cursor display to be delayed from the location specified in CRE and CRF.

Bit	Description
7	Reserved
6:5	**Text Cursor Delay [1:0]:** This two-bit field specifies a delay, given in character clocks, from the text cursor location specified in CRE and CRF to the actual display of the text cursor.
4:0	**Text Cursor End [4:0]:** This field specifies the scanline within the character cell at which the text cursor is to end. When the Text Cursor End value is: • less than or equal to the character cell height, no text cursor will display. • greater than the character cell height, the effective text cursor end value will be equal to the character cell height.

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6.4.14 CRC: Screen A Start Address High Register

I/O Port Address: 3?5

Index: C

Bit	Description	Reset State
7	Screen A Start Address [15]	0
6	Screen A Start Address [14]	0
5	Screen A Start Address [13]	0
4	Screen A Start Address [12]	0
3	Screen A Start Address [11]	0
2	Screen A Start Address [10]	0
1	Screen A Start Address [9]	0
0	Screen A Start Address [8]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, along with CRD and Extension Register CR1B[3:2, 0], specify the display memory location at which data to be displayed on the screen starts.

Bit	Description
7:0	**Screen A Start Address [15:8]:** The 19-bit Screen A Start Address field contains a value that specifies the starting display memory location for data to be displayed on the screen. • Bits [18:16] are in Extension Register CR1B[3:2,0]. • Bits [15:8] are in this register. • Bits [7:0] are in CRT Controller Register CRD.

6.4.15 CRD: Screen A Start Address Low Register

I/O Port Address: 3?5

Index: D

Bit	Description	Reset State
7	Screen A Start Address [7]	0
6	Screen A Start Address [6]	0
5	Screen A Start Address [5]	0
4	Screen A Start Address [4]	0
3	Screen A Start Address [3]	0
2	Screen A Start Address [2]	0
1	Screen A Start Address [1]	0
0	Screen A Start Address [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, along with CRC and Extension Register CR1B[3:2, 0], specify the display memory location at which data to be displayed on the screen starts.

Bit	Description
7:0	**Screen A Start Address [7:0]:** The 19-bit Screen A Start Address field contains a value that specifies the starting display memory location for data to be displayed on the screen. • Bits [18:16] are in Extension Register CR1B[3:2,0]. • Bits [15:8] are in CRT Controller Register CRC. • Bits [7:0] are in this register.

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6.4.16 CRE: Text Cursor Location High Register

I/O Port Address: 3?5

Index: E

Bit	Description	Reset State
7	Text Cursor Location [15]	0
6	Text Cursor Location [14]	0
5	Text Cursor Location [13]	0
4	Text Cursor Location [12]	0
3	Text Cursor Location [11]	0
2	Text Cursor Location [10]	0
1	Text Cursor Location [9]	0
0	Text Cursor Location [8]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, along with CRF, specifies the display memory location at which the text cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [15:8]:** The Text Cursor Location is a 16-bit field that specifies the display memory location at which the text cursor is to be displayed. • Bits [15:8] are in this register. • Bits [7:0] are in CRT Controller Register CRF. • The value contained in this field specifies an address in display memory, not an offset from the beginning of the screen. When the value of the Screen A Start is changed without a compensating change in the Text Cursor Location field, the text cursor will move on the screen.

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6.4.17 CRF: Text Cursor Location Low Register

I/O Port Address: 3?5

Index: F

Bit	Description	Reset State
7	Text Cursor Location [7]	0
6	Text Cursor Location [6]	0
5	Text Cursor Location [5]	0
4	Text Cursor Location [4]	0
3	Text Cursor Location [3]	0
2	Text Cursor Location [2]	0
1	Text Cursor Location [1]	0
0	Text Cursor Location [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, with CRE, specifies the display memory location at which the text cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [7:0]:** The Text Cursor Location is a 16-bit field that specifies the display memory location at which the text cursor is to be displayed. • Bits [15:8] are in CRT Controller Register CRE. • Bits [7:0] are in this register.

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6.4.18 CR10: Vertical Sync Start Register

I/O Port Address: 3?5

Index: 10

Bit	Description	Reset State
7	Vertical Sync Start [7]	0
6	Vertical Sync Start [6]	0
5	Vertical Sync Start [5]	0
4	Vertical Sync Start [4]	0
3	Vertical Sync Start [3]	0
2	Vertical Sync Start [2]	0
1	Vertical Sync Start [1]	0
0	Vertical Sync Start [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

The Vertical Sync Start field specifies the scanline at which the Vertical Sync pulse is to become active.

Access to this register is controlled by CRT Controller Register CR3[7].

- When CR3[7] = 1, this register is read/write.
- When CR3[7] = 0, this register is write-only.

Bit	Description
7:0	**Vertical Sync Start [7:0]:** The Vertical Sync field specifies the scanline at which the Vertical Sync pulse will become active. • This register contains the least-significant eight bits [7:0] of that field. • Bits [9:8] in CRT Controller Register CR7[7,2] extend this field to ten bits. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

6.4.19 CR11: Vertical Sync End Register

I/O Port Address: 3?5

Index: 11

Bit	Description	Reset State
7	Write Protect CR7 through CR0	0
6	Refresh Cycle Control	0
5	Disable Vertical Interrupt	0
4	Clear Vertical Interrupt	0
3	Vertical Sync End [3]	0
2	Vertical Sync End [2]	0
1	Vertical Sync End [1]	0
0	Vertical Sync End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the scanline at which the Vertical Sync pulse is to become inactive, thereby effectively specifying the Vertical Sync pulse width. In addition, this register contains controls for the vertical interrupt and two miscellaneous control bits, CR11[7:6].

Access to this register is controlled by CR3[7].
- When CR3[7] = 1, this register is read/write.
- When CR3[7] = 0, this register is write-only.

Bit	Description
7	**Write Protect CR7 through CR0:** When this bit: • = 0, CR0 through CR7 can be written normally. • = 1, CR0 through CR7 cannot be written, except for CR7[4], which can always be written.
6	**Refresh Cycle Control:** When this bit: • = 0, three refresh cycles will be executed per scanline. • = 1, five refresh cycles will be executed per scanline.
5	**Disable Vertical Interrupt:** When this bit: • = 0, vertical interrupt is enabled and functions normally. • = 1, vertical interrupt is disabled, and the INTR pin cannot go active.
4	**Clear Vertical Interrupt:** When this bit: • = 0, the Interrupt Pending Bit (FEAT[7]) will be cleared to 0, and the INTR pin will be forced inactive. • = 1, it has no effect.

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6.4.19 CR11: Vertical Sync End Register *(cont.)*

Bit	Description
3:0	**Vertical Sync End [3:0]:** • This field determines the width of the Vertical Sync pulse. • The value of this field is compared with the least-significant four bits of the Scanline Counter. When a match occurs, the Vertical Sync pulse is ended. • The Vertical Sync pulse is limited to 15 scanlines. • The vertical sync end value to be programmed into this register may be calculated as follows: FROM: Vertical sync start (value programmed in CR10 and CR7[7,2]) SUBTRACT: – Vertical sync width (as desired) TO GET: = Vertical sync end The vertical sync pulse must never be programmed to extend past the Vertical Total. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.20 CR12: Vertical Display End Register

I/O Port Address: 3?5

Index: 12

Bit	Description	Reset State
7	Vertical Display End [7]	0
6	Vertical Display End [6]	0
5	Vertical Display End [5]	0
4	Vertical Display End [4]	0
3	Vertical Display End [3]	0
2	Vertical Display End [2]	0
1	Vertical Display End [1]	0
0	Vertical Display End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

The Vertical Display End field is used to specify the scanline at which the display is to end.

Bit	Description
7:0	**Vertical Display End [7:0]:** The Vertical Display End field is used to specify the scanline at which the display is to end. • The least-significant eight bits [7:0] of this field are in this register. • The most-significant two bits [9:8] are in register CR7[6,1]. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.21 CR13: Offset Register

I/O Port Address: 3?5

Index: 13

Bit	Description	Reset State
7	Offset [7]	0
6	Offset [6]	0
5	Offset [5]	0
4	Offset [4]	0
3	Offset [3]	0
2	Offset [2]	0
1	Offset [1]	0
0	Offset [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the display 'pitch,' which is the distance in the display memory between the beginnings of adjacent character rows or scanlines.

Bit	Description
7:0	**Offset [7:0]:** This register specifies the distance in display memory between the beginnings of adjacent character rows or scanlines. This field is extended to nine bits with Extension Register CR1B[4]. Except for the first scanline, to calculate the address from which to begin fetching data, add the contents of this register CR13 to the beginning address of the previous scanline or character row. Depending on the value of CR17[6], the offset will shift left either no or one bit positions.

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6.4.22 CR14: Underline Row Scanline Register

I/O Port Address: 3?5

Index: 14

Bit	Description	Reset State
7	Reserved	0
6	Double-Word Mode	0
5	Count by Four	0
4	Underline Scanline [4]	0
3	Underline Scanline [3]	0
2	Underline Scanline [2]	0
1	Underline Scanline [1]	0
0	Underline Scanline [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to enable or disable access to the Extension Registers.

Bit	Description
7	Reserved
6	**Double-Word Mode:** When this bit: • is 1, double-word addressing is selected. — The CRTC Memory Address Counter is rotated left for two bit positions. — As a result, display memory address bits MA[1] and MA[0] are sourced from CRTC Address Counter bits [13] and [12], respectively. • is 0, CR17[6] controls whether the CL-GD7542 uses the byte-address mode or the word-address mode.
5	**Count by Four:** When Double-Word mode: • is not enabled (CR14[6] = 0), this bit must be cleared to 0. • is enabled (CR14[6] = 1), this bit must be set to 1 to clock the Memory Address Counter with Character Clock divided by four.
4:0	**Underline Scanline [4:0]:** Within a character cell, this field specifies the scanline where the underline occurs.

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6.4.23 CR15: Vertical Blanking Start Register

I/O Port Address: 3?5

Index: 15

Bit	Description	Reset State
7	Vertical Blanking Start [7]	0
6	Vertical Blanking Start [6]	0
5	Vertical Blanking Start [5]	0
4	Vertical Blanking Start [4]	0
3	Vertical Blanking Start [3]	0
2	Vertical Blanking Start [2]	0
1	Vertical Blanking Start [1]	0
0	Vertical Blanking Start [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register specifies the scanline at which blanking is to become active.

Bit	Description
7:0	**Vertical Blanking Start [7:0]:** This 10-bit field specifies the scanline on which vertical blanking is to start. • The least-significant eight bits [7:0] of this field are in this register. • The most-significant two bits [9:8] of this field are in CRT Controller Registers CR9[5] and CR7[3]. For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.24 CR16: Vertical Blanking End Register

I/O Port Address: 3?5

Index: 16

Bit	Description	Reset State
7	Vertical Blanking End [7]	0
6	Vertical Blanking End [6]	0
5	Vertical Blanking End [5]	0
4	Vertical Blanking End [4]	0
3	Vertical Blanking End [3]	0
2	Vertical Blanking End [2]	0
1	Vertical Blanking End [1]	0
0	Vertical Blanking End [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

The Vertical Blanking End field specifies the scanline at which vertical blanking is to end.

Bit	Description
7:0	**Vertical Blanking End [7:0]:** The Vertical Blanking End field specifies the scanline at which vertical blanking is to end. When Extension Register CR1B[5] • = 0, the entire field is the eight bits of CRT Controller Register CR16[7:0]. • = 1, the field is extended to ten bits with Extension Register CR1A[7:6]. The contents of the Vertical Blanking End field are compared to the scanline counter to determine when to terminate vertical blanking. • If CR1B[5] is 0, this comparison limits the duration of vertical blanking to 255 scanlines. • If CR1B[5] is, this comparison does not limit the duration of vertical blanking to 255 scanlines. (That is, the duration of vertical blanking may be more than 255 scanlines.) For a summary of CRTC Timing Registers, refer to Figure 6–1 and Table 6–1.

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6.4.25 CR17: Mode Control Register

I/O Port Address: 3?5

Index: 17

Bit	Description	Reset State
7	CRTC Timing Logic Enable	0
6	Byte/Word Address Mode	0
5	Address Rotation	0
4	Reserved	
3	Count by Two	0
2	Multiply Vertical Registers by Two	0
1	Compatibility-Mode (Hercules™) Support	0
0	Compatibility-Mode (CGA) Support	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains a number of miscellaneous control bits.

Bit	Description
7	**CRTC Timing Logic Enable:** When this bit: • = 1, CRTC timing logic is enabled and functions normally. • = 0, CRTC timing logic is disabled, forcing a reset condition.
6	**Byte/Word Address Mode:** • When this bit = 1: — The Byte-Address mode is enabled. — Before the contents of the CRTC Address Counter are sent to display memory, they are not rotated. • When this bit = 0: — The Word-Address mode is enabled. — Before the contents of the CRTC Address Counter are sent to display memory, they are rotated left one bit position.
5	**Address Rotation:** • When CR17[6] = 1, this bit is ignored. • When CR17[6] = 0: — and this bit is 1, the left rotation described in CR17[6] above involves 16 bits of the CRTC Address Counter. — and this bit is 0, the left rotation described in CR17[6] above involves 14 bits of the CRTC Address Counter.
4	Reserved

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6.4.25 CR17: Mode Control Register *(cont.)*

Bit	Description
3	**Count by Two:** When this bit: • = 1, the CL-GD7542 clocks the Memory Address Counter with the Character Clock, divided by two. • = 0, the CL-GD7542 clocks the Memory Address Counter with the Character Clock.
2	**Multiply Vertical Registers by Two:** When this bit: • is 1, the Scanline Counter is clocked with Horizontal Sync, divided by two. (In effect, the Vertical Registers are multiplied by two.) — This division allows the number of scanlines to be doubled to 2048. — All periods will be even multiples of two scanlines. • is 0, the Scanline Counter is clocked with Horizontal Sync. — As a result, the number of scanlines is 1024.
1	**Compatibility-Mode (Hercules™) Support:** When this bit: • = 0, Scanline Counter bit [1] is substituted for CRTC Address Counter [14]. This substitution provides for Hercules™ compatibility. • = 1, the substitution described above does not occur.
0	**Compatibility-Mode (CGA) Support:** When this bit: • = 0, Scanline Counter bit [0] is substituted for CRTC Address Counter [14]. This substitution provides for CGA compatibility. • = 1, the substitution described above does not occur.

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6.4.26 CR18: Line Compare Register

I/O Port Address: 3?5

Index: 18

Bit	Description	Reset State
7	Line Compare [7]	0
6	Line Compare [6]	0
5	Line Compare [5]	0
4	Line Compare [4]	0
3	Line Compare [3]	0
2	Line Compare [2]	0
1	Line Compare [1]	0
0	Line Compare [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

The Line Compare field is used to specify where Screen A ends and Screen B starts for a vertically split screen.

Bit	Description
7:0	**Line Compare [7:0]:** The Line Compare field is used to implement a vertically split screen by specifying where Screen A ends and Screen B starts. • This register contains the eight least-significant bits [7:0] of this field. • The two most-significant bits [9:8] are in CR9[6] and CR7[4]. The top portion of the split screen is called Screen A. • Screen A may start anywhere in display memory. • Screen A can be panned and scrolled on a pixel-by-pixel basis. The bottom portion of the split screen is called Screen B. • Screen B always starts at location 0 in display memory. • Screen B cannot be panned or scrolled.

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6.4.27 CR22: Graphics Controller Data Latches Readback Register

I/O Port Address: 3?5

Index: 22

Bit	Description	Reset State
7	Graphics Controller Data Latch n Readback [7]	0
6	Graphics Controller Data Latch n Readback [6]	0
5	Graphics Controller Data Latch n Readback [5]	0
4	Graphics Controller Data Latch n Readback [4]	0
3	Graphics Controller Data Latch n Readback [3]	0
2	Graphics Controller Data Latch n Readback [2]	0
1	Graphics Controller Data Latch n Readback [1]	0
0	Graphics Controller Data Latch n Readback [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This register address is used to read the Graphics Controller Data Latches.

Bit	Description
7:0	**Graphics Controller Data Latch n Readback [7:0]:** This read-only register may be used to read back the contents of one of the four VGA graphics controller display memory data latches. • The number of the display memory data latch that is read back is selected with Graphics Controller Register GR4[1:0]. • The graphics controller data latches are loaded whenever display memory is read by the CPU.

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6.4.28 CR24: Attribute Controller Toggle Readback Register

I/O Port Address: 3?5

Index: 24

Bit	Description	Reset State
7	Attribute Controller Data-Index Toggle Readback	0
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register provides access to the Attribute Controller Toggle.

Bit	Description
7	**Attribute Controller Data-Index Toggle Readback:** When this bit: • = 1, on the next access, the Attribute Controller reads or writes a data value. • = 0, on the next access, the Attribute Controller reads or writes an index value.
6:0	Reserved

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6.4.29 CR26: Attribute Controller Index Readback Register

I/O Port Address: 3?5

Index: 26

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Video Enable Status	0
4	Attribute Controller Index [4]	0
3	Attribute Controller Index [3]	0
2	Attribute Controller Index [2]	0
1	Attribute Controller Index [1]	0
0	Attribute Controller Index [0]	0

NOTE: '?' in the above register addresses is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register provides access to the current Attribute Controller Index.

Bit	Description
7:6	Reserved
5	**Video Enable Status:** This bit provides the status of the Video Enable bit in Attribute Controller Index Register ARX[5].
4:0	**Attribute Controller Index [4:0]:** This field reads back the value that is in Attribute Controller Index ARX[4:0].

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6.5 Graphics Controller Registers

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6.5.1 GRX: Graphics Controller Index Register

I/O Port Address: 3CE

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Graphics Controller Index [5]	0
4	Graphics Controller Index [4]	0
3	Graphics Controller Index [3]	0
2	Graphics Controller Index [2]	0
1	Graphics Controller Index [1]	0
0	Graphics Controller Index [0]	0

This register is used to specify a graphics controller register.

Bit	Description
7:6	Reserved
5:0	**Graphics Controller Index [5:0]:** This field specifies one of the following: • a register in the Graphics Controller group • an Extension Register that is accessed by the next I/O read or I/O write to I/O Port Address 3CF.

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6.5.2 GR0: Set / Reset Register

I/O Port Address: 3CF

Index: 0

Bit	Description	Reset State
7	Write Mode 5 Background [7] / Reserved	0
6	Write Mode 5 Background [6] / Reserved	0
5	Write Mode 5 Background [5] / Reserved	0
4	Write Mode 5 Background [4] / Reserved	0
3	Write Mode 5 Background [3] / Set/Reset Plane 3	0
2	Write Mode 5 Background [2] / Set/Reset Plane 2	0
1	Write Mode 5 Background [1] / Set/Reset Plane 1	0
0	Write Mode 5 Background [0] / Set/Reset Plane 0	0

This register specifies:

- the background color, when Extended Write Mode 5 is selected.
- values to be written into the respective display memory planes when the processor executes a Write Mode 0 or Write Mode 3 operation.

For an overview of Write Modes, refer to the description in Graphics Controller Register GR5.

Bit	Description
7:0	**Write Mode 5 Background [7:0]:** When Graphics Controller Register GR5[2:0] selects Extended Write Mode 5, these bits [7:0] specify the background color for Extended Write Mode 5.
7:4	**Reserved:** • When Graphics Controller Register GR5[2:0] does not select Extended Write Mode 5, these bits are reserved. • When Extension Register GRB[2]: — is 0, writes to these bits are ignored, and reads return zeroes. — is 1, these bits are read/write, but bit contents are not used.
3:0	**Set/Reset Plane [3:0]:** When Graphics Controller Register GR5[2:0] does not select Extended Write Mode 5, these bits [3:0] control the values written into the respective display memory planes for Write Mode 3 and Write Mode 0.

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6.5.3 GR1: Set / Reset Enable Register

I/O Port Address: 3CF

Index: 1

Bit	Description	Reset State
7	Write Mode 4, 5 Foreground [7] / Reserved	0
6	Write Mode 4, 5 Foreground [6] / Reserved	0
5	Write Mode 4, 5 Foreground [5] / Reserved	0
4	Write Mode 4, 5 Foreground [4] / Reserved	0
3	Write Mode 4, 5 Foreground [3] / Enable Set/Reset Plane 3	0
2	Write Mode 4, 5 Foreground [2] / Enable Set/Reset Plane 2	0
1	Write Mode 4, 5 Foreground [1] / Enable Set/Reset Plane 1	0
0	Write Mode 4, 5 Foreground [0] / Enable Set/Reset Plane 0	0

This register:

- defines the foreground color when Extended Write Mode 4 or 5 is selected.
- is used with Graphics Controller Register GR0 to determine values to be written into the respective display memory planes when Write Mode 0 is selected.

For an overview of Write Modes, refer to the description in Graphics Controller Register GR5.

Bit	Description
7:0	**Write Mode 4, 5 Foreground [7:0]:** These bits specify the foreground color for an Extended Write Mode when: • Extended Write Mode 4 is selected. (Graphics Controller Register GR5[2:0] is 100). • Extended Write Mode 5 is selected. (Graphics Controller Register GR5[2:0] is 101).
7:4	**Reserved:** • When Graphics Controller Register GR5[2:0] selects Extended Write Mode 4 or 5, these bits are reserved. • When Extension Register GRB[2]: — is 0, writes to these bits are ignored, and reads return zeroes. — is 1, these bits are read/write, but bit contents are not used.
3 0	**Enable Set / Reset Plane [3:0]:** When Write Mode 0 is selected (Graphics Controller Register GR5[2:0] is 000) *ar 1* when a bit in this field: • = 1, the corresponding value in Graphics Controller Register GR0[3:0] is written into the corresponding display memory plane. • = 0, the corresponding value from the CPU data bus is written into the corresponding display memory plane.

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6.5.4 GR2: Color Compare Register

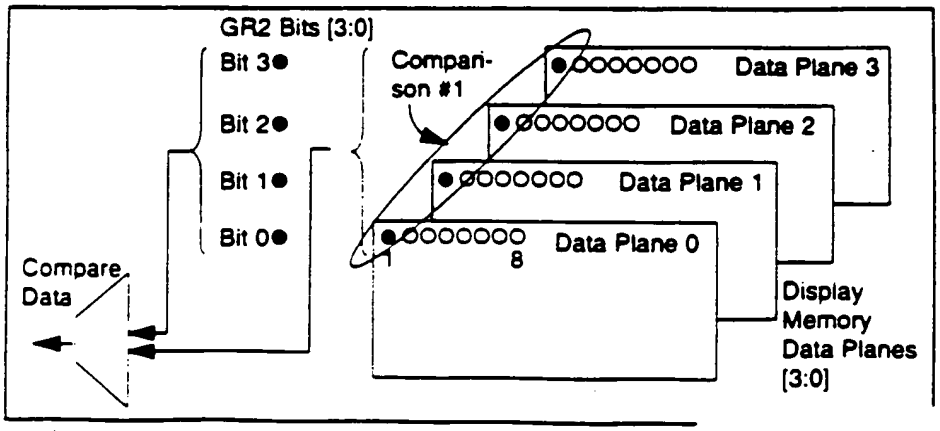
I/O Port Address: 3CF

Index: 2

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Compare Plane [3]	0
2	Color Compare Plane [2]	0
1	Color Compare Plane [1]	0
0	Color Compare Plane [0]	0

This register specifies the color compare plane(s) for Read Mode 1.

Bit	Description
7:4	Reserved
3:0	**Color Compare Plane [3:0]:** This field represents a color comparison value consisting of 1 to 4 bits. • GR5[3] must be set to 1 (Read Mode 1 is selected) to enable this field. • GR7[3:0] bits select display memory data planes for the comparison below. • For each selected display memory data plane, the color value of the corresponding bit in this field is compared to the color of the eight neighboring horizontal pixels in the corresponding display memory data plane. (For display memory data planes that are not chosen, their data is forced to match the values of the other data planes, becoming a "don't care" in the process.) • The eight bits from the comparison are read into the CPU.



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6.5.5 GR3: Data Rotate Register

I/O Port Address: 3CF

Index: 3

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Logical Function Select [1]	0
3	Logical Function Select [0]	0
2	Data Rotate Count [2]	0
1	Data Rotate Count [1]	0
0	Data Rotate Count [0]	0

This register contains two fields that are used with Write Modes 0 and 3.

Bit	Description
7:5	Reserved
4:3	**Logical Function Select [1:0]:** This two-bit field: • is used for Write Mode 0 only (Graphics Controller Register GR5[2:0] is 000). • selects the logical function operation that takes place between the data in the CPU data latches and the data from the CPU or Set/Reset Logic. The result of the functional operation is written into display memory. The logical function operations are summarized in the following table:

GR3		Logical Function Operation
[4]	[3]	
0	0	None: The data in the latches are ignored.
0	1	Data in latches is logically ANDed with data from CPU or Set/Reset Logic
1	0	Data in latches is logically ORed with data from CPU or Set/Reset Logic
1	1	Data in latches is logically XORed with data from CPU or Set/Reset Logic

2:0	**Data Rotate Count [2:0]:** This field allows data from the CPU bus to be rotated up to seven bit positions prior to being altered by the Set/Reset logic.

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6.5.6 GR4: Read Map Plane Select Register

I/O Port Address: 3CF

Index: 4

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Display Memory Data Plane Select [1]	0
0	Display Memory Data Plane Select [0]	0

This register is used to select a display memory data plane for Read Mode 0. (For an overview of the Write Modes, refer to the description in GR5.)

Bit	Description
7:2	Reserved
1:0	**Display Memory Data Plane Select [1:0]:** This field: • is used only when Read Mode 0 is selected (Graphics Controller Register GR5[3] = 1). • specifies the display memory data plane selected for a read by Read Mode 0, as shown in the following table:

GR4		Display Memory Data Plane Selected for Read by Read Mode 0
[1]	[0]	
0	0	Display Memory Data Plane 0
0	1	Display Memory Data Plane 1
1	0	Display Memory Data Plane 2
1	1	Display Memory Data Plane 3

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6.5.7 GR5: Mode Register

I/O Port Address: 3CF

Index: 5

Bit	Description	Reset State
7	Reserved	
6	256-Color Mode	0
5	Video Data Shift Register Mode	0
4	Odd/Even Addressing Mode	0
3	Read Mode	0
2	Write Mode [2]	0
1	Write Mode [1]	0
0	Write Mode [0]	0

This register specifies the Write Mode and Read Mode. In addition, it controls the configuration of the video data shift registers.

Bit	Description
7	Reserved
6	**256-Color Mode:** When this bit: • = 1, video data shift registers are configured for 256-color video modes, and Graphics Controller Register GR5[5] is ignored. • = 0, video data shift registers are configured for 16-, 4-, or 2-color video modes.
5	**Video Data Shift Register Mode:** When this bit: • = 0, video data shift registers are configured for EGA compatibility. • = 1, video data shift registers are configured for CGA compatibility, which is used for video modes 4 and 5.
4	**Odd/Even Addressing Mode:** • When this bit is 1, the CL-GD7542 is configured for odd/even addressing. • This bit should always be programmed to the opposite value as Sequencer Register SR4[2].

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6.5.7 GR5: Mode Register *(cont.)*

Bit **Description**

3 **Read Mode:**

This bit specifies whether the CL-GD7542 is in Read Mode 0 or Read Mode 1.

GR5 [3]	Read Mode	CPU Read Source
0	Read Mode 0	CPU reads data directly from display memory
1	Read Mode 1	CPU reads data that results from the color-compare logic of GR2

Read Mode 0:

- During Read Mode 0, the CPU reads data directly from display memory.
- Read Mode 0 returns eight adjacent bits of the display memory data plane specified in GR4[1:0].
- Read Mode 0 does not use the color-compare logic of register Graphics Controller Register GR2.
- A Read Mode 0 operation can be forced with an I/O read of CRT Controller Register CR22, the Graphics Controller Data Latches Readback Register.

Read Mode 1:

- During Read Mode 1, the CPU reads data that results from the color-compare logic of Graphics Controller Register GR2.
- Read Mode 1 allows eight adjacent pixels (16-color modes) to be compared to a specified color value in a single operation. Each of the eight bits returned to the CPU indicates the result of a comparison between the four bits of the Color Compare (Graphics Controller Register GR2[3:0]) and the bits from the four display memory planes.
- When the four bits of the Color Compare operation match the four bits from the display memory data planes, a 1 is returned for the corresponding bit position.
- When any bits in the Color Don't Care Plane (Graphics Controller Register GR7[3:0]) are zeroes, the value in the corresponding display memory data plane is forced to match the values of the other data planes, becoming a "don't care" in the process.

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CL 28604

6.5.7 GR5: Mode Register *(cont.)*

Bit **Description**

2:0 **Write Mode [2:0]:**

These bits specify if the CL-GD7542 is in Write or Extended Write Mode.

- When Extension Register GRB[2]=0, GR5[2] is forced to 0.

GR5			Write Mode Selected	
[2]	[1]	[0]		
0	0	0	GRB[2] = 0 forces GR5[2] = 0	Write Mode 0
0	0	1		Write Mode 1
0	1	0		Write Mode 2
0	1	1		Write Mode 3
1	0	0	Extended Write Mode 4	
1	0	1	Extended Write Mode 5	
1	1	0	Reserved	
1	1	1	Reserved	

Write Mode 0:

- Each of the four display memory data planes is written with the CPU data rotated by the number of counts in Graphics Controller Register GR3[2:0].
- When a bit in Graphics Controller Register GR1[3:0] is 1:
  - — the corresponding display memory data plane is written with the contents of the corresponding bit in GR0[3:0].
  - — under the control of GR3[4:3], the contents of CPU data latches may be logically combined with data from the set/reset logic.
- Bit planes are enabled with Sequencer Register SR2[3:0].
- Bit positions are enabled with Graphics Controller Register GR8.

Write Mode 1:

- Each of the four display memory data planes is written with data in CPU data latches, loaded from display memory by a previous read.
- Write Mode 1 ignores Graphics Controller Register GR8.

Write Mode 2:

- Display memory data planes [3:0] are written with CPU data bit values [3:0].
- Bit planes are enabled with Sequencer Register SR2[3:0].
- Bit positions are enabled with Graphics Controller Register GR8.
- Write Mode 2 ignores the data rotator, set/reset, and function-select fields.

Write Mode 3:

- Display memory plane data comes from corresponding bits of GR0[3:0].
- The bit-position-enable field is formed with the logical AND of Graphics Controller Register GR8 and the rotated CPU data.
- Write Mode 3 ignores the set/reset and function-select fields.

Continued on next page.

6.5.7 GR5: Mode Register *(cont.)*

Bit **Description**

2:0(cont.)

Extended Write Mode 4:

- The contents of GR1[7:0] are written into up to eight adjacent pixels.
- The CPU data bits are used to control whether a pixel is written.
  - — When a CPU data bit is a 1, the corresponding pixel is written.
  - — When a CPU data bit is a 0, the corresponding pixel is not changed.
- This mode can be used for 256-color text expansion for which the background is to be preserved.
- This mode can also be used for 64K-color text expansion for which the background is to be preserved.

Extended Write Mode 5:

- The contents of either GR1[7:0] or GR0[7:0] are written into each of eight adjacent pixels.
- For each of the eight pixels, the choice between GR1 and GR0 is made according to the value of the corresponding bit of the CPU data, summarized in the following table.

CPU Data	GR0 / GR1	Note
0	GR0	Background
1	GR1	Foreground

- This mode is intended for 256-color text expansion, for which both the foreground and background are to be written.
- This mode can also be used for 64K-color text expansion for which both the foreground and background are to be written.

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CL 28606

6.5.8 GR6: Miscellaneous Register

I/O Port Address: 3CF

Index: 6

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Display Memory Map [1]	0
2	Display Memory Map [0]	0
1	Chain Odd Maps to Even	0
0	Graphics Mode	0

This register contains miscellaneous control bits.

Bit — **Description**

7:4 — Reserved

3:2 — **Display Memory Map [1:0]:**
This field specifies the beginning address and size of the display memory in the CPU host address space. This field is summarized in the following table:

GR6 [3]	GR6 [2]	Display Memory Map Plane	Display Memory Address in CPU Host Address Space	Display Memory Size (Kbytes)	Affected Mode(s)
0	0	0	A000:0 to BFFF:F	128	Extended
0	1	1	A000:0 to AFFF:F	64	EGA / VGA
1	0	2	B000:0 to BFFF:F	32	Hercules
1	1	3	B800:0 to BFFF:F	32	CGA

1 — **Chain Odd Maps to Even:**
- When this bit is 1, CPU Address Bit[0] is replaced with a higher-order address bit. This replacement causes the even host addresses to access Planes 0 and 2, and the odd host addresses to access Planes 1 and 3.
- This mode is useful for MDA emulation.

0 — **Graphics Mode:**
When this bit:
- = 0, the CL-GD7542 functions in text (alphanumeric) modes.
- = 1, the CL-GD7542 functions in graphics (all-points-addressable) modes.

6.5.9 GR7: Color Don't-Care Plane Register

I/O Port Address: 3CF

Index: 7

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Don't-Care Plane [3]	0
2	Color Don't-Care Plane [2]	0
1	Color Don't-Care Plane [1]	0
0	Color Don't-Care Plane [0]	0

This register is used with Graphics Controller Register GR2 for Read Mode 1 accesses. (For an overview of the Read Modes, refer to the description of Graphics Controller Register GR5.)

Bit	Description
7:4	Reserved
3:0	**Color Don't-Care Plane [3:0]:** These four bits are used to control color compare logic for the four Color Don't-Care Planes. If a bit: • = 1, the corresponding plane is involved in color compares. • = 0, the corresponding plane is not involved in color compares.

6.5.10 GR8: Display Memory Bit Mask Register

I/O Port Address: 3CF

Index: 8

Bit	Description	Reset State
7	Display Memory Bit Write Enable [7]	0
6	Display Memory Bit Write Enable [6]	0
5	Display Memory Bit Write Enable [5]	0
4	Display Memory Bit Write Enable [4]	0
3	Display Memory Bit Write Enable [3]	0
2	Display Memory Bit Write Enable [2]	0
1	Display Memory Bit Write Enable [1]	0
0	Display Memory Bit Write Enable [0]	0

This register is used to control writing to display memory on a bit basis in Write Modes 0, 2, and 3.

Bit	Description
7:0	**Display Memory Bit Write Enable [7:0]:** Each bit in this register controls whether the corresponding bit in display memory is written in Write Modes 0, 2, or 3. When a bit: • = 1, the corresponding bit in display memory is written. • = 0, the corresponding bit in display memory is not written.

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CL 28609

6.6 Attribute Controller Registers

6.6.1 ARX: Attribute Controller Index Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Video Enable	0
4	Attribute Controller Index [4]	0
3	Attribute Controller Index [3]	0
2	Attribute Controller Index [2]	0
1	Attribute Controller Index [1]	0
0	Attribute Controller Index [0]	0

This register is used to specify the register in the Attribute Controller block that is accessed with the next I/O write to 3C0 or I/O read to 3C1.

For the Attribute Controller block, both the index and data registers are at the same port addresses, unlike other blocks, for which index and data registers are at different port addresses.

Alternate writes to ARX toggle between index and data. The CRT Controller Register CR24 provides access to the Attribute Controller Toggle, which reads or writes either a data value or an index value.

Bit	Description
7:6	Reserved
5	**Video Enable:** When this bit: • = 0, the screen displays the color indicated by AR11. • = 1, the screen displays normal video.
4:0	**Attribute Controller Index [4:0]:** This field is the index to the Attribute Controller data registers. The CRT Controller Register CR24 provides access to the current Attribute Controller index value.

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6.6.2 AR0 to ARF: Attribute Controller Palette Registers

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 0:F

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Secondary Red	0
4	Secondary Green / Intensity	0
3	Secondary Blue / Monochrome	0
2	Red	0
1	Green	0
0	Blue	0

These bits act as pointers to palette entries.

Bit	Description
7:6	Reserved
5:0	**Palette Entries:** In 16-color text and graphics modes, the digital attribute controller palette entries in this register are chosen by the four bits of pixel data, and they point to palette memory entries. • The palette memory entries are normally programmed, and so the DAC outputs reflect these values. • As a result, the palette memory is programmed to simulate standard EGA colors.

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6.6.3 AR10: Attribute Controller Mode Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 10

Bit	Description	Reset State
7	AR14 Video Source Enable	0
6	Pixel Double-Clock Select	0
5	Pixel Panning Compatibility	0
4	Reserved	
3	Character Blink Enable	0
2	Line Graphics Enable	0
1	Display Type	0
0	Graphics Mode	0

This register contains some miscellaneous control bits for the Attribute Controller.

Bit	Description
7	**AR14 Video Source Enable:** • When an 8-, 16-, or 24-bit pixel mode is chosen, this bit is ignored. • When this bit: — = 1, AR14[1:0] are used as the source for the Color Lookup Table address bits [5:4], which allows rapid selection of four 16-color palettes. — = 0, palette registers AR0 to ARF[5:4] are used as the source for the Color Lookup Table address bits [5:4].
6	**Pixel Double-Clock Select:** • When this bit is 0, pixels are clocked on every cycle. • When this bit is 1, pixels are clocked on every other clock cycle. Also: — Registers AR0 to ARF are bypassed. — This bit setting is used with Mode 13. — The CL-GD7542 sequencer logic operates at twice the pixel clock rate.
5	**Pixel Panning Compatibility:** When this bit: • = 0, the two parts of a split screen pan together. • = 1, a line compare match in the CRTC forces the output of the AR13 Pixel Panning Register to a 0 until the next VSYNC occurs. This action allows the panning of Screen A without Screen B.
4	Reserved
3	**Character Blink Enable:** When this bit: • = 0, character blinking is disabled • = 1, character blinking is enabled at the frequency rate of vertical refresh, divided by 32.

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6.6.3 AR10: Attribute Controller Mode Register *(cont.)*

Bit **Description**

2 **Line Graphics Enable:**
When this bit:
- = 0, bit 9 of a 9-bit-wide character cell is the same as the background.
- = 1, bit 9 of a 9-bit-wide character cell is made the same value as bit 8. This value is used for those character sets that have special characters associated with line graphics, for characters codes in the range C0 through DF.

1 **Display Type:**
This bit is used only if the CL-GD7542 is in alphanumeric modes When this bit:
- = 0, the Attribute Byte contents are treated as color attributes.
- = 1, the Attribute Byte contents are treated as MDA-compatible attributes.

The following table shows examples of monochrome attributes.

Bit Definitions for Attribute Byte								Hex Code Of Attribute Byte	Monochrome Attribute Byte
Blink Bit [7]	Background Bits			Intensity Bit [3]	Foreground Bits				
	[6]	[5]	[4]		[2]	[1]	[0]		
0	0	0	0	0	1	1	1	07h	Normal
0	0	0	0	1	1	1	1	0Fh	Intense
0	0	0	0	0	0	0	1	01h	Underline
0	0	0	0	1	0	0	1	09h	Underline Intense
0	1	1	1	0	0	0	0	70h	Reverse
1	1	1	1	0	0	0	0	F0h	Blinking Reverse

0 **Graphics Mode:**
When this bit:
- = 0, the Attribute Controller functions in text (alphanumeric) modes.
- = 1, the Attribute Controller functions in graphics (all-points-addressable) modes.

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6.6.4 AR11: Overscan (Border) Color Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 11

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	(Border Color Bit) Secondary Red	0
4	(Border Color Bit) Secondary Green	0
3	(Border Color Bit) Secondary Blue	0
2	(Border Color Bit) Red	0
1	(Border Color Bit) Green	0
0	(Border Color Bit) Blue	0

This register points to the entry in the Color Lookup Table that defines the Border Color.

- As shown in Figure 6–1 at CRT Controller Register CR0, the border is defined as that portion of the raster between blanking and active video, on all four sides of the screen.
- Typically, the Color Lookup Table entries are programmed, and so the color defined by the bits above is the color that results.

Bit	Description
7:6	Reserved
5:0	**Border Color Bits [5:0]:** Depending on if the CGA or EGA mode is in use, either four of these bits (for CGA) or six of these bits (for EGA) are used to select the Color Lookup Table entry for the Border Color in CGA and EGA Modes.

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6.6.5 AR12: Color Plane Enable Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 12

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Video Status Mux [1]	0
4	Video Status Mux [0]	0
3	Color Plane Enable [3]	0
2	Color Plane Enable [2]	0
1	Color Plane Enable [1]	0
0	Color Plane Enable [0]	0

This register contains:

- a field that chooses the inputs for diagnostic bits in STAT[5:4].
- a field that enables the four color planes in the Attribute Controller Palette Registers.

Bit	Description
7:6	Reserved
5:4	**Video Status Mux [1:0]:** This field chooses the inputs for the diagnostic status bits in STAT[5:4] as indicated in the following table:

AR12		STAT	
[5]	[4]	[5]	[4]
0	0	FP[2] Red	FP[0] Blue
0	1	FP[3] Secondary Blue	FP[1] Green
1	0	FP[5] Secondary Red	FP[4] Secondary Green
1	1	FP[7]	FP[6]

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6.6.5 AR12: Color Plane Enable Register *(cont.)*

Bit	Description
3:0	**Color Plane Enable [3:0]:** This field controls which display memory data plane will send data to a corresponding attribute controller color palette register, as shown in the following table:

AR12 Bit / State	Display Memory Data Plane	Result
AR12[3] = 0	Plane 3	Plane 3 disabled.
AR12[3] = 1		Plane 3 data selected for Color Palette Register 3.
AR12[2] = 0	Plane 2	Plane 2 disabled.
AR12[2] = 1		Plane 2 data selected for Color Palette Register 2.
AR12[1] = 0	Plane 1	Plane 1 disabled.
AR12[1] = 1		Plane 1 data selected for Color Palette Register 1.
AR12[0] = 0	Plane 0	Plane 0 disabled.
AR12[0] = 1		Plane 0 data selected for Color Palette Register 0.

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6.6.6 AR13: Pixel Panning Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 13

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Pixel Panning [3]	0
2	Pixel Panning [2]	0
1	Pixel Panning [1]	0
0	Pixel Panning [0]	0

This register:

- specifies the number of pixels the display data are shifted to the left.
- functions both in the graphics (all-points-addressable) and text (alphanumeric) modes.

Bit	Description
7:4	Reserved
3:0	**Pixel Panning [3:0]:** This field controls fine panning on a pixel-by-pixel basis by specifying the number of pixels the display data are shifted to the left. The values programmed into AR13[3:0] are interpreted as indicated in the following table:

AR13 [3]	AR13 [2]	AR13 [1]	AR13 [0]	Hex Code	Shift for 9-Bit Characters	Shift for 8-Bit Characters	Shift for Mode 13
0	0	0	0	0h	1 bit left	(none)	(none)
0	0	0	1	1h	2 bits left	1 bit left	–
0	0	1	0	2h	3 bits left	2 bits left	1 bit left
0	0	1	1	3h	4 bits left	3 bits left	–
0	1	0	0	4h	5 bits left	4 bits left	2 bits left
0	1	0	1	5h	6 bits left	5 bits left	–
0	1	1	0	6h	7 bits left	6 bits left	3 bits left
0	1	1	1	7h	8 bits left	7 bits left	–
1000 to 1111				8h - Fh	no shift	1 bit right	–

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6.6.7 AR14: Color Select Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 14

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Bit C [7]	0
2	Color Bit C [6]	0
1	Color Bit C [5]	0
0	Color Bit C [4]	0

This register contains two fields that are involved in the selection of addresses into the Color Lookup Table.

Bit	Description
7:4	Reserved
3:2	**Color Bits C [7:6]:** • In 8-, 16-, and 24-bit pixel modes, these bits are ignored. • These two bits are concatenated with the six bits from the Attribute Controller Palette Registers AR0 to ARF to form the address into the Color Lookup Table and to drive flat-panel interface pins FP[7:6].
1:0	**Color Bits C [5:4]:** • In 8-, 16-, and 24-bit pixel modes, these bits are ignored. • When AR10[7]: — is 0, these two bits are ignored. — is 1, these two bits replace the corresponding two bits from the Attribute Controller Palette Registers AR0 to ARF to form the address into the Color Lookup Table and to drive flat-panel interface pins FP[5:4].

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CL 28622

6.7 Extension Registers

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6.7.1 SR6: Unlock All Extensions Registers

I/O Port Address: 3C5

Index: 6

Bit	Description	Reset State
7	Not Used	x
6	Not Used	x
5	Not Used	x
4	Unlock All Extension Registers	1
3	Not Used	x
2	Unlock All Extension Registers	0
1	Unlock All Extension Registers	1
0	Unlock All Extension Registers	0

This register is used to enable or disable access to all Extension Registers.

Bit	Description
7:0	**Unlock All Extensions Registers (Access Value):** When the value of this field: • is xxx1x010: — The field will be read as 00010010. — Extension Registers will be unlocked (enabled) for read/write access. • is any other value: — The field will be read as 00001111. — Extension Registers will be disabled for read/write access.

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6.7.2 SR7: Extended Sequencer Mode Register

I/O Port Address: 3C5

Index: 7

Bit	Description	Reset State
7	Memory Segment Select [3]	0
6	Memory Segment Select [2]	0
5	Memory Segment Select [1]	0
4	Memory Segment Select [0]	0
3	Reserved	
2	Select CRTC Character Clock Divider [1]	0
1	Select CRTC Character Clock Divider [0]	0
0	Select High-Resolution Packed-Pixel Mode	0

This register has several purposes which are described in the following bit descriptions.

Bit	Description
7:4	**Memory Segment Select [3:0]:** • When this programmed field value is 0000: — the CL-GD7542 will be configured for standard VGA display memory addressing, responding to memory accesses at Axxx:x, or Bxxx:x, or both, as specified by GR6[3:2]. • When this programmed field value is other than 0000: — the CL-GD7542 will be configured for 1-Mbyte linear memory addressing. — the CL-GD7542 will respond to any memory access for which CPU address bits[23:20] match this field value. • When this programmed field value is other than 0000 *and*: — when there is a full one Mbyte of display memory installed, *and* the CL-GD7542 is configured for extended 256-color chain-4, then the 1-Mbyte address range will have one-to-one mapping to the one Mbyte of installed display memory, — when the CL-GD7542 is configured for unchained, x8, or x16 addressing, then it will respond to the entire 1-Mbyte range, but address wrapping will take place. — GRB[5] is programmed to a 1, then SR7[4] becomes a don't-care bit, and the CL-GD7542 will respond to a 2-Mbyte address.
3	Reserved

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6.7.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit **Description**

2:1 **Select CRTC Character Clock Divider [1:0]:**
This field selects how the CRTC Character Clock is divided down, as indicated in the following table:

SR7		CRTC Character Clock Divider Mode
[2]	[1]	
0	0	Normal operation
0	1	CRTC Character Clock ÷ 2 for 16 bit/pixel data
1	0	CRTC Character Clock ÷ 3 for 24 bit/pixel data
1	1	16 bit/pixel data at pixel rate (only)

CRTC Character Clock ÷ 2 for 16-Bit/Pixel Data:
When this mode is selected:
- the DAC and Video Shift Register are clocked at the VCLK data byte rate
- the CRTC is clocked with a character clock of 8 pixels (16 VCLKs)

The above clocking allows:
- the CRTC timing value for 640 x 480 modes and 800 x 600 modes with 16-bit pixels to be programmed in units of an 8-pixel character clock.
- Offset Register CR13 to be set to:
  - — A0h for 640 x 480 mode
  - — C8h for 800 x 600 mode
- The hardware cursor x-position to be set in pixel units.
- The Cursor Data Invert function to operate on 15-, 16-, or 18-bit RGB data presented to the DAC.

CRTC Character Clock ÷ 3 for 24-Bit/Pixel Data:
When this mode is selected:
- the DAC and Video Shift Register is clocked at the VCLK data byte rate
- the CRTC is clocked with a character clock of 8 pixels (24 VCLKs)

The above clocking allows:
- the CRTC timing value for 640 x 480 modes with 24-bit pixels to be programmed in units of an 8-pixel character clock.
- Offset Register CR13 Offset Register to be set to F0h.

The hardware cursor is not supported in this configuration.

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6.7.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit	Description
2:1 *(cont.)*	**Select CRTC Character Clock Divider [1:0]:** **16-Bit/Pixel Data at Pixel Rate:** When this mode is selected: • the sequencer will provide 16-bit data to the palette DAC at the displayed pixel rate. This action allows 5-5-5 or 5-6-5 color modes to be selected with a 1x VCLK. • The data at P[7:0] will be only the low-byte of the pixel data. (The high-byte of the pixel data is not available externally.) • This mode also provides for 1024 x 768 display modes, with 5-5-5 or 5-6-5 color, and with VCLK equal to the pixel rate.
0	**Select High-Resolution Packed-Pixel Mode:** When this bit is 1: • Video shift registers are configured so one character clock equals 8 pixels. • True packed-pixel memory addressing is enabled. • This mode may also be used with 16- and 24-bit pixel modes. (Refer to SR7[2:1].) • This mode may not be used with video mode 13, which is packed pixel, but not high resolution. For video mode 13, set AR10[6] = 1. Notes: *In true packed-pixel addressing, consecutive pixels are stored at consecutive addresses.* *In contrast, with chain-4 addressing, consecutive pixels are stored at every fourth address in display memory.*

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6.7.3 SR8: Miscellaneous Control

I/O Port Address: 3C5

Index: 8

Bit	Description	Access	Reset State
7(MSB)	Not Used	-	
6	Reserved	-	
5	Latch FCESYNC# and FCEVIDEO#	R/W	0
4	Reserved	-	
3	Reserved	-	
2	Reserved	-	
1	Reserved	-	
0(LSB)	Reserved	-	

Bit	Description
7	Not Used
6	Reserved
5	**Latch FCESYNC# and FCEVIDEO#:** When this bit is 1, the values on the FCESYNC# and FCEVIDEO# inputs are latched, so that the pins can be used for other functions.
4:0	Reserved

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6.7.4 SR9, SRA: Scratch Pad 0 and 1 Registers

I/O Port Address: 3C5

Index: 9, A

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

These two registers are reserved for the exclusive use of the CL-GD7542 BIOS and must never be written by any application program. They are listed here only for completeness.

Bit	Description
7:0	These bits are reserved for the Cirrus Logic, Inc., BIOS.

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6.7.5 SRB, SRC, SRD, SRE: VCLK0, 1, 2, 3 Numerator Registers

I/O Port Address: 3C5

Index: B, C, D, E

Bit	Description	Reset State
7	Reserved	
6	VCLK Numerator [6]	0
5	VCLK Numerator [5]	0
4	VCLK Numerator [4]	0
3	VCLK Numerator [3]	0
2	VCLK Numerator [2]	0
1	VCLK Numerator [1]	0
0	VCLK Numerator [0]	0

These registers, in conjunction with Extension Registers SR1B to SR1E, are used to determine the frequency of video clocks VCLKs. (For more information, refer to Appendix A7.)

Bit	Description
7	Reserved
6:0	**VCLK Numerator [6:0]:** The following table shows VCLK-related default values loaded at system reset. The default values are determined by the expression explained on the following page. (For more information on the VCLK denominator and post-scalar, refer to Extension Registers SR1B to SR1E.)

Table 6–2. VCLK Numerator, Denominator, and Post-scalar Values

VCLKi and Frequency		VCLK Numerator Values			DCLK Numerator Values			
VCLKi	VCLKi Frequency	Numerator Register and Hex Value in Register		*NB* = Value Used in Equation Numerator	Denominator Register and Hex Value in Register		*DB* = Value Used in Equation Denominator, Resulting from Post-Scalar	*P* = Post-Scalar Value Used in Equation Denominator
	MHz	Register	Hex	Decimal Equivalent of Hex Value	Register	Hex	Decimal	Decimal
VCLK0	25.180	SRB	66h	102	SR1B	3Bh	29	1
VCLK1	28.325	SRC	5Bh	91	SR1C	2Fh	23	1
VCLK2	41.165	SRD	45h	69	SR1D	30h	24	0
VCLK3	36.082	SRE	7Eh	126	SR1E	19h	25	1

Continued on next page.

6.7.5 SRB, SRC, SRD, SRE: VCLK0, 1, 2, 3 Numerator Registers *(cont.)*

Bit	Description
6:0 *(cont.)*	**VCLK Numerator [6:0]:**

Each Video Clock frequency is determined by the following expression:

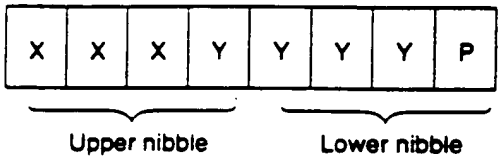
$$\text{VCLK i (MHz)} = \frac{\text{OSC} \times \text{NR}}{\text{DR} \times [\text{P} + 1]}$$

Where:

VCLK i	= Video Clock i, where i = 0, 1, 2, 3
OSC	= Input Clock, 14.31818 MHz
Numerator Register	= Value of Register SRi [6:0], where i = B, C, D, E
Denominator Register	= Value of Register SR1i [5:1], where i = B, C, D, E
Post-scalar	= Value of Register SR1i [0], where i = B, C, D, E

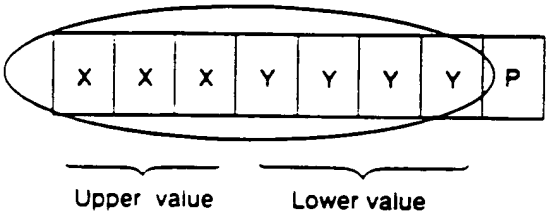
The DR denominator value is determined as follows:

1. The hex value programmed in the appropriate denominator register is read.



Hex number read:
Upper nibble = Values in XXXY.
Lower nibble = Values in YYY, plus post-scalar P = YYYP.

2. To extract a value to be used in the equation, the post-scalar value is ignored, which has the effect of shifting all values in the register to the right.



Circled area is what is actually used in the equation.
Upper value = Values in XXX. Lower value = Values in YYYY.

3. The value that is extracted is converted to decimal and plugged into the equation, along with P, the post-scalar value, which is obtained from Table 6–2.

6.7.6 SRF: DRAM Control Register

I/O Port Address: 3C5

Index: F

Bit	Description	Reset State
7	DRAM Bank Select	0
6	Disable CPU-Write FIFO Fast-Page-Detection Mode	0
5	CRT FIFO Depth Control	0
4	Display Memory Data Bus Width [1]	0
3	Display Memory Data Bus Width [0]	0
2	DRAM RAS Timing	0
1	Reserved	0
0	Multiple-CAS# / Multiple-WE# DRAM Select	1

This register is used to control the display memory.

Bit	Description
7	**DRAM Bank Select:** • This bit is used with SRF[4:3] to specify the display memory data bus width according to the number of banks of display memory used. • When this bit: — is 1, the CL-GD7542 is configured for two banks of display memory (four 256K x 16 DRAMs). — is 0, the CL-GD7542 is configured for one bank of display memory (four 512K x 8 DRAMS, or two 256K x 16 DRAMs).
6	**Disable CPU-Write FIFO Fast-Page-Detection Mode:** • To avoid CPU write buffer under-runs, this bit *must* be programmed to 1, either when loading font data for page-mode font access, or when performing multiple color-expand writes in 16-bit pixel modes. • When this bit: — is 1, CPU writes to display memory will take place as random cycles. — is 0, consecutive CPU writes to display memory are executed as Fast-page Mode writes, whenever possible.
5	**CRT FIFO Depth Control:** When this bit is 0 (the default): • The CRT write buffer depth is set to 8 levels (32 bits/level). • This setting is typically used for standard video modes and for extended 16-color modes. When this bit is 1: • The CRT write buffer depth is set to 16 levels (64 bytes). • This setting is typically used for any 16-bit or 24-bit pixel modes and for extended 8-bit pixel modes. This setting should never be used for any text mode.

Continued on next page.

6.7.6 SRF: DRAM Control Register *(cont.)*

Bit **Description**

4:3 **Display Memory Data Bus Width [1:0]:**
This two-bit field is used with SRF[7] to specify the display memory data bus width according to the following table:

SRF			Display Memory Data Bus Width	Memory Organization	Total Memory
[7]	[4]	[3]			
0	0	0	—	Reserved	Reserved
0	0	1	—	Reserved	Reserved
0	1	0	32 Bit	Two 256K x 16 DRAMs	1 MByte
				Four 512K x 8 (symmetric) DRAMs	2 MBytes
0	1	1	—	Reserved	Reserved
1	1	0	32 Bit	Four 256K x 16 DRAMs (two banks)	2 MBytes
111			—	Reserved	Reserved

These bits have one level of buffering. At the end of each horizontal scanline refresh interval, when horizontal blanking begins, the state of each of these bits is transferred to the timing logic. This transfer avoids changing the timing logic in mid-scanline.

2 **DRAM RAS Timing:**
This bit indicates the DRAM row-address strobe timing as summarized in the following table.

SRF[2]	Timing for RAS high	Timing for RAS low	Note
0	3 MCLK	4 MCLK	Extended RAS (default)
1	2.5 MCLK	3.5 MCLK	Standard RAS

The default is extended RAS timing, which fits all DRAMs. However, in order to achieve optimal performance, the timing selected should match the MCLK.

1 Reserved

0 **Multiple-CAS# / Multiple-WE# DRAM Select:**
- A 0 selects multiple-WE# 256 x 16-bit DRAM support.
- A 1 selects multiple-CAS# DRAM support, which is the default.

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6.7.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position

I/O Port Address: 3C5

Index: 10, 30, 50, 70, 90, B0, D0, F0

Bit	Description	Reset State
7	HW Cursor and HW Icon Coarse Horizontal Position [10]	0
6	HW Cursor and HW Icon Coarse Horizontal Position [9]	0
5	HW Cursor and HW Icon Coarse Horizontal Position [8]	0
4	HW Cursor and HW Icon Coarse Horizontal Position [7]	0
3	HW Cursor and HW Icon Coarse Horizontal Position [6]	0
2	HW Cursor and HW Icon Coarse Horizontal Position [5]	0
1	HW Cursor and HW Icon Coarse Horizontal Position [4]	0
0	HW Cursor and HW Icon Coarse Horizontal Position [3]	0

This register, and bits SRX[7:5] of the index that is used to access it, is used to define in character clocks the coarse horizontal (X) pixel offset of the graphics hardware cursor and icon. For more information on the hardware cursor and icon, refer to Appendices A2 and A3.

For all 8-bit text modes and non-expanded graphics modes and text modes which do not require the fourth expansion bit, the entire 12-bit cursor or icon horizontal position can be written in a single 16-bit I/O write as follows:

- The expansion bits in SR2A[6] and SR2E[0], which are cleared to 0, are ignored.
- The offset must be placed in AX[15:5].
- AX[4:0] must be 10000.
- DX must be 3C4h.

When 10, 30, 50...F0 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 will return the previously stored three bits of the cursor or icon position.

Note: Changes programmed in SR10 do not take effect until SR11 has been written.

Bit	Description
7:0	**Cursor and Icon Horizontal Position [10:3]:** SR12[3] selects whether the value in this register refers to the hardware cursor or the hardware icon. Cursor 12-bit Horizontal Position • When SR12[3] = 0, the hardware cursor is selected. • SR10[7:0] are the upper 8 coarse-position bits. • SRX[7:5] are the lower 3 fine-position bits, defined in dot clocks. • SR2E[0] extends the cursor fine position by one msb for horizontally expanded graphics modes. This extra bit is valid only with a 10-dot character clock. • The hardware cursor is not available in text modes and mode 13.

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6.7.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position *(cont.)*

Bit	Description
7:0*(cont.)*	**Cursor and Icon Horizontal Position [10:3]:**

Icon 12-bit Horizontal Position

- When SR12[3] = 1, the hardware icon is selected.
- SR10[7:0] form the upper-eight bits of the 11-bit icon horizontal offset.
- SRX[7:5] form the lower-three bits of the 11-bit icon horizontal offset.
- SR2A[6] is the fourth bit of a dot-clock-level delay in expanded-graphics modes and in text modes with 9-dot or 10-dot fonts.
- The icon is supported in all modes, except interlaced, 24 bpp with 3X clock, and 16 bpp with 2X clock. (The latter does not support horizontal doubling.)

To program the horizontal position of the hardware icon:

- Place the icon hot point (top left) at pixel n (with 0 as the first pixel).
- Program the coarse position as: Integer [(n ÷ (k-1)) ÷ k].
  (k = the number of dots in a character clock.)
- Program the fine position as: Remainder [(n ÷ (k-1)) ÷ k].

For example, to place the icon:

- at pixel 10, which is 11 pixels from the left (n = 10)
- with an 8-dot character clock, as in graphics mode 12 (k = 8)

Program:

- the coarse position as = Integer [(10 ÷ (8 - 1)) ÷ 8] = Integer [17 ÷ 8] = 2h
- the fine position as = Remainder [17 ÷ 8] = 1h

An example of programming for an 8-dot character clock is given in the table below.

Pixel Position	Position Programmed	
	Coarse.	Fine
0	0	7
1	1	0
2	1	1
3	1	2
4	1	3
5	1	4
6	1	5
7	31	6
8	1	7
9		0
10	2	1

There are only three cases of character clock width.

- 10 dots – used for text and graphics expansion on 800 x 600 LCD
- 9 dots – used for text on 800 x 600 LCDs, when 720 dots are displayed
- 8 dots – used in all other cases

6.7.8 SR11: Hardware Cursor and Hardware Icon Coarse Vertical Position

I/O Port Address: 3C5

Index: 11, 31, 51, 71, 91, B1, D1, F1

Bit	Description	Reset State
7	HW Cursor and HW Icon Coarse Vertical Position [10]	0
6	HW Cursor and HW Icon Coarse Vertical Position [9]	0
5	HW Cursor and HW Icon Coarse Vertical Position [8]	0
4	HW Cursor and HW Icon Coarse Vertical Position [7]	0
3	HW Cursor and HW Icon Coarse Vertical Position [6]	0
2	HW Cursor and HW Icon Coarse Vertical Position [5]	0
1	HW Cursor and HW Icon Coarse Vertical Position [4]	0
0	HW Cursor and HW Icon Coarse Vertical Position [3]	0

This register, and bits SRX[7:5] of the index that is used to access it, is used to define in scanlines the coarse vertical (Y) scanline offset of the graphics hardware cursor and icon. For more information on the hardware cursor and icon, refer to Appendices A2 and A3.

The entire 11-bit cursor or icon vertical position can be written in a single 16-bit I/O write as follows:

- The offset must be placed in AX[15:5].
- AX[4:0] must be 10001.
- DX must be 03C4.

When 10, 30, 50...F1 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 will return the previously stored three bits of the cursor or icon position.

Bit	Description
7:0	**Cursor and Icon Vertical Position [10:3]:** SR12[3] selects whether the value in this register refers to the hardware cursor or the hardware icon. Cursor and Icon 11-bit Vertical Position • When SR12[3]: — is 0, the hardware cursor is selected. — is 1, the hardware icon is selected. • SR11[7:0] are the upper 8 coarse-position bits. • SRX[7:5] are the lower 3 fine-position bits, defined in scanlines

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6.7.9 SR12: Video Data Path Control Register

I/O Port Address: 3C5

Index: 12

Bit	Description	Reset State
7	Overscan Color Protect	0
6	Tri-State All Display Memory Pins	0
5	VCLK = VCO ÷ 4	0
4	MCLK = MVCO ÷ 2	0
3	Hardware Icon and Hardware Cursor Position Modification	0
2	Cursor Pixel Size Select	0
1	CPU Access to DAC Extended Colors	0
0	Graphics Hardware Cursor Enable	0

This register is used to enable or disable 4-bit packed-pixel addressing on the CL-GD7542.

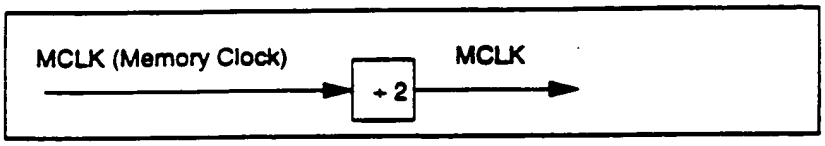
Bit	Description
7	**Overscan Color Protect:** When this bit: • is 1, the overscan color comes from the hidden DAC register (the 16-cell RAMDAC RAM extension.) As a result, the border color is locked to a value dictated by the enviromental requirements, and it cannot be changed by the application. • is 0, the overscan color comes from AR11[5:0].
6	**Tri-State All Display Memory Pins:** • When this bit is 0, all display memory pins operate normally. • When this bit is 1, all display memory pins are forced to a tri-stated high-impedance off state. The display memory pins can then be multiplexed for use with another graphics controller.
5	**VCLK = VCO ÷ 4:** When this bit is 1, the video clock (VCLK) signal is derived from the voltage-controlled oscillator (VCO) frequency divided by four. • This bit must be used to get VCLK frequencies of 20MHz or less. For example, to get 20 MHz: — Program VCO for 80 MHz. — Set SR12[5] = 1, which divides the VCO signal by four. — As a result, VCLK = 20 MHz. • This bit is useful in 5V Core-VDD systems where at low frequencies, the VCO frequency range is not good enough. (Note that SR1B through SR1E[0] is VCLK divided by two). While the VCO is within its operating range, as appropriate for the desired VCLK frequency, divide by 2 or by 4.

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6.7.9 SR12: Video Data Path Control Register *(cont.)*

Bit	Description
4	**MCLK = MCLK ÷ 2:** When this bit: • is 1, the memory clock (MCLK) signal is derived by dividing by two the original memory clock signal (which is the MVCO, the memory voltage-controlled oscillator).  • is 0, the memory clock is not divided by 2. In this case, the clock that is used as the memory clock is the same frequency as the MVCO.  • This bit may is used to get MCLK frequencies outside the memory VCO frequency range for a given Core VDD value and frequency.
3	**Hardware Icon and Hardware Cursor Position Modification:** This bit selects whether the CPU can modify the position (both horizontal and vertical) of either the hardware icon or the hardware cursor. The same registers are used to modify both hardware icon and hardware cursor position. • When this bit is 0, the CPU can modify the hardware cursor position. • When this bit is 1, the CPU can modify the hardware icon position. • This bit does not affect SR2A[6] or SR2E[0], which are always accessible by the CPU.
2	**Cursor Pixel Size Select:** • When this bit is 0, the 32 x 32 pixel hardware cursor is selected. • When this bit is 1, the 64 x 64 pixel hardware cursor is selected.
1	**CPU Access to DAC Extended Colors:** • When this bit is 0, the CPU accesses the standard VGA 256 x 18 Color Lookup Table. • When this bit is 1, the CPU accesses the DAC extended colors, which are 16 additional 18-bit wide RAMDAC RAM locations. — Some locations have a specific purpose, such as hardware cursor colors (2 locations), hardware icon colors (4 locations), and border color (1 location). — Other locations are not used, or can be used as scratch registers by the BIOS and drivers.

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6.7.9 SR12: Video Data Path Control Register *(cont.)*

Bit **Description**

1 *(cont.)* **CPU Access to DAC Extended Colors (cont.):**
The address map for the DAC extended colors is given in the following table:

I/O Address	Physical RAM Location	Function
X0h	256	Hardware cursor back-ground color
XFh	257	Hardware cursor foreground color
X2h	258	Fix color of overscan (the border)
X3h	259	Hardware icon color #0. (This function is not used, if in 3 colors + transparent mode.)
X4h	260	Hardware icon color #1
X5h	261	Hardware icon color #2
X6h	262	Hardware icon color #3
XD, XE	269, 270	Used by Video BIOS

0 **Graphics Hardware Cursor Enable:**
When this bit is 1, the graphics hardware cursor is enabled.

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6.7.10 SR13: Graphics Cursor Pattern Address Offset Register

I/O Port Address: 3C5

Index: 13

Bit	Description	Reset State
7	Not Used	
6	Not Used	
5	Reserved	
4	Cursor Pattern Select [4]	0
3	Cursor Pattern Select [3]	0
2	Cursor Pattern Select [2]	0
1	Cursor Pattern Select [1] / Reserved	0
0	Cursor Pattern Select [0] / Reserved	0

This register is used to select:

- one of 32 possible cursor patterns for the 32 x 32 cursor
- one of 8 possible cursor patterns for the 64 x 64 cursor

For a complete programming guide for the graphics hardware cursor, refer to Appendix A2.

Bit	Description
7:6	Not Used
5	Reserved
4:0	**Cursor Pattern Select (32 x 32 Cursor):** When SR12[2] is 0: • This 5-bit field can select 1 of 32 cursor patterns for the 32 x 32 cursor. • The patterns are stored in 8 Kbytes of the top 32 Kbytes of display memory.
4:2	**Cursor Pattern Select (64 x 64 Cursor):** When SR12[2] is 1: • This 3-bit field can select 1 of 8 cursor patterns for the 64 x 64 cursor. • The patterns are stored in 8 Kbytes of the top 32 Kbytes of display memory.
1 0	Reserved, when SR12[2] = 1.

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6.7.11 SR14, SR15: Scratch Pad 2, 3 Registers

I/O Port Address: 3C5

Index:14, 15

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

These two registers are reserved for the exclusive use of the CL-GD7542 BIOS and must never be written by any application program. They are listed here only for completeness.

Bit	Description
7:0	These bits are reserved for the Cirrus Logic, Inc., BIOS.

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6.7.12 SR16: Performance Tuning Register

I/O Port Address: 3C5

Index:16

Bit	Description	Reset State
7	Extra Wait State for Fast VL Bus	1
6	RDY# Delay for I/O	1
5	RDY# Delay for Memory Write [1]	1
4	RDY# Delay for Memory Write [0]	1
3	FIFO Demand Threshold [3]	0
2	FIFO Demand Threshold [2]	0
1	FIFO Demand Threshold [1]	0
0	FIFO Demand Threshold [0]	0

This register is used to control the delay from ADS# to RDY#, and to control the threshold at which the CRT FIFO will be refilled. This register must never be written by an application program. It is listed here for completeness only.

Bit **Description**

7 **Extra Wait State for Fast VL Bus:**

- When this bit is 1, and when the CL-GD7542 is configured for the VL bus, one extra wait state is added to both I/O and memory accesses.
- This bit must be 1 if the bus clock is fast, compared to the memory clock.
- In conjunction with the state of SR16[6], this bit controls the CPU1X clock delay from ADS# to RDY# for I/O cycles.
- For further explanation, refer to the tables in SR16[6] and SR16[5:4].

6 **RDY# Delay for I/O:**

- This field applies only when the CL-GD7542 is configured for local bus.
- In conjunction with the state of SR16[7], this bit controls the CPU1X clock delay from ADS# to RDY# for read/write I/O cycles.
- The following table summarizes the values:

SR16		CPU1X Clock Delay
[7]	[6]	
0	0	1
0	1	2
1	0	2
1	1	3 (Default)

Continued on next page.

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6.7.12 SR16: Performance Tuning Register *(cont.)*

Bit **Description**

5:4 **RDY# Delay for Memory Write [1:0]:**

- This field is used to control the delay from ADS# to RDY# for memory write cycles.
- This field applies only when the CL-GD7542 is configured for local bus.
- The table below summarizes values that may be programmed into this field. The value programmed must satisfy the following inequality:
  [(2 + value of bits 7,5,4) x CPU Clock Period] ≥ [(3 x MCLK Period) + 2 ns]

SR16			CPU1X Clock Delay
[7]	[5]	[4]	
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	3
1	0	1	4
1	1	0	5
1	1	1	6 (Default)

3:0 **FIFO Demand Threshold [3:0]:**

- The value written to this field will select the level at which the CL-GD7542 sequencer will begin cycles to refill the CRT FIFO (and thereby hold off CPU cycles).
- For each video mode and MCLK frequency, there will be an optimum value that will use the DRAM most efficiently.

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6.7.13 SR18: Signature Generator Control Register

I/O Port Address: 3C5

Index:18

Bit	Description	Reset State
7	LCD Signature Generator Enable	0
6	Reserved	
5	Reserved	
4	Pixel Bus Bit Select [2]	0
3	Pixel Bus Bit Select [1]	0
2	Pixel Bus Bit Select [0]	0
1	Reset Signature Generator	0
0	Signature Generator Enable / Status	0

This register is used to control and monitor the status of the CL-GD7542 signature generator, which is used for board-level testing of the video sub-system. For a complete description of the signature generator, refer to Appendix A10.

Bit	Description
7	**LCD Signature Generator Enable:** When this bit is 1, the LCD signature generator is enabled.
6	Reserved
5	Reserved
4:2	**Pixel Bus Bit Select [2:0]:** This field is used to select the Feature Connector Pixel Bus bit that will be used as the input for the signature generator according to the following table:

SR18			Feature Connector Pixel Bus Bit
[4]	[3]	[2]	
0	0	0	FCP[0]
0	0	1	FCP[1]
0	1	0	FCP[2]
0	1	1	FCP[3]
1	0	0	FCP[4]
1	0	1	FCP[5]
1	1	0	FCP[6]
1	1	1	FCP[7]

Continued on next page.

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6.7.13 SR18: Signature Generator Control Register *(cont.)*

Bit	Description
1	**Reset Signature Generator:** • When this bit is 1, the signature generator is reset to an initial, defined condition. • When this bit is 0, the signature generator is allowed to run under the control of SR18[0].
0	**Signature Generator Enable / Status:** • When this bit is 1, the signature generator is enabled and begins operation on the next VSYNC. From the Feature Connector Pixel Bus bit chosen by SR18[4:2], the signature generator accumulates a signature for one video frame and then stops, forcing this bit to 0. • By monitoring the status of this bit, the program can determine when the signature is complete.

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6.7.14 SR19: Signature Generator Result Low Byte Register

I/O Port Address: 3C5

Index: 19

Bit	Description	Reset State
7	Signature Generator Result [7]	0
6	Signature Generator Result [6]	0
5	Signature Generator Result [5]	0
4	Signature Generator Result [4]	0
3	Signature Generator Result [3]	0
2	Signature Generator Result [2]	0
1	Signature Generator Result [1]	0
0	Signature Generator Result [0]	1

For a complete description of the signature generator, refer to Appendix A10.

Bit	Description
7:0	**Signature Generator Result [7:0]:** This register is used to read the low-order byte of the CL-GD7542 signature generator result.

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6.7.15 SR1A: Signature Generator Result High Byte Register

I/O Port Address: 3C5

Index: 1A

Bit	Description	Reset State
7	Signature Generator Result [15]	0
6	Signature Generator Result [14]	0
5	Signature Generator Result [13]	0
4	Signature Generator Result [12]	0
3	Signature Generator Result [11]	0
2	Signature Generator Result [10]	0
1	Signature Generator Result [9]	0
0	Signature Generator Result [8]	0

For a complete description of the signature generator, refer to Appendix A10.

Bit	Description
7:0	**Signature Generator Result [15:8]:** This register is used to read the high-order byte of the CL-GD7542 signature generator result.

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6.7.16 SR1B,SR1C,SR1D,SR1E: Denominator/Post-scalar for VCLK 0,1,2,3

I/O Port Address: 3C5

Index: 1B, 1C, 1D, 1E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	VCLK Denominator [4]	Note a
4	VCLK Denominator [3]	Note a
3	VCLK Denominator [2]	Note a
2	VCLK Denominator [1]	Note a
1	VCLK Denominator [0]	Note a
0	VCLK Post-Scalar	Note a

Note a. The reset values for the VCLK Numerator for these four registers are shown in Table 6–2, "VCLK Numerator, Denominator, and Post-scalar Values," on page 207.

These registers, in conjunction with SRB, SRC, SRD, and SRE, are used to determine the frequency of video clock 0 (VCLK0), etc. For complete programming information for the synthesizers, refer to Appendix A7.

Bit	Description
7:6	Reserved
5:1	**VCLK Denominator (D) [4:0]:** Refer to Table 6–2, "VCLK Numerator, Denominator, and Post-scalar Values," on page 207 for detailed explanation of the VCLK derivation.
0	**VCLK Post-Scalar (P):** Refer to Table 6–2, "VCLK Numerator, Denominator, and Post-scalar Values," on page 207 for detailed explanation of the VCLK derivation.

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6.7.17 SR1F: MCLK Frequency and VCLK Source Select Register

I/O Port Address: 3C5

Index: 1F

Bit	Description	Reset State
7	Not Used	
6	VCLK Source Select	0
5	MCLK Frequency [5]	(Refer to MCLK Table below)
4	MCLK Frequency [4]	(Refer to MCLK Table below)
3	MCLK Frequency [3]	(Refer to MCLK Table below)
2	MCLK Frequency [2]	(Refer to MCLK Table below)
1	MCLK Frequency [1]	(Refer to MCLK Table below)
0	MCLK Frequency [0]	(Refer to MCLK Table below)

This register is used to program the MCLK frequency. This register should never be programmed by an applications program. It is listed here only for completeness.

Bit **Description**

7 Not Used.

6 **VCLK Source Select:**

- When this bit is 0, the VCLK synthesizer operates normally.
- When this bit is 1, VCLK is derived from MCLK as follows:

SR1F[6]	SR1E[0]	VCLK Source
0	X	VLCK (Normal Operation)
1	0	VCLK = MCLK
1	1	VCLK = MCLK ÷ 2

5:0 **MCLK Frequency [5:0]:**

- To directly program the MCLK frequency, use the following equation: MCLK = (Reference Frequency ÷ 8) x SR1F[5:0]
- This field may be programmed with values from 21 to 38 (decimal).
- The following table assumes a reference frequency of 14.31818 MHz.

SR1F[5:0] (Decimal)	SR1F[5:0] (Hex)	Resulting MCLK Frequency
21	15h	37.585 MHz
23	17h	41.165 MHz
24	18h (default, at-reset value)	42.955 MHz
25	19h	44.744 MHz
26	1Ah	46.534 MHz
28	1Ch	50.114 MHz

- For information on DRAM requirements for MCLK frequencies, refer to Appendix A6

6.7.18 SR20: Miscellaneous Control 2

I/O Port Address: 3C5

Index: 20

Bit	Description	Reset State
7(MSB)	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	DRAM Interface-Input Threshold Select	0
0(LSB)	CPU Bus Interface-Input Threshold Select	0

This register is reserved exclusively for the CL-GD7542 BIOS and must never be written by an application program. It is listed here only for completeness.

Bit	Description
7:2	Reserved
1	**DRAM Interface-Input Threshold Select:** • When this bit is 0, DRAM interface-input thresholds are at TTL levels. • When this bit is 1, DRAM interface-input thresholds are at CMOS levels.
0	**CPU Bus Interface-Input Threshold Select:** • When this bit is 0, CPU bus interface-input thresholds are at TTL levels. • When this bit is 1, CPU bus interface-input thresholds are at CMOS levels.

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6.7.19 SR21: Dual-Scan Color Control

I/O Port Address: 3C5

Index: 21

Bit	Description	Reset State
7(MSB)	Refresh Per Line Select	0
6	Dual-Scan STN Color STN Select	0
5	Reserved	
4	Graphics Hardware Cursor-Size Select	0
3	Reserved	
2	Reserved	
1	Reserved	
0(LSB)	Reserved	

The SR21[7,6,4] bits are user programmable for the CL-GD7542. The SR21[3:0] bits are reserved for manufacturing testing and must never be written by an application program.

Bit	Description
7	**Refresh Per Line Select:** • When this bit is 1, one refresh cycle per scanline is selected. • When this bit is 0 (the default), CR11[6] selects either three or five refresh cycles per scanline.
6	**Dual-Scan STN Color Select:** CR2C[7:6] must be programmed to 10 to select STN color LCDs. When CR2C[7:6] = 10 and this bit: • = 1, dual-scan STN color mode is selected. • = 0, single-scan STN color mode is selected.
5	Reserved
4	**Graphics Hardware Cursor-Size Select:** When SR12[0] is 1 and: • this bit is 1, the 64 x 64-bit hardware cursor is selected. • this bit is 0, the 32 x 32-bit hardware cursor is selected. For hardware cursor pattern choices, refer to SR13[4:0].
3.0	Reserved for testing only.

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6.7.20 SR22: Hardware Configuration Read Register 1

I/O Port Address: 3C5

Index: 22

Bit	Description	Access	Reset State
7	PCI Minimum Grant	R	= MD[23]
6	Reserved	R	
5	Sleep Address Select	R	= MD[21]
4	Reserved		
3	External Clock Select	R	= MD[19]
2	Select VESA Local Bus > 33MHz	R	= MD[18]
1	Reserved		
0	Select 32-Bit PCI Bus	R	= MD[16]

This register contains a read-only field that allows the BIOS to determine configuration information for bus type, sleep address, and external clock by reading the level on the indicated MD pins during the low-to-high transition of the Reset pulse.

- All these MD pins have pull-down resistors internally, and so the default readings are all 0.
- An external 60 k-ohm pull-up resistor is needed to establish a high (1) on these pins.

Bus-select bits SR22[7,2,0] are mutually exclusive. Only *one* can be high at any time.

- If there are no external pull-ups on SR22 bus-select bits 7, 2, and 0, the CL-GD7542 will be configured for VESA local bus operation ≤ 33MHz.
- If there are no external pull-ups on *any* of the SR22 bus-select bits, the CL-GD7542 will be configured for VESA local bus operation ≤ 33MHz. In addition, the CL-GD7542 will be configured with internal clock synthesizers and a sleep address of 3C3h.

Bit	Description
7	**PCI Minimum Grant:** • An external pull-up on PCI-MGE / MD[23] reads back a 1. In this case: — The PCI burst cycle to the CL-GD7542 must be a minimum of 16 CPU clock cycles. — PCI Configuration Register 3Ch, offset 2 will read back a 1, allowing the PCI core logic to detect the presence of the pull-up resistor. — The CL-GD7542 expects a default minimum grant value of 8 bus clocks. — A pull-up should not be used on PCI / MD[16], as only one PCI bus external configuration pull-up should be used (either PCI-MGE or PCI). • No external pull-up on PCI-MGE / MD[23] reads back a 0. Inthis case: — The PCI burst cycle to the CL-GD7542 will be 8 CPU clock cycles. — PCI Configuration Register 3Ch, offset 2 will read back a 0. • Normally, no pull-up is required on PCI-MGE / MD[23] .

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6.7.20 SR22: Hardware Configuration Read Register 1 *(cont.)*

Bit	Description
6	Reserved
5	**Sleep Address Select:** • An external pull-up on S46 / MD[21] reads back a 1, which selects I/O address 46E8h as the sleep address. • No external pull-up on S46 / MD[21] reads back a 0, indicating the selection of sleep address 3C3h, the default.
4	Reserved
3	**External Clock Select:** • An external pull-up on XCLK/ MD[19] reads back a 1, powering down the internal clock for MCLK and VCLK, and enabling the external XMCLK and XVCLK clock inputs. (This external pull-up is used for manufacturing test and for logic simulations by Cirrus Logic.) • No external pull-up on XCLK/ MD[19] reads back a 0, so that the internal clock MCLK and VCLK are used by default.
2	**Select VESA Local Bus > 33MHz:** • An external pull-up on FVL / MD[18] reads back a 1, selecting a fast VESA local bus operation at > 33MHz. • No external pull-up on FVL / MD[18] reads back a 0, selecting a VESA local bus operation ≤ 33MHz.
1	Reserved
0	**Select 32-bit PCI Bus:** • An external pull-up on PCI / MD[16] reads back a 1, configuring the CL-GD7542 for 32-bit PCI bus operation. • No external pull-up on PCI / MD[16] reads back a 0, configuring the CL-GD7542 for VESA local bus operation ≤ 33MHz.

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6.7.21 SR23: Software Configuration Register 1

I/O Port Address: 3C5

Index:23

Bit	Description	Reset State
7	Enable FCVCLK	0
6	ACTI / FCEVIDEO# / SBYI Select	0
5	BLI / SUSPI Select	0
4	VCLK Output Enable	0
3	Reserved	0
2	48-KByte BIOS Decode Select	0
1	Reserved	
0	Reserved	

This register contains a read-only field that allows for miscellaneous configurations.

Bit	Description
7	**Enable FCVCLK:** A 1 in this bit enables the FCVCLK input to drive either the RAMDAC or the video clock (VCLK), depending on the state of External/General Register MISC[3]. When SR23[7] = 1: • *and* MISC[3] = 0, FCVCLK is sent only to the RAMDAC, enabling only that part of the CL-GD7542. • *and* MISC[3] = 1, FCVCLK is used for to drive VCLK, which clocks the entire CL-GD7542. • *and* there is a high on TVON, the TVON high signal forces MISC[3] to 1. In this case also, FCVCLK is used to drive VCLK, which clocks the entire CL-GD7542.
6	**ACTI / FCEVIDEO# / SBYI Select:** When SR24[7] = 0: • *and* this bit is 0, the ACTI / FCEVIDEO# / SBYI pin is configured as the hardware-controlled Standby input. • *and* this bit is 1, the ACTI / FCEVIDEO# / SBYI pin is configured as the Activity sense input to reset the power-down timers. When SR24[7] = 1: • the ACTI / FCEVIDEO# / SBYI pin is always FCEVIDEO#, independent of the SR23[6] value.
5	**BLI / SUSPI Select:** When this bit: • is 0, the BLI / SUSPI pin is configured for hardware-controlled Suspend input. • is 1, and SR24[7] = 0, the BLI / SUSPI pin is configured for Backlight Input control.

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6.7.21 SR23: Software Configuration Register 1 *(cont.)*

Bit	Description
4	**VCLK Output Enable:** • When this bit is 0 (the default), the VCLK output is low. • When this bit is 1, the internal VCLK is available for testing on the VCLK / FCDCLK pin, independent of SR22[3] (the external/internal clock selection). Note: When SR24[7] = 1, the internal VCLK is also available on the FCDCLK output.
3	Reserved
2	**48-KByte BIOS Decode Select:** When BIOS is enabled: • A 0 in this bit selects 32-KByte BIOS decode. • A 1 in this bit selects 48-KByte BIOS decode.
1:0	Reserved

6.7.22 SR24: LCD Type Switches and FC Enable

I/O Port Address: 3C5

Index:24

Bit	Description	Reset State
7	Feature Connector External Pull-up Video Port Enable	FC Pull-up
6	Reserved	
5	Fast 16-Bit CPU Bus Access Enable	0
4	FCDCLK Output Select	0
3	External Pull-Up Read under Software Control	0
2	SW2 Pin Read	Switch Value
1	SW1 Pin Read	Switch Value
0	SW0 Pin Read	Switch Value

Bit	Description
7	**Feature Connector External Pull-up Video Port Enable:** • An external pull-up resistor on FC / MD25 configures all appropriate pins for the Feature Connector Video Port. (Refer to pin descriptions in Chapter 2.) • When no pull-up is used, these pins revert to their other functions or are disabled (that is, inputs are ignored and outputs are high impedance).
6	Reserved
5	**Fast 16-Bit CPU Bus Access Enable:** • When this bit is 0, the RDY# / TRDY# output is delayed for 16-bit accesses by one bus-clock cycle to minimize bus contention problems. • When this bit is 1, the clock delay is removed, which allows faster bus access. This bit works with both the VESA local bus and the PCI bus.
4	**FCDCLK Output Select:** This bit is used to select the clock that appears on the FCDCLK pin. • When this bit is 1: — The selection is the VCLK VCO output clock. — Even if SR23[7] = 1, the internal VCLK clock synthesizer outputs the internal clock to the VCLK output pin. This configuration is used with the Feature Connector for video overlay. • When this bit is 0, the selection is PCLKO, which is a dot clock that SR1[3] does *not* divide by 2.
3	**External Pull-Up Read Under Software Control:** • This bit is used to restore operation: — when total graphics controller power-off is used. — when the Reset pulse is too short to read the switches which have large pull-up or pull-down resistance. • This bit is programmed first to a 1 then to a 0. Configuration inputs are read on the 1-to-0 transition of this bit. By toggling this bit, configuration pins can be read and latched at any time, not just at Reset.

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6.7.22 SR24: LCD Type Switches and FC Enable *(cont.)*

Bit	Description
2:0	**SW2 to SW0 Pin Read:** These read-only bits reflect the active level of switch inputs SW2 to SW0. • These bits are read continuously during normal operation, and are not affected by SR24[3]. • These bits are normally for BIOS use.

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6.7.23 SR25: Timer-Software Reset and Hardware Configuration #2

I/O Port Address: 3C5

Index:25

Bit	Description	Reset State
7	Reserved	
6	External RAMDAC Address / Chip Select	0
5	Enable 1-bit/pixel Packed-Pixel Mode	0
4	Enable External XVCLK Input	0
3	Enable 4-bit/pixel Packed-Pixel Mode	0
2	Reserved	
1	Reset Standby Timer	0
0	Reset Backlight Timer	0

Bit	Description
7	Reserved
6	**External RAMDAC Address / Chip Select:** • When this bit is 0, the TVON pin is controlled by Extension Register CR30[3]. • When this bit is 1: — The TVON output becomes the external RAMDAC Chip Select. At system reset, both the TVON and RAMDAC Select functions are inactive low. As a result, no matter how the chip comes up, external RAMDAC is not affected. — It disables the internal DAC and RAMDAC RAM I/O readback. The RAM continues to be updated by RAMDAC writes, but it does not respond to any RAMDAC read except 3C7. — In VL bus mode, the CL-GD7542 does not assert LDEV# and RDY. — In PCI bus mode, the CL-GD7542 does not support external RAMDAC related to I/O select or shadowing. • This bit must be set to 1, *before* TV-OUT feature is enabled (CR30[3] = 1), to ensure that the TVON pin becomes the external RAMDAC Chip Select.
5	**Enable 1-bit/pixel Packed-Pixel Mode:** When this bit is 1, the 1-bit-per-pixel packed-pixel mode is enabled.
4	**Enable External XVCLK Input:** When this bit is 1, and when SR22[3] is 0, an external 14.31818 input must be connected to the OSC / XVCLK input pin. (However, MCLK will not use this input. Instead, it will still use the internal MVCO source.) • On VCLK generation, this bit is OR'ed with SR22[3]. • This bit is to be used for NTSC-Out.
3	**Enable 4-bit/pixel Packed-Pixel Mode:** When this bit is 1, 4-bit-per-pixel packed-pixel mode is enabled.

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6.7.23 SR25: Timer-Software Reset and Hardware Configuration #2 *(cont.)*

Bit	Description
2	Reserved
1	**Reset Standby Timer:** This bit is used to reset the internal Standby Mode Timer, when there is an I/O read to the keyboard controller (port 60h).
0	**Reset Backlight Timer:** This bit is used to reset the internal Backlight Timer, when there is an I/O read to the keyboard controller (port 60h).

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6.7.24 SR26: Shader Signature — Least-Significant Byte

I/O Port Address: 3C5

Index:26

Bit	Description	Reset State
7	Shader Signature [7]	0
6	Shader Signature [6]	0
5	Shader Signature [5]	0
4	Shader Signature [4]	0
3	Shader Signature [3]	0
2	Shader Signature [2]	0
1	Shader Signature [1]	0
0	Shader Signature [0]	0

The Shader Signature field is used for factory testing only. Application programs should not use the Shader Signature registers, which are listed here only for completeness.

Bit	Description
7:0	**Shader Signature [7:0]:** This register contains the least-significant byte for the Shader Signature. For the most-significant byte, refer to SR27. The Shader Signature field is used for testing the CL-GD7542 shader logic.

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6.7.25 SR27: Shader Signature — Most-Significant Byte

I/O Port Address: 3C5

Index:27

Bit	Description	Reset State
7	Shader Signature [15]	0
6	Shader Signature [14]	0
5	Shader Signature [13]	0
4	Shader Signature [12]	0
3	Shader Signature [11]	0
2	Shader Signature [10]	0
1	Shader Signature [9]	0
0	Shader Signature [8]	0

The Shader Signature field is used for factory testing only. Application programs should not use the Shader Signature registers, which are listed here only for completeness.

Bit	Description
7:0	**Shader Signature [15:8]:** This register contains the most-significant byte for the Shader Signature. For the most-significant byte, refer to SR26. The Shader Signature field is used for testing the CL-GD7542 shader logic.

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6.7.26 SR2A: Hardware Icon #0 Control Register

I/O Port Address: 3C5

Index:2A

Bit	Description	Reset State
7	Reserved	
6	Icon Horizontal Fine-Position msb[3]	0
5	Memory Map Selection for Hardware Icon #0	0
4	Vertical Scanline Doubling for Hardware Icon #0	0
3	Horizontal Pixel Doubling for Hardware Icon #0	0
2	Blink Enable for Hardware Icon #0	0
1	Display Mode Select for Hardware Icon #0	0
0	Display Enable for Hardware Icon #0	0

Bit	Description
7	Reserved
6	**Icon Horizontal Fine-Position msb[3]:** The least-significant bits[2:0] are in register SRX[7:5]. This 4-bit word is used with 9-dot and 10-dot fonts (character clocks), when in text or horizontally-expanded graphics. The coarse horizontal position is SR10. Note: When horizontal expansion from 640 to 800 is enabled, the hardware cursor must be positioned within 10 dots.
5	**Memory Map Selection for Icon #0:** • A 0 in this bit selects map 0. • A 1 in this bit selects map 1.
4	**Vertical Scanline Doubling for Icon #0:** When this bit is 1: • Icon #0 displays 128 scanlines, but each scanline is replicated vertically. • Icon #0 extends down and forces all other icons down.
3	**Horizontal Pixel Doubling for Icon #0:** When this bit is 1: • Icon #0 displays 128 pixels, but each pixel is replicated horizontally. • Icon #0 expands to the right on the display.
2	**Blink Enable for Icon #0:** • When this bit is 1, icon #0 blinks at one-half the text-cursor blink rate. • When this bit is 0, icon #0 is steady state.
1	**Display Mode Select for Icon #0:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. • A 0 in this bit selects the four-color display mode for icon #0. • A 1 in this bit selects the three-colors-and-transparent display mode.
0	**Display Enable for Icon #0:** When this bit is 1, it enables icon #0 to display.

6.7.27 SR2B: Hardware Icon #1 Control Register

I/O Port Address: 3C5

Index:2B

Bit	Description	Reset State
7	High Drive on FPVDCLK and LLCLK	0
6	Monitor Sense Assist Bit	0
5	Memory Map Selection for Hardware Icon #1	0
4	Vertical Scanline Doubling for Hardware Icon #1	0
3	Horizontal Pixel Doubling for Hardware Icon #1	0
2	Blink Enable for Hardware Icon #1	0
1	Display Mode Select for Hardware Icon #1	0
0	Display Enable for Hardware Icon #1	0

Bit	Description
7	**High Drive on FPVDCLK and LLCLK:** When this bit is 1, FPVDCLK and LLCLK have double the normal output drive to support high-load LCDs.
6	**Monitor Sense Assist Bit:** When this bit is 1: • It disables the internal BLANK# signal to the DAC, thus allowing border color during the entire non-display time. • *and* ARX[5] = 0, this bit can be used to force a monitor display for accurate monitor sense, independent of the following: — CPU speed — CPU interrupts — the video mode
5	**Memory Map Selection for Icon #1:** • A 0 in this bit selects map 0. • A 1 in this bit selects map 1.
4	**Vertical Scanline Doubling for Icon #1:** When this bit is 1: • Icon #1 displays 128 scanlines, but each scanline is replicated vertically. • Icon #1 extends down and forces all other icons down.
3	**Horizontal Pixel Doubling for Icon #1:** When this bit is 1: • Icon #1 displays 128 pixels, but each pixel is replicated horizontally. • Icon #1 expands to the right on the display.

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6.7.27 SR2B: Hardware Icon #1 Control Register *(cont.)*

Bit	Description
2	**Blink Enable for Icon #1:** • When this bit is 1, the icon blinks at one-half the text-cursor blink rate. • When this bit is 0, the icon is steady state.
1	**Display Mode Select for Icon #1:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. • A 0 in this bit selects the four-color display mode for icon #1. • A 1 in this bit selects the three-colors-and-transparent display mode.
0	**Display Enable for Icon #1:** When this bit is 1, it enables icon #1 to display.

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6.7.28 SR2C: Hardware Icon #2 Control and Miscellaneous PCI Register

I/O Port Address: 3C5

Index:2C

Bit	Description	Reset State
7	Enable PCI Base Register 14h [31:24]	0
6	Byte-swap for PCI Base Register 14h [31:24]	0
5	Memory Map Selection for Icon #2	0
4	Vertical Scanline Doubling for Icon #2	0
3	Horizontal Pixel Doubling for Icon #2	0
2	Blink Enable for Icon #2	0
1	Display Mode Select for Icon #2	0
0	Display Enable for Icon #2	0

Bit	Description
7	**Enable PCI Base Register 14h:** • When this bit is 1, and the CL-GD7542 is in PCI bus mode, base register 14h [31:24] is decoded as a valid address range. • When this bit is 0, this address range is ignored.
6	**Byte-swap for PCI Base Register 14h:** When this bit is 1, and the CL-GD7542 is in PCI bus mode: • Byte swapping is enabled for the base register 14h[31:24] address range. • Byte[0] is swapped with byte[1], and byte[2] is swapped with byte[3].
5	**Memory Map Selection for Icon #2:** • A 0 in this bit selects map 0. • A 1 in this bit selects map 1.
4	**Vertical Scanline Doubling for Icon #2:** When this bit is 1: • Icon #2 displays 128 scanlines, but each scanline is replicated vertically. • Icon #2 extends down and forces all other icons down.
3	**Horizontal Pixel Doubling for Icon #2:** When this bit is 1: • Icon #2 displays 128 pixels, but each pixel is replicated horizontally. • Icon #2 expands to the right on the display.
2	**Blink Enable for Icon #2:** • When this bit is 1, icon #2 blinks at one-half the text-cursor blink rate. • When this bit is 0, icon #2 is steady state.
1	**Display Mode Select for Icon #2:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. • A 0 in this bit selects the four-color display mode for icon #2. • A 1 in this bit selects the three-colors-and-transparent display mode.
0	**Display Enable for Icon #2:** When this bit is 1, it enables icon #2 to display.

6.7.29 SR2D: Hardware Icon #3 Control and HIMEM Select Register

I/O Port Address: 3C5

Index:2D

Bit	Description	Reset State
7	HIMEM[1] Reference Bit	0
6	HIMEM[0] Reference Bit	0
5	Memory Map Selection for Icon #3	0
4	Vertical Scanline Doubling for Icon #3	0
3	Horizontal Pixel Doubling for Icon #3	0
2	Blink Enable for Icon #3	0
1	Display Mode Select for Icon #3	0
0	Display Enable for Icon #3	0

Bit	Description
7:6	**HIMEM[1:0] Reference Bits:** These bits are extensions of memory segment select bits in register SR7[7:4]. The CL-GD7542 compares the value in these bits with the levels on the HIMEM[1:0] pins to define the valid upper-address space. • In VESA local bus operations, when HIMEM[1:0] = SR2D[7:6] and A[23:20] = SR7[7:4], the CL-GD7542 identifies the upper address as its CPU address-mapped area. • In PCI bus operations, when these two bits are non-zero, the chip is in linear memory mode. When SR2D[7:6] or SR7[7:4] are not zero, the PCI memory map is defined by base registers 10 or 14 (upper bytes). • For segmented addressing mode, these bits must be 0.
5	**Memory Map Selection for Icon #3:** • A 0 in this bit selects map 0. • A 1 in this bit selects map 1.
4	**Vertical Scanline Doubling for Icon #3:** When this bit is 1: • Icon #3 displays 128 scanlines, but each scanline is replicated vertically. • Icon #3 extends down and forces all other icons down.
3	**Horizontal Pixel Doubling for Icon #3:** When this bit is 1: • Icon #3 displays 128 pixels, but each pixel is replicated horizontally. • Icon #3 expands to the right on the display.
2	**Blink Enable for Icon #3:** • When this bit is 1, icon #3 blinks at one-half the text-cursor blink rate. • When this bit is 0, icon #3 is steady state.

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6.7.29 SR2D: Hardware Icon #3 Control and HIMEM Select Register *(cont.)*

Bit	Description
1	**Display Mode Select for Icon #3:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. • A 0 in this bit selects the four-color display mode for icon #3. • A 1 in this bit selects the three-colors-and-transparent display mode.
0	**Display Enable for Icon #3:** When this bit is 1, it enables icon #3 to display.

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6.7.30 SR2E: Graphics-Cursor Horizontal-Position Extension Register

I/O Port Address: 3C5

Index:2E

Bit	Description	Reset State
7	Early OVRW# Signal Delay [2]	0
6	Early OVRW# Signal Delay [1]	0
5	Early OVRW# Signal Delay [0]	0
4	Memory-Write Cycle Delay [1]	0
3	Memory-Write Cycle Delay [0]	0
2	Hardware Icon #0 Address Map Select [1]	0
1	Hardware Icon #0 Address Map Select [0]	0
0	Hardware Cursor Horizontal Fine-Position msb[3]	0

Bit **Description**

7:5 **Early OVRW# Signal Delay [2:0]:**
These three bits are used to define the time interval between the Overlay Window output from the CL-GD7542 and the data input from the external TV decoder.

- This time interval is used for a time differential adjustment that is intended to compensate for the Feature Connector system delay:
  - — *from* the time the OVRW# output is generated
  - — *to* the time the Feature Connector data is presented to the CL-GD7542
- The FCEVIDEO input must be externally synchronized to the data input from the OVRW# output.
- The table that follows shows early clock cycles for either 1x or 2x DCLKs.
  - — The programmed number of early clock cycles defines the delay between the assertion and de-assertion of OVRW# and the corresponding start and end of the overlay window.
  - — The 1x DCLKs are typically 25-MHz clocks that are used for 8-bit pixels.
  - — The 2x DCLKs are typically 50-MHz clocks that are used for 16-bit pixels.

SR2E			Total Early Clock Cycles	
[7]	[6]	[5]	1x DCLK	2x DCLKs
0	0	0	0	3
0	0	1	don't use	4
0	1	0	don't use	5
0	1	1	0	6
1	0	0	1	7
1	0	1	2	8
1	1	0	3	9
1	1	1	11	25

Continued on next page

6.7.30 SR2E: Graphics-Cursor Horizontal-Position Extension Register *(Cont.)*

Bit **Description**

4:3 **Memory-Write Cycle Delay [1:0]:**
These two bits are used to delay the start of a memory-write cycle in units of MCLKs, as explained in the table below:

SR2E [4]	SR2E [3]	Delay Start of Memory-Write Cycle By:	Conditions Under Which to Use:
0	0	3 MCLKs	Use for worst-case timing conditions.
0	1	2 MCLKs	Optimized for 33-MHz PCI bus. Optimized for 50-MHz VESA VL bus.
1	0	1 MCLKs	Optimized for 33-MHz VL bus.
1	1	0 MCLKs	Optimized for 20-MHz VL bus.

2:1 **Hardware Icon #0 Address Map Select [1:0]:**
- When this field is zero, each icon has two memory maps assigned to it.
- When this field is non-zero, only icon #0 can be used.
  - — Hardware icon #0 can have up to eight memory maps.
  - — The other hardware icons #1:#3 should be disabled.
  - — The number in SR2E[2:1] points to the pair of two icon maps selected by SR2A[5], but in this case, all maps will go to icon #0 for display.
  - — In this order of significance, SR2E[2:1] and SR2A[5] select the eight memory maps for icon #0.

0 **Hardware Cursor Horizontal Fine Position msb[3]:**
- When SR12[3] = 0, the CPU can modify the hardware cursor position.
- The hardware cursor horizontal fine position is a 4-bit word consisting of this bit and three least-significant bits [2:0], in SRX[7:5].
- The hardware cursor horizontal fine position is used with 10-dot character clocks, when in horizontally expanded graphics modes.
- The hardware cursor horizontal coarse position is in register SR10.
- In non-expanded graphics modes, this bit is always 0.

Note: The hardware cursor must be positioned within 10 dots when horizontal expansion from 640 to 800 is enabled.

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6.7.31 SR2F: Half-Frame-Accelerator FIFO Threshold

I/O Port Address: 3C5

Index:2F

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Half-Frame Accelerator FIFO Threshold [3]	0
2	Half-Frame Accelerator FIFO Threshold [2]	0
1	Half-Frame Accelerator FIFO Threshold [1]	0
0	Half-Frame Accelerator FIFO Threshold [0]	0

Note: These register bits affect only dual-scan panels.

Bit	Description
7:4	Reserved
3:0	**Half-Frame Accelerator FIFO Threshold [3:0]:** The half-frame accelerator FIFO is 16 data stages deep and 32 bits wide. Before a new request can be made for a refill of the half-frame-accelerator read FIFO, SRF[3:0] controls how many 32-bit data stages are empty in the half-frame-accelerator read FIFO. (At the same time that the half-frame-accelerator read FIFO is emptied, it is refilled.) Note: A color LCD has a higher FIFO threshold than a monochrome LCD. (To minimize CRT-FIFO latency, in 16-bit and 24-bit per pixel modes, program a low threshold of 3h for a monochrome LCD. Program 6h for a dual-scan color STN LCD.) Example: If SR2F[3:0] = 4, after only four half-frame-accelerator FIFO stages are empty, a new request, programmed in hex, will be made for new half-frame-accelerator cycles. For this example, program a FIFO threshold that is: • low (2h to 4h) for 2 to 4 data stages for dual-scan monochrome STN panels. • higher (4h to 7h) for 4 to 7 data stages for dual-scan color STN panels. • less than Ah for all other cases.

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CL 28671

6.7.32 GR9: Offset Register 0

I/O Port Address: 3CF

Index:9

Bit	Description	Reset State
7	Offset 0 [7]	0
6	Offset 0 [6]	0
5	Offset 0 [5]	0
4	Offset 0 [4]	0
3	Offset 0 [3]	0
2	Offset 0 [2]	0
1	Offset 0 [1]	0
0	Offset 0 [0]	0

This register is used to access up to 2 Mbytes of display memory with up to 16-Kbyte granularity.

Bit	Description
7:0	**Offset Register 0 [7:0]:** • This offset register is used when one of the following conditions is true: — GRB[0] = 0 — GRB[0] = 1 *and* address bit A[15] = 0 • When one of the above conditions is true *and* GRB[5] = 0: — The register's offset value is added to the contents of XA (bus addresses A[19:12]) to provide XMA, an address into display memory. — Access is for 1 Mbyte of display memory with 4-Kbyte granularity. • When one of the above conditions is true *and* GRB[5] = 1: — The register's offset value is added to the contents of XA (bus addresses A[20:14]) to provide XMA, an address into display memory. — Access is for up to 2 Mbytes of display memory with 16-Kbyte granularity. **XMA.** XMA is the display memory address, prior to modification by address wrap controls. XMA = (Bus Address XA) + (value from Offset Register GR9 or GRA). **XA.** XA is the address on the bus, with bits [16] and [15] possibly forced to a 0 as indicated in the following table.

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6.7.32 GR9: Offset Register 0 *(cont.)*

Configuration		Bus Address XA		
If Display Memory is:	And Register Setting:	[16]	[15]	[14:0]
128 Kbytes	GR6[3:2] = 00	A[16]	A[15]	A[14:0]
64 Kbytes	GR6[3:2] = 01 *AND* GRB[0] = 0 (Offset 1 Disabled)	0	A[15]	A[14:0]
64 Kbytes	GR6[3:2] = 01 *OR* GRB[0] = 1 (Offset 1 Enabled)	0	0	A[14:0]

The XA bus address is summed with the contents of an Offset Register with one of three relative alignments, according to the configuration indicated in the three tables that follow:

Table 6–3. One MByte of Memory, 4 KBytes of Granularity, VGA Mapping

Bus Address (XA)	0	0	0	XA[16]	XA[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[7]	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]
= Display Memory Address (XMA)	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

Table 6–4. Two MBytes of Memory, 16 KBytes of Granularity, VGA Mapping

Bus Address	0	0	0	0	XA[16]	XA[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]	0	0
= Display Memory Address	XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

Table 6–5. One MByte or Two MBytes of Memory, 16 KBytes of Granularity, Linear Addressing

Bus Address	LA[20]	LA[19]	LA[18]	LA[17]	A[16]	A[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]	0	0
= Display Memory Address	XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

6.7.33 GRA: Offset Register 1

I/O Port Address: 3CF

Index: A

Bit	Description	Reset State
7	Offset 1 [7]	0
6	Offset 1 [6]	0
5	Offset 1 [5]	0
4	Offset 1 [4]	0
3	Offset 1 [3]	0
2	Offset 1 [2]	0
1	Offset 1 [1]	0
0	Offset 1 [0]	0

This register is used to provide access for up to 2 Mbytes of display memory with 16-Kbyte granularity.

Bit	Description
7:0	**Offset 1 [7:0]:** • When GRB[0] = 0, this register is disabled. • When GRB[0] = 1: — *and* A[15] = 1, the contents of GRA[7:0] are added to the contents of A[19:12] to provide access to up to 1 Mbyte of address into display memory, with 4-Kbyte granularity. — *and* GRB[5] = 1, the contents of GRA[6:0] are added to the contents of A[20:14] to provide access to up to 2 Mbytes of address into display memory, with 16-Kbyte granularity.

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CL 28674

6.7.34 GRB: Graphics Controller Mode Extensions Register

I/O Port Address: 3CF

Index: B

Bit	Description	Reset State
7	Reserved	0
6	Reserved	0
5	Offset Granularity	0
4	Enhanced Writes for 16-bit Pixels Enable	0
3	8-Byte-Wide Display Memory Data Latches Enable	0
2	Extended Write Modes Enable	0
1	By-8 Addressing Enable	0
0	Offset Register 1 Enable	0

This register is used to enable or disable extended write modes which provide enhanced performance.

Bit	Description
7:6	Reserved
5	**Offset Granularity:** When this bit is programmed to 1, Offset Registers GR9 and GRA are redefined as containing bits [6:0]. In this case: • These bits are added to address bits [20:14] to provide access to 2 Mbytes of display memory with 16-Kbyte granularity. • SR7[4] (the low-order bit of a 1-Mbyte address page) becomes a don't care. • Linear address memory mapping becomes 2 Mbytes on any 2-Mbyte boundary.
4	**Enhanced Writes for 16-bit Pixels Enable:** GRB[2] must be 1 in order to enable this bit. When both GRB[2] and GRB[4] are programmed to 1, the CL-GD7542 will execute the following enhanced write modes when Extended Write Modes 4 and 5 are enabled and executed: • **By-16 Addressing Enabled:** The system address is shifted by 4, relative to true packed-pixel addressing, so that each system byte address points to a different 8-pixel (16-byte) block in display memory. • **16-Byte Transfer Enabled:** Up to 16 bytes (8 pixels) can be written into display memory for each CPU byte transfer. • **GR10 and GR11 Enabled:** GR10 and GR11 are enabled as foreground and background color extensions. • **SR2 Doubling Enabled:** Each bit of SR2 is used as a pixel write mask for two bytes (one pixel).

Continued on next page

6.7.34 GRB: Graphics Controller Mode Extensions Register *(cont.)*

Bit	Description
3	**8-Byte-Wide Display Memory Data Latches Enable:** When this bit is 1, display memory data latches are 8 bytes wide rather than the normal 4 bytes.
2	**Extended Write Modes Enable:** When this bit is 1, the CL-GD7542 will enable and execute the following extended write modes: • **8-Byte Transfer Enabled:** — When GRB[2] = 1, up to 8 bytes (8 pixels) can be written into display memory for each CPU byte transferred. — When GRB[2] = 1 *and* GRB[4] = 1, up to 16 bytes can be written into display memory for color expansion. • **GR5[2] Enabled:** When GRB[2] = 1, Extended Write Modes 4 and 5 can be enabled. • **GR0 Extended:** When GRB[2] = 1, Register GR0 is extended from 4 bits to 8 bits. • **GR1 Extended:** When GRB[2] = 1, Register GR1 is extended from 4 bits to 8 bits. • **SR2 Extended:** When GRB[2] = 1, Register SR2 is extended from 4 bits to 8 bits. • **GRB[4] Enabled:** When GRB[2] = 1, GRB[4] is enabled.
1	**By-8 Addressing Enable:** • When this bit is 1, the system address is shifted by 3, relative to true packed-pixel addressing, so that each system byte address points to a different 8-pixel (8-byte) block in display memory. • When GRB[4] = 1, this bit is a don't care.
0	**Offset Register 1 Enable:** • When this bit is programmed to 1, the value in system address [15] will be used to choose between Offset Register 0 and Offset Register 1. • When this bit is programmed to 0, the value in system address [15] will be ignored, and Offset Register 0 will always be chosen. • This bit must always be programmed to a 0 for 1 Mbyte of linear addressing.

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CL 28676

6.7.35 GRC: Color Key Compare Register

I/O Port Address: 3CF

Index: C

Bit	Description	Reset State
7	Color Key Compare [7]	1
6	Color Key Compare [6]	1
5	Color Key Compare [5]	1
4	Color Key Compare [4]	1
3	Color Key Compare [3]	1
2	Color Key Compare [2]	1
1	Color Key Compare [1]	1
0	Color Key Compare [0]	1

This register contains an 8-bit value that is compared to video data. For more information, refer to Appendix A8.

Bit	Description
7:0	**Color Key Compare [7:0]:** This register contains an 8-bit value that is compared to the video data. When Mode Switching 10 or 11 is chosen, a match between this value in GRC[7:0] and the video data value will cause the video data pixel to be replaced with data from the feature connector.

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6.7.36 GRD: Color Key Compare Mask Register

I/O Port Address: 3CF

Index: D

Bit	Description	Reset State
7	Color Key Compare Mask [7]	0
6	Color Key Compare Mask [6]	0
5	Color Key Compare Mask [5]	0
4	Color Key Compare Mask [4]	0
3	Color Key Compare Mask [3]	0
2	Color Key Compare Mask [2]	0
1	Color Key Compare Mask [1]	0
0	Color Key Compare Mask [0]	0

This register contains an 8-bit mask under which the color key comparison of GRC is made. For more information, refer to Appendix A8.

Bit	Description
7:0	**Color Key Compare Mask [7:0]:** A bit value of 1 for a GRD bit will cause the corresponding video data bit to be masked out and not participate in the color comparison.

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CL 28678

6.7.37 GRE: PCI-Burst and Green-PC Control Register

I/O Port Address: 3CF

Index: E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Enable PCI-Bus Burst-Write Mode	0
3	Enable Extensive PCI-Bus Burst-Write Mode	0
2	DPMS (Green PC) Control [1]	0
1	DPMS (Green PC) Control [0]	0
0	DCLK Output Divided By Two	0

This register contains miscellaneous control bits.

Bit 7:5 — Reserved

Bit 4 — Enable PCI-Bus Burst-Write Mode:

- When the PCI bus is selected (SR22[7] = 1 or SR22[0] = 1), and this bit is 1, the CPU may execute burst writes during vertical non-display time.
- When the system BitBLT (bit block transfer) is enabled, the CL-GD7542 automatically disables this burst-write function.
- The CL-GD7542 does not support PCI-burst-read cycles.

Bit 3 — Enable Extensive PCI-Bus Burst-Write Mode:

When the PCI bus is selected (SR22[7] = 1 or SR22[0] = 1), and this bit is 1, the CPU may execute burst writes anytime during a frame.

Bit 2:1 — DPMS (Green PC) Control [1:0]:

These two bits control the CRT monitor power as specified in the Display Power Management Signalling (DPMS) specification, as shown in the following table:

GRE [2]	GRE [1]	CRT Monitor Power Mode	VSYNC Activity	HSYNC Activity	DAC Power	CL-GD7542 Power Management Mode
0	0	On	Pulsing	Pulsing	On	Active
0	1	Standby	Pulsing	Static at MISC[6] inactive level	Off	Active, Standby, or Suspend
1	0	Suspend	Static at MISC[7] inactive level	Pulsing	Off	Active, Standby, or Suspend
1	1	Off	Static at MISC[7] inactive level	Static at MISC[6] inactive level	Off	Active, Standby, or Suspend

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6.7.37 GRE: PCI-Burst and Green-PC Control Register *(Cont.)*

Bit	Description
2:1(*cont.*)	Because the DPMS CRT power-management modes are not related to the CL-GD7542 controller power-management modes, they can be independently programmed, except for the following restrictions: • Prior to placing the CL-GD7542 in Suspend mode, the BIOS may program any DPMS power-saving mode for the CRT. — The 32-kHz input to the CL-GD7542 is used to provide any sync pulse required by the DPMS. • When the CL-GD7542 timer-driven (that is, hardware-controlled) Standby mode is used, the DPMS STANDBY signal is forced by the hardware. — Because the CL-GD7542 Standby mode is timer-driven, software control is not allowed. • When the CL-GD7542 is in LCD-only mode, the BIOS must set GRE[2:1] = 11 to power off any CRT that may be connected to the notebook computer. • The inactive static VSYNC and HSYNC signal levels are determined by the polarity selection in External/General Register MISC[7:6]. — When MISC[7] = 1, the inactive level is low for the VSYNC signal. — When MISC[6] = 1, the inactive level is low for the HSYNC signal.
0	**DCLK Output, Divided By Two:** • When this bit is 0, the CL-GD7542 operates normally. • When this bit is 1, the CL-GD7542 emulates external DAC clocking mode 1. — The DCLK rising edge can be used to clock a 16-bit data pixel low byte. — The DCLK falling edge can be used to clock a 16-bit data pixel high byte. • In the CL-GD7542, the option of setting this bit to 1: — works only for the CRT-only mode. — does not work for the LCD or SimulSCAN mode. When this bit is 1, the clock to the LCD section is also divided by two, which prevents the LCD from working properly.

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CL 28680

6.7.38 GR10: 16-bit Pixel Background Color High Byte Register

I/O Port Address: 3CF

Index: 10

Bit	Description	Reset State
7	Background Color [15]	0
6	Background Color [14]	0
5	Background Color [13]	0
4	Background Color [12]	0
3	Background Color [11]	0
2	Background Color [10]	0
1	Background Color [9]	0
0	Background Color [8]	0

This register contains the high-order eight bits of the background color for Extended Write Mode 5.

Bit	Description
7:0	**Background Color [15:8]:** • The contents of this register: — are the high-order eight bits of the background color for Extended Write Mode 5. — are sent to display memory map planes 1 and 3. • The contents of Graphics Controller Register GR0: — are the low-order eight bits of the background color for Extended Write Mode 5. — are sent to display memory map planes 0 and 2.

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6.7.39 GR11: 16-bit Pixel Foreground Color High Byte Register

I/O Port Address: 3CF

Index: 11

Bit	Description	Reset State
7	Foreground Color [15]	0
6	Foreground Color [14]	0
5	Foreground Color [13]	0
4	Foreground Color [12]	0
3	Foreground Color [11]	0
2	Foreground Color [10]	0
1	Foreground Color [9]	0
0	Foreground Color [8]	0

This register contains the high-order eight bits of the foreground color for Extended Write Modes 5 and 4.

Bit	Description
7:0	**Foreground Color [15:8]:** • The contents of this register: — are the high-order eight bits of the foreground color for Extended Write Modes 5 and 4. — are sent to display memory map planes 1 and 3. • The contents of Graphics Controller Register GR1: — are the low-order eight bits of the foreground color for Extended Write Modes 5 and 4. — are sent to display memory map planes 0 and 2.

6.7.40 GR20: BLT Width Low Register

I/O Port Address: 3CF

Index: 20

Bit	Description	Reset State
7	BLT Width [7]	0
6	BLT Width [6]	0
5	BLT Width [5]	0
4	BLT Width [4]	0
3	BLT Width [3]	0
2	BLT Width [2]	0
1	BLT Width [1]	0
0	BLT Width [0]	0

This register contains the low-order eight bits of the BitBLT (bit block transfer) width. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Width [7:0]:** This field is the low-order eight bits of the 11-bit value specifying the width-1, in bytes, of the areas involved in a BitBLT.

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6.7.41 GR21: BLT Width High Register

I/O Port Address: 3CF

Index: 21

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	BLT Width [10]	0
1	BLT Width [9]	0
0	BLT Width [8]	0

This register contains the high-order three bits of the BLT width.

Bit	Description
7:3	Reserved
2:0	**BLT Width [10:8]:** This field is the high-order three bits of the 11-bit value specifying the width-1, in bytes, of the areas involved in a BitBLT.

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6.7.42 GR22: BLT Height Low Register

I/O Port Address: 3CF

Index: 22

Bit	Description	Reset State
7	BLT Height [7]	0
6	BLT Height [6]	0
5	BLT Height [5]	0
4	BLT Height [4]	0
3	BLT Height [3]	0
2	BLT Height [2]	0
1	BLT Height [1]	0
0	BLT Height [0]	0

This register contains the low-order eight bits of the BLT height. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Height [7:0]:** This field is the low-order eight bits of the 10-bit value specifying the height-1, in scanlines, of the areas involved in a BitBLT.

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6.7.43 GR23: BLT Height High Register

I/O Port Address: 3CF

Index: 23

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	BLT Height [9]	0
0	BLT Height [8]	0

This register contains the high-order two bits of the BLT height.

Bit	Description
7:2	Reserved
1:0	**BLT Height [9:8]:** This field is the high-order two bits of the 10-bit value specifying the height-1, in scanlines, of the areas involved in a BitBLT.

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6.7.44 GR24: BLT Destination Pitch Low Register

I/O Port Address: 3CF

Index: 24

Bit	Description	Reset State
7	BLT Destination Pitch [7]	0
6	BLT Destination Pitch [6]	0
5	BLT Destination Pitch [5]	0
4	BLT Destination Pitch [4]	0
3	BLT Destination Pitch [3]	0
2	BLT Destination Pitch [2]	0
1	BLT Destination Pitch [1]	0
0	BLT Destination Pitch [0]	0

This register contains the low-order eight bits of the BLT destination pitch. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Destination Pitch [7:0]:** This field is the low-order eight bits of the 12-bit value specifying the destination pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT.

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6.7.45 GR25: BLT Destination Pitch High Register

I/O Port Address: 3CF

Index: 25

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	BLT Destination Pitch [11]	0
2	BLT Destination Pitch [10]	0
1	BLT Destination Pitch [9]	0
0	BLT Destination Pitch [8]	0

This register contains the high-order four bits of the BLT destination pitch. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:4	Reserved
3:0	**BLT Destination Pitch [11:8]:** This field is the high-order four bits of the 12-bit value specifying the destination pitch of the areas involved in a BitBLT.

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6.7.46 GR26: BLT Source Pitch Low Register

I/O Port Address: 3CF

Index: 26

Bit	Description	Reset State
7	BLT Source Pitch [7]	0
6	BLT Source Pitch [6]	0
5	BLT Source Pitch [5]	0
4	BLT Source Pitch [4]	0
3	BLT Source Pitch [3]	0
2	BLT Source Pitch [2]	0
1	BLT Source Pitch [1]	0
0	BLT Source Pitch [0]	0

This register contains the low-order eight bits of the BLT source pitch. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Source Pitch [7:0]:** This field is the low-order eight bits of the 12-bit value specifying the source pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT.

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6.7.47 GR27: BLT Source Pitch High Register

I/O Port Address: 3CF

Index: 27

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	BLT Source Pitch [11]	0
2	BLT Source Pitch [10]	0
1	BLT Source Pitch [9]	0
0	BLT Source Pitch [8]	0

This register contains the high-order four bits of the BLT source pitch.

Bit	Description
7:4	Reserved
3:0	**BLT Source Pitch [11:8]:** This field is the high-order four bits of the 12-bit value specifying the source pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT.

6.7.48 GR28: BLT Destination Start Low Register

I/O Port Address: 3CF

Index: 28

Bit	Description	Reset State
7	BLT Destination Start [7]	0
6	BLT Destination Start [6]	0
5	BLT Destination Start [5]	0
4	BLT Destination Start [4]	0
3	BLT Destination Start [3]	0
2	BLT Destination Start [2]	0
1	BLT Destination Start [1]	0
0	BLT Destination Start [0]	0

This register contains the low-order eight bits of the BLT destination start. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Destination Start [7:0]:** This field is the low-order eight bits of the 21-bit BLT destination start value that specifies the byte address of the beginning destination pixel for a BitBLT.

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CL 28691

6.7.49 GR29: BLT Destination Start Mid Register

I/O Port Address: 3CF

Index: 29

Bit	Description	Reset State
7	BLT Destination Start [15]	0
6	BLT Destination Start [14]	0
5	BLT Destination Start [13]	0
4	BLT Destination Start [12]	0
3	BLT Destination Start [11]	0
2	BLT Destination Start [10]	0
1	BLT Destination Start [9]	0
0	BLT Destination Start [8]	0

This register contains the middle eight bits of the BLT destination start.

Bit	Description
7:0	**BLT Destination Start [15:8]:** This field is the middle eight bits of the 21-bit BLT destination start value that specifies the byte address of the beginning destination pixel for a BitBLT.

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CL 28692

6.7.50 GR2A: BLT Destination Start High Register

I/O Port Address: 3CF

Index: 2A

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	BLT Destination Start [20]	0
3	BLT Destination Start [19]	0
2	BLT Destination Start [18]	0
1	BLT Destination Start [17]	0
0	BLT Destination Start [16]	0

This register contains the high-order five bits of the BLT destination start.

Bit	Description
7:0	**BLT Destination Start [20:16]:** This field is the high-order five bits of the 21-bit BLT destination start value that specifies the byte address of the beginning destination pixel for a BitBLT.

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6.7.51 GR2C: BLT Source Start Low Register

I/O Port Address: 3CF

Index: 2C

Bit	Description	Reset State
7	BLT Source Start [7]	0
6	BLT Source Start [6]	0
5	BLT Source Start [5]	0
4	BLT Source Start [4]	0
3	BLT Source Start [3]	0
2	BLT Source Start [2]	0
1	BLT Source Start [1]	0
0	BLT Source Start [0]	0

This register contains the low-order eight bits of the BLT source start. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Source Start [7:0]:** This field is the low-order eight bits of the 21-bit BLT source start value that specifies the byte address of the beginning source pixel for a BitBLT.

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CL 28694

6.7.52 GR2D: BLT Source Start Mid Register

I/O Port Address: 3CF

Index: 2D

Bit	Description	Reset State
7	BLT Source Start [15]	0
6	BLT Source Start [14]	0
5	BLT Source Start [13]	0
4	BLT Source Start [12]	0
3	BLT Source Start [11]	0
2	BLT Source Start [10]	0
1	BLT Source Start [9]	0
0	BLT Source Start [8]	0

This register contains the middle eight bits of the BLT source start.

Bit	Description
7:0	**BLT Source Start [15:8]:** This field is the middle eight bits of the 21-bit BLT source start value that specifies the byte address of the beginning source pixel for a BitBLT.

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6.7.53 GR2E: BLT Source Start High Register

I/O Port Address: 3CF

Index: 2E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	BLT Source Start [20]	0
3	BLT Source Start [19]	0
2	BLT Source Start [18]	0
1	BLT Source Start [17]	0
0	BLT Source Start [16]	0

This register contains the high-order five bits of the BLT source start.

Bit	Description
7:5	Reserved
4:0	**BLT Source Start [20:16]:** This field is the high-order five bits of the 21-bit BLT source start value that specifies the byte address of the beginning source pixel for a BitBLT.

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6.7.54 GR30: BLT Mode Register

I/O Port Address: 3CF

Index: 30

Bit	Description	Reset State
7	Enable Color Expand	0
6	Enable 8 x 8 Pattern Copy	0
5	Reserved	
4	Color Expand / Transparency Width	0
3	Enable Transparency Compare	0
2	BLT Source Display Memory / System Memory	0
1	BLT Destination Display Memory / System Memory	0
0	BLT Direction	0

This register contains the bits that specify the BitBLT (bit block transfer) details, but not the BLT raster operation. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7	**Enable Color Expand:** • When this bit is programmed to 1, the raster operation source will be the expanded result from the bit-mapped source. — The destination must be screen memory. — The direction must be incremental. — Raster operations are available for all block moves. — Graphics Controller Registers GR0 and GR1 and Extension Registers GR10 and GR11 are used for bit-map color-expanded BLT operations. — When the source data is expanded, the most-significant bit of the first source byte will become the first pixel in the screen memory destination. — For color-expanded BLTs (the source is system memory or display memory), each logical line must be an even byte. — Source bytes must be completely used. As a result, when a logical line is not an even multiple of eight pixels, 'dummy' bits are used to fill it out to an even byte. — 'Dummy' bits will be ignored under control of the BLT width setting. — When the source of color-expanded data is display memory, the source starting address must be on a 4-byte boundary, and the addressing will always be linear. (The source pitch will be ignored.) — Fo. information regarding color expansion, refer to Appendix A4. • When this bit is programmed to 0, the raster operation source will be the pixel data read from the source.

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6.7.54 GR30: BLT Mode Register *(cont.)*

Bit — **Description**

6 — **Enable 8 x 8 Pattern Copy:**
When this bit is 1, the source pattern will be copied repeatedly to the destination rectangular area.
- The pattern source must be aligned on a four-byte boundary.
- The pattern source will be linear-addressed data in one of three arrangements as shown in the following table:

Operating Mode	Pattern Source Arrangement
Color Expansion Enabled	8 bytes of monochrome bitmap for the 8 x 8 pattern
8-bit Pixels	64 bytes of color data for 64 pixels
16-bit Pixels	128 bytes of color data for 64 pixels

5 — Reserved

4 — **Color Expand / Transparency Width:**
- When GR30[7] is 1:
  - — *and* this bit is 1, the bit-mapped source will be expanded to 16 bits/pixel.
  - — *and* this bit is 0, the bit-mapped source will be expanded to 8 bits/pixel.
- When GR30[3] is 1:
  - — *and* this bit is 1, the transparency compare will be on 16-bit pixels.
  - — *and* this bit is 0, the transparency compare will be on 8-bit pixels.

3 — **Enable Transparency Compare:**
- When this bit is 1, then for each pixel, the result of the raster operation is compared to the Transparent Color Registers (Extension Registers GR34 and GR35).
  - — When the compare is a match, data are not written to the destination.
  - — When the color-expand BLT is to be used with an opaque foreground and a transparent background (similar to Extended Write Mode 4), the transparency feature must be used, and the transparent color must be set to the background color.
- When this bit is 0, the data are written to the destination without regard to Transparent Color Registers GR34 and GR35.

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6.7.54 GR30: BLT Mode Register *(cont.)*

Bit	Description
2	**BLT Source Display Memory / System Memory:** • When this bit is 1, the BLT source will be system memory. — The CPU will perform the system bus transfers, but the CL-GD7542 will ignore the address provided with such transfers. — The CPU is required to transfer data in increments of four bytes. When the total number of bytes moved for a BLT is not a multiple of four, the CPU must write 'extra' bytes. — System-memory-to-system-memory BLTs are not allowed. • When this bit is 0, the BLT source will be display memory. • When system-to-screen BitBLTs are being executed: — that involve color expansion, the BLT Source Start Registers GR2C, GR2D, and GR2E must be cleared to 0. — that do not involve color expansion, 16-bit host transfers must be used, or the system will become non-operative.
1	**BLT Destination Display Memory / System Memory:** • When this bit is 1, the BLT destination will be system memory. — The CPU will perform the system bus transfers, but the CL-GD7542 will ignore the address provided with such transfers. — The CPU is required to transfer data in increments of four bytes. When the total number of bytes moved for a BLT is not a multiple of four, the CPU must read 'extra' bytes. — System-memory-to-system-memory BLTs are not allowed. • When this bit is 0, the BLT destination will be display memory. • When system-to-screen BitBLTs are being executed, 16-bit host transfers must be used, or the system will become non-operative.
0	**BLT Direction:** When this bit: • is 1: — the source and destination addresses will be decremented. — The BLT will proceed from higher addresses to lower addresses. — The starting address will be the highest addressed byte in each area. • is 0: — the source and destination addresses will be incremented. — The BLT will proceed from lower addresses to higher addresses.

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6.7.55 GR31: BLT Start / Status Register

I/O Port Address: 3CF

Index: 31

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	BLT Progress Status (Read Only)	0
2	BLT Reset	0
1	BLT Start / Suspend	0
0	BLT Status (Read Only)	0

This register contains the bit that begins a BLT and a bit that indicates whether the BLT has completed. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:4	Reserved
3	**BLT Progress Status (Read Only):** This bit will be set to 1 at the start of a BLT. • When the BLT operation resets (refer to GR32[2]), this bit clears to 0. • When the BLT operation suspends (refer to GR31[1]), this bit remains a 1.
2	**BLT Reset:** • When this bit is set to 1: — The entire BLT engine is immediately reset and any operation in progress will be terminated. The operation cannot be restarted. — GR31[3] clears to 0. • This bit must be cleared to 0 before any BitBLT operations are attempted.
1	**BLT Start / Suspend:** • When this bit is set to 1, the BLT starts with the next available display memory cycle. • GR31[0] must be monitored to determine when the BLT is complete. • This bit will clear to 0 when the BLT completes. • When this bit is cleared to 0, the BLT suspends at the current scanline end. — When the BLT is suspended, the BLT Height Registers reflect the line count for the last completed transfer. — When the BLT is suspended, GR31[3] remains a 1. — A suspended BLT may resume by setting this bit to 1.
0	**BLT Status (Read Only):** • When this bit is a 1, the BLT is in progress. • When this bit is a 0, the BLT is complete.

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6.7.56 GR32: BLT Raster Operation Register (ROP)

I/O Port Address: 3CF

Index: 32

Bit	Description	Reset State
7	f [7]	0
6	f [6]	0
5	f [5]	0
4	f [4]	0
3	f [3]	0
2	f [2]	0
1	f [1]	0
0	f [0]	0

This register selects a raster operation function. For more information, refer to Appendix A1.

Bit	Description
7:0	**f [7:0]:** This eight-bit value selects 1 of 16 possible two-operand raster operation (ROP) functions, as indicated in the table below:

Z (Logical Function: Algebraic Notation)	ROP No. (Hex)	Comparable Microsoft Name	Value Microsoft Uses to Get ROP
0	00	BLACKNESS	00000042
1	0E	WHITENESS	00FF0062
S	0D	SRCCOPY	00CC0020
D	06	-	00AA0029
-S	D0	NOTSRCCOPY	00330008
-D	0B	DSTINVERT	00550009
S.D	05	SRCAND	008800C6
S.-D	09	SRCERASE	00440328
-S.D	50	-	00220326
-S.-D	90	NOTSRCERASE	001100A6
S+D	6D	SRCPAINT	00EE0086
S+-D	AD	-	00DD0228
-S+D	D6	MERGEPAINT	00BB0226
-S+-D	DA	-	007700E6
S- = D	59	SRCINVERT (xor)	00660046
S = D	95	- (xnor)	00990066

6.7.57 GR34: BLT Transparent Color Low Register

I/O Port Address: 3CF

Index: 34

Bit	Description	Reset State
7	BLT Transparent Color [7]	0
6	BLT Transparent Color [6]	0
5	BLT Transparent Color [5]	0
4	BLT Transparent Color [4]	0
3	BLT Transparent Color [3]	0
2	BLT Transparent Color [2]	0
1	BLT Transparent Color [1]	0
0	BLT Transparent Color [0]	0

This register contains the low-order eight bits of the 16-bit Transparent Color. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Transparent Color [7:0]:** • This field is the low-order eight bits of the BLT Transparent Color. • When GR30[3] = 1, this value will be compared with the raster operation result. If it is equal, the raster operation result is not written to the destination.

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6.7.58 GR35: BLT Transparent Color High Register

I/O Port Address: 3CF

Index: 35

Bit	Description	Reset State
7	BLT Transparent Color [15]	0
6	BLT Transparent Color [14]	0
5	BLT Transparent Color [13]	0
4	BLT Transparent Color [12]	0
3	BLT Transparent Color [11]	0
2	BLT Transparent Color [10]	0
1	BLT Transparent Color [9]	0
0	BLT Transparent Color [8]	0

This register contains the high-order eight bits of the 16-bit Transparent Color. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Transparent Color [15:8]:** • This field is the high-order eight bits of the BLT Transparent Color. • When Graphics Controller Register GR30[3] = 1, this value will be compared with the raster operation result. If it is equal, the result is not written to the destination. • For 8-bit color modes, Graphics Controller Register GR35 must be set equal to GR34.

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6.7.59 GR38: BLT Transparent Color Mask Low Register

I/O Port Address: 3CF

Index: 38

Bit	Description	Reset State
7	BLT Transparent Color Mask [7]	0
6	BLT Transparent Color Mask [6]	0
5	BLT Transparent Color Mask [5]	0
4	BLT Transparent Color Mask [4]	0
3	BLT Transparent Color Mask [3]	0
2	BLT Transparent Color Mask [2]	0
1	BLT Transparent Color Mask [1]	0
0	BLT Transparent Color Mask [0]	0

This register contains the low-order eight bits of the 16-bit Transparent Color Mask. For more information on the BitBLT, refer to Appendix A1.

Bit	Description
7:0	**BLT Transparent Color Mask [7:0]:** • This field is the low-order eight bits of the BLT Transparent Color Mask. • When Graphics Controller Register GR30[3] = 1, the transparent color will be compared with the raster operation result under this mask. If it is equal, the result is not written to the destination. • A 1 in any bit location makes the corresponding compare a don't care.

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6.7.60 GR39: BLT Transparent Color Mask High Register

I/O Port Address: 3CF

Index: 39

Bit	Description	Reset State
7	BLT Transparent Color Mask [15]	0
6	BLT Transparent Color Mask [14]	0
5	BLT Transparent Color Mask [13]	0
4	BLT Transparent Color Mask [12]	0
3	BLT Transparent Color Mask [11]	0
2	BLT Transparent Color Mask [10]	0
1	BLT Transparent Color Mask [9]	0
0	BLT Transparent Color Mask [8]	0

This register contains the high-order eight bits of the 16-bit Transparent Color Mask.

Bit	Description
7:0	**BLT Transparent Color Mask [15:8]:** • This field is the high-order eight bits of the BLT Transparent Color Mask. • When Graphics Controller Register GR30[3] = 1, the transparent color will be compared with the raster operation result under this mask. If it is equal, the result is not written to the destination. • For 8-bit color modes, GR39 must equal GR38. • A 1 in any bit location makes the corresponding compare a don't care.

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6.7.61 CR19: Interlace End Register

I/O Port Address: 3?5

Index: 19

Bit	Description	Reset State
7	Interlace End [7]	0
6	Interlace End [6]	0
5	Interlace End [5]	0
4	Interlace End [4]	0
3	Interlace End [3]	0
2	Interlace End [2]	0
1	Interlace End [1]	0
0	Interlace End [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains the ending horizontal character count for the Odd Field VSYNC.

Bit	Description
7:0	**Interlace End:** • This value is the number of characters in the last scanline of the Odd Field in interlaced timing. • This value can be adjusted to center the scanlines in the Odd Field half-way between scanlines in the Even Field. • This register is typically programmed to approximately half of the Horizontal Total.

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6.7.62 CR1A: Miscellaneous Control Register

I/O Port Address: 3?5

Index: 1A

Bit	Description	Reset State
7	Vertical Blanking End Extension [9]	0
6	Vertical Blanking End Extension [8]	0
5	Horizontal Blanking End Extension [7]	0
4	Horizontal Blanking End Extension [6]	0
3	DAC Mode Switching / Overlay Mode Control [1]	0
2	DAC Mode Switching / Overlay Mode Control [0]	0
1	Enable Double Buffered Display Start Address	0
0	Enable Interlaced Timing	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains timing extension bits as well as some miscellaneous control bits.

Bit **Description**

7:6 **Vertical Blanking End Extension [9:8]:**
This two-bit field is used to extend the Vertical Blanking End value to 10 bits.
- These bits are enabled only when CR1B[5] is 1 or when CR1B[7] is 1.
- For more information on the functioning of these bits, refer to CR16.

5:4 **Horizontal Blanking End Extension [7:6]:**
This two-bit field is used to extend the Horizontal Blanking End value to 8 bits.
- These bits are enabled only when CR1B[5] is 1 or when CR1B[7] is 1.
- For more information on the functioning of these bits, refer to CR3[4:0].

3:2 **DAC Mode Switching / Overlay Mode Control [1:0]:**
This field is used to select DAC Mode Switching and Overlay Mode, as summarized in the following table. For more information, refer to Appendix A8.

CR1A [3]	CR1A [2]	DAC Mode Switching Enabled or Disabled	Overlay Mode Control
0	0	(Normal VGA-compatible operation.)	
		Disabled	No Overlay.
0	1	Enabled	Overlay controlled with FCEVIDEO#.
1	0	Enabled	Overlay controlled with color key and OVRW#.
1	1	Enabled	Overlay controlled with color key only.

Continued on next page.

6.7.62 CR1A: Miscellaneous Control Register *(cont.)*

Bit	Description
1	**Enable Double Buffered Display Start Address:** When this bit is 1, the Display Start Address will be updated on the VSYNC following a write to Start Address Low. This update provides control of display frame switching without the need to explicitly monitor VSYNC.
0	**Enable Interlaced Timing:** When this bit is 1, it enables interlaced timing. • In text mode, interlaced sync is enabled. • In graphics mode: — Both interlaced sync and video data are enabled. — For both interlaced sync and video data, the CRTC Scanline Double bit (CR9[7]) must be 0. — Graphics modes 4 and 6 must always be non-interlaced. • When this bit is 1, IRQ requests are generated only at the end of odd fields, that is, at the end of a frame.

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6.7.63 CR1B: Extended Display Controls Register

I/O Port Address: 3?5

Index: 1B

Bit	Description	Reset State
7	Enable Blanking End Extension	0
6	Enable Text Mode Fast-Page	0
5	Blanking Control	0
4	Offset Register Extension [8]	0
3	Screen A Start Address Bit [18]	0
2	Screen A Start Address Bit [17]	0
1	Enable Extended Address Wrap	0
0	Screen A Start Address Bit [16]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains miscellaneous bits that control extended display functions.

Bit	Description
7	**Enable Blanking End Extension:** • When this bit is 1, the Vertical and Horizontal Blanking End Extension bits of CR1A[7:6] and CR1A[5:4] are enabled, regardless of the CR1B[5] level. • When this bit is 0 and CR1B[5] = 0, the Vertical and Horizontal Blanking End Extension bits of CR1A[7:6] and CR1A[5:4] are disabled.
6	**Enable Text Mode Fast-Page:** • When this bit is 0, all font fetch cycles take place as random-read cycles. This bit must be 0 for standard VGA dual-font operation. • When this bit is 1, fast-page-mode cycles will be used to fetch font data. This setting allows for text modes with a VCLK greater than 30 MHz, as is required for 132-column modes.
5	**Blanking Control:** • When this bit is 0 (the standard VGA mode): — The blanking signal generated by the CRTC controls the DAC blanking. — The border can be used. (For more information, refer to AR11.) • When this bit is 1: — The display enable controls the DAC blanking. — The border cannot be used, as the blanking registers will no longer be available to control the border. Instead, the blanking registers are used to generate the OVRW# signal. — The DAC is blanked during the time the border is normally displayed. — The OVRW# pin is an output and follows the blanking signal generated by the CRTC. — The Vertical and Horizontal Blanking End Extension Bits in CR1A[7:4] are enabled and used to specify the active portion of the video overlay. For more information, refer to Appendix A8.

Continued on next page.

6.7.63 CR1B: Extended Display Controls Register *(cont.)*

Bit	Description
4	**Offset Register Extension [8]:** This bit is the most-significant ninth bit of the CRT Controller Offset field. For more information, refer to CRT Controller Offset Register CR13.
3:2	**Screen A Start Address Bits [18:17]:** These are the most-significant two bits of the CTR Controller Screen A Start Address Registers CRC and CRD. Bit 16 is in CR1B[0].
1	**Enable Extended Address Wrap:** • When this bit is 0, VGA compatibility is offered as follows: — the CRTC Character Address Counter is 16 bits wide. — the display memory address wraps at 64K maps (for 256K total memory). • When this bit is 1: — *and* Chain-4 addressing is selected (Sequencer Register SR4[3] = 1), then DRAM addresses MA[0] and MA[1] are supplied from addresses XMA[16] and XMA[17]. The other DRAM addresses are supplied from the XMA[18:12] addresses,which are the sum of bus addresses XA[16:12] and either Graphics Controller Offset Register 0 (GR9) or Offset Register 1 (GRA). — *and* CRTC Double Word addressing is selected (CR14[6] = 1), then DRAM addresses MA[0] and MA[1] are supplied from the CL-GD7542 internal CRT address counter addresses CR[14] and CR[15]. This action provides four displayable pages in video mode 13h. — the CL-GD7542 internal CRT character counter addresses CA[16] and CA[18] provide up to 256K bytes in each bit plane, or one Mbyte of packed-pixel memory. — the CL-GD7542 CRT controller address counter is 19 bits wide. — the display memory address wraps at the total available memory size.
0	**Screen A Start Address Bit [16]:** This is bit 16 of the Screen A Start Address. Bits 17 and 18 are in CR1B[3:2]. For more information, refer to CRT Controller Screen A Start Address Registers CRC and CRD.

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6.7.64 CR1D: Overlay Mode Register

I/O Port Address: 3?5

Index: 1D

Bit	Description	Reset State
7	Reserved	
6	Overlay Timing Signal Source	0
5	Reserved	
4	Reserved	
3	Reserved	
2	DAC Mode Switching Control [1]	0
1	DAC Mode Switching Control [0]	0
0	Reserved	

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register contains controls for the extended overlay modes.

Bit — **Description**

7 — **Reserved**

6 — **Overlay Timing Signal Source:**
- When this bit is 0, *and* Extension Register CR1A[3:2] = 01, the FCEVIDEO# input is used as the timing signal for the overlay modes.
- When this bit is 1, *and* Extension Register CR1A[3:2] = 10, the internally generated OVRW# output is used as the timing signal for the overlay modes. This bit setting eliminates the need to connect the OVRW# output to the FCEVIDEO# input.

5:3 — **Reserved**

2:1 — **DAC Mode Switching Control [1:0]:**
This field controls DAC mode switching. CR1A[3:2] selects the overlay mode.

CR1D		DAC Mode Switch State and Results		
[2]	[1]	DAC Mode Switch State	Result for: Background	Result for: Overlay Window Mode
0	0	True. Selected Extended DAC mode is enabled.	VGA data from display memory (typically mode 5F)	Live video (typically true color)
0	1	False. Selected Extended DAC mode is enabled6	Live video (typically true color)	VGA data from display memory (typically mode 5F)
1	X	Don't Care. Extended DAC mode is disabled.	-	-

0 — **Reserved**

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6.7.65 CR1E: LCD Shading

I/O Port Address: 3?5

Index: 1E

Bit	Description	Access	Reset State
7(MSB)	Shade Mapping [1]	R/W	0
6	Shade Mapping [0]	R/W	0
5	Reverse Video for Text Modes	R/W	0
4	Reverse Video for Graphics Modes	R/W	0
3	Reserved		
2	Horizontal CRTC Registers Access Control Override	R/W	0
1	Text-Mode Contrast Enhancement	R/W	0
0(LSB)	Graphics Mode Dithering Enable	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit — **Description**

7:6 **Shade Mapping [1:0]:**
These two bits are used to program monochrome grayscale mapping (that is, shading) according to the following table:

CR1E [7]	CR1E [6]	Shade Map
0	0	Graphics Mode. 18-bit output of Look-up Table converted to 64 shades, with NTSC weighting.
0	0	Reserved
1	0	Text Mode. Direct display of up to 16 or 64 shades of pixel data (4-bit planar, or lower 6 of 8 bits packed-pixel)
1	1	Reserved

5 **Reverse Video for Text Modes:**
When this bit is 1, all text modes are displayed in reverse video.

4 **Reverse Video for Graphics Modes:**
When this bit is 1, all graphics modes are displayed in reverse video.

3 Reserved

Continued on next page.

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6.7.65 CR1E: LCD Shading *(cont.)*

Bit — **Description**

2 — **Horizontal CRTC Registers Access Control Override:**
If this bit is 0:
- *and* the following conditions exist:
  - — CR20[5] = 1 (the LCD panel interface is enabled)
  - — R9X[3:2] = 01 (the LCD panel interface is set for 800 x 600 panel)
  - — CR2E[3:2] = 11 (horizontal expansion is on)
  - — CR2E[5] = 1 (horizontal centering is on)

  then standard CRT Controller Horizontal Registers CR0,2,3,4,5 are automatically used to control the CRT controller.
- *but* not all of the above conditions take place as described, then horizontal timing shadow registers RiY and RiZ are automatically used to control the CRT controller.

If this bit is 1:
- then the automatic selection described above is overridden, and horizontal timing shadow registers RiY and RiZ are automatically used to control the CRT controller.

1 — **Text-Mode Contrast Enhancement:**
This bit is used along with R8X[4] to enable text-mode contrast enhancement.

CR1E[1]	R8X[4]	Text-Mode Contrast-Enhancement Characteristics
0	0	No enhancement of text mode.
0	1	Foreground-only enhancement If BG > FG, then BGC = BG and FGC = 0. If BG < FG, then BGC = BG and FGC = 1.
1	0	Contrast enhancement If BG > FG, then BGC = BG and FGC = 0. If BG < FG, then BGC = 0 and FGC = FG.

BG = Background, FG = Foreground, xxC = Color

0 — **Graphics Mode Dithering Enable:**
This bit:
- = 1 to enable dithering in graphics mode.
- = 0 to disable dithering in non-packed pixel graphics mode.

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6.7.66 CR1F: LCD Modulation Control

I/O Port Address: 3?5

Index: 1F

Bit	Description	Access	Reset State
7(MSB)	External / Internal Modulation Control	R/W	0
6	MOD or Retrace LLCLK Control [6]	R/W	0
5	MOD or Retrace LLCLK Control [5]	R/W	0
4	MOD or Retrace LLCLK Control [4]	R/W	0
3	MOD or Retrace LLCLK Control [3]	R/W	0
2	MOD or Retrace LLCLK Control [2]	R/W	0
1	MOD or Retrace LLCLK Control [1]	R/W	0
0(LSB)	MOD or Retrace LLCLK Control [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used for one of two purposes:

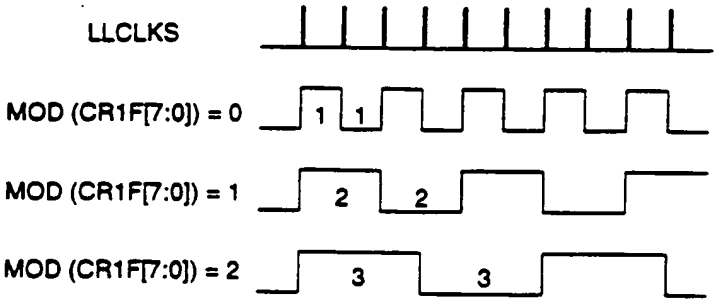
1. It controls the characteristics of the LCD Modulation (MOD) signal.
2. During vertical blanking, it generates extra line clocks (LLCLKs), which have two functions.
   a. They eliminate any "waterfall motion" (rolling lines appearing on the entire panel).
   b. They guarantee the panel receives a specific number of LLCLKS per frame.

Bit	Description
7	**External or Internal Modulation Control:** This bit controls the source of the modulation (MOD) signal for the LCD. • Clear this bit to 0 when an LCD needs an externally supplied MOD signal. — In this case, CR1F[6:0] can be used to program from 1 to 128 scanlines before MOD changes polarity. — Program CR1F[6:0] to determine the half-period of the square-wave output on the MOD pin, based on the programmed number of LLCLKs

Continued on next page.

6.7.66 CR1F: LCD Modulation Control *(cont.)*

Bit	Description
7(Cont.)	**External or Internal Modulation Control:** • When CR1F[7] = 0, the resulting value of the MOD signal is one more than the value that is programmed into CR1F[7:0]. — For example, if register bits CR1F[7:0] are programmed: — to 0, the half-period of the square-wave MOD output is 1. — to 1, the half-period of the square-wave MOD output is 2. — to 2, the half-period of the square-wave MOD output is 3.



	• Set this bit to 1 when the LCD generates its own internal MOD signal and does not require an externally supplied MOD signal. (In addition, set CR1F[6:0] appropriately, as described below.)
6:0	**MOD or Retrace LCD Line Clock (LLCLK) Control [6:0]:** • When CR1F[7] is 0: — The LCD requires an externally supplied MOD signal. — The contents of CR1F[6:0] can select up to 128 scanlines before the MOD signal changes polarity. • When CR1F[7] is 1: — The LCD generates its own internal MOD signal and does not require an externally supplied MOD signal. — For dual-scan LCDs, program CR1F[6:0] for only the number of LLCLKs that appear during vertical retrace (seen on every other half-frame of the LCD). — For single-scan LCDs, program CR1F[6:0] for the total number of LLCLKs for the entire frame of the LCD. — The contents of CR1F[6:0] are added to 180 hex (384 decimal) to determine the total number of LLCLKs. (The number 180 hex has been determined to allow a working range of LLCLKs.) Total number of LLCLKs = 180h + [value in (CR1F[6:0])]

6.7.67 CR20: Power Management Register

I/O Port Address: 3?5

Index: 20

Bit	Description	Access	Reset State
7(MSB)	Debounce Timer Resolution	R/W	0
6	CRT Enable	R/W	0
5	LCD Enable	R/W	0
4	Activate Standby Mode	R/W	0
3	Activate Suspend Mode	R/W	0
2	DRAM Refresh Select [1]	R/W	0
1	DRAM Refresh Select [0]	R/W	0
0(LSB)	Text Mode Shading Control	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Debounce Timer Resolution:** • When this bit is 0, the debounce-timer resolution = 30 µsec (32-kHz period). • When this bit is 1, the debounce-timer resolution = 1.0 sec.
6	**CRT Enable:** Setting this bit to 1 enables the analog CRT output from the video DAC.
5	**LCD Enable:** To enable the LCD interface, set this bit to 1. • When this bit has a transition that is : — low to high, the CL-GD7542 LCD power-up sequence will occur, which enables the internal LCD BIAS, backlight, logic supply, and drive signals. — high to low, the CL-GD7542 LCD power-down sequence will occur, which disables the internal LCD BIAS, backlight, logic supply, and drive signals. • When this bit is 1, the Line Frame Signal (LFS) and LCD Line Clock (LLCLK) timing signals for monochrome LCDs are generated. These bits are generated from the LCD Timing Registers, R0X through RBX. — For most TFT-color LCDs, the sync timing programmed by the CRT controller is used, in which case, specially compensated VSYNC and HSYNC signals are sent to the LFS and LLCLK outputs. — In addition, the display enable signal controls the display data. • When this bit is 1, some VGA register bits are redefined for LCDs as shown in the following table:

Continued on next page.

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6.7.67 CR20: Power Management Register *(cont.)*

Bit **Description**

5 (Cont.)

VGA-Defined Register Bits	New LCD Definition for Register Bits *When CR20[5] = 1*
AR13[3:0]	When Sequencer Register SR1[0] = 0 (DCLK is divided by 8) and when pixel panning, the shift effect of Attribute Controller Register AR13[3:0] is masked. As a result, a value of either 8h or 0h equals a "no shift".
MISC[7:6]	CRT sync polarity bits are redefined for External/General Register MISC[7:6] so that 00 = 800 x 600 LCD and 11 = 640 x 480 LCD.
SR1[0]	This bit is locked to 0 so that it is = 8 dots/character.
SR1[3]	Except for video mode 13, this bit selects the horizontally-locked timing for 40- or 80-column (character) modes.

NOTE: Clock select bits do not need to be locked. As required by the LCD, clock programming registers must be set for the same frequency.

4 **Activate Standby Mode:**
Setting this bit to 1 overrides the current internal Standby timer setting and immediately places the CL-GD7542 into Standby mode.

3 **Activate Suspend Mode:**
Setting this bit to 1 initiates software-controlled Suspend mode. In this mode, the power-down sequence is started to blank the LCD.

2:1 **DRAM Refresh Select:**
The programming of these two bits control the type of refresh applied to the display memory during Suspend mode as follows.

CR20 [2]	CR20 [1]	Display Memory Refresh Type
0	0	Refresh cycle 8 ms, CAS*-before-RAS*.
0	1	Refresh cycle 64-ms, CAS*-before-RAS*.
1	0	Self-refresh.
1	1	No refresh. All clock inputs are disabled. All outputs to display memory are high-impedance.

0 **Text Mode Shading Control:**
When this bit:
- is 0, text shades are derived directly from foreground/background data.
- is 1, text shades are derived the same way as graphics, with CR1E[7:6].

6.7.68 CR21: Power-Down Timer Control

I/O Port Address: 3?5

Index: 21

Bit	Description	Access	Reset State
7(MSB)	Timer for FPBL Control [3]	R/W	0
6	Timer for FPBL Control [2]	R/W	0
5	Timer for FPBL Control [1]	R/W	0
4	Timer for FPBL Control [0]	R/W	0
3	Timer for Standby Mode Control [3]	R/W	0
2	Timer for Standby Mode Control [2]	R/W	0
1	Timer for Standby Mode Control [1]	R/W	0
0(LSB)	Timer for Standby Mode Control [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register has two timers, each of which control the time at which power to the LCD is switched off.

- Programming CR21[7:4] controls the time it takes for the LCD backlight to switch off.
- Programming CR21[3:0] controls the time it takes for the Standby mode to be entered and power to the LCD to be switched off.

The timers operate as follows.

- Both timers may be set for times from 1 to 15 minutes.
- A programmed value of zero disables the timer.
- Instead of 60 seconds, the timers use 64 seconds for each "minute" programmed.
- The timers subtract a correcting factor of 32 seconds from the timed subtotal.
- For example, a setting of 15 minutes (Fh) will result in:
  [(15 counts X 64 seconds) – 32 seconds] =
  [(960 seconds) – 32 seconds] =
  928 seconds, or an actual time of (928 ÷ 60) = 15.5 minutes.

For typical power-down timer settings, refer to the table shown.

Bit	Description
7:4	**Timer for FPBL [3:0]:** These bits program the value for the internal flat panel backlight timer.
3:0	**Timer for Standby Mode Control [3:0]:** These bits program the value for the internal Standby mode timer.

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6.7.68 CR21: Power-Down Timer Control *(cont.)*

Table 6–6. Typical Power-Down Timer Settings

CR21 Backlight Timer Control Bits				Hex Code	Actual Seconds Programmed for Delay Time (Seconds)	Approximate Corresponding Delay Time (Minutes)
[7]	[6]	[5]	[4]			
CR21 Standby Mode Timer Control Bits						
[3]	[2]	[1]	[0]			
0	0	0	0	0h	disabled	disabled
0	0	0	1	1h	32	0.5
0	1	0	1	5h	288	4.8
0	1	1	1	7h	416	6.9
1	0	1	0	Ah	608	10.1
1	1	1	1	Fh	928	15.5

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6.7.69 CR23: SUSPI Debounce Timer

I/O Port Address: 3?5

Index: 23

Bit	Description	Access	Reset State
7(MSB)	SUSPI Debounce Timer [3]	R/W	0
6	SUSPI Debounce Timer [2]	R/W	0
5	SUSPI Debounce Timer [1]	R/W	0
4	SUSPI Debounce Timer [0]	R/W	0
3	FPBL Control Override	R/W	0
2	FPBL Output State	R/W	0
1	FPVCC Control Override	R/W	0
0(LSB)	FPVCC Output State	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit **Description**

7:4 **SUSPI Debounce Timer [3:0]:**
These bits define the number of seconds the input to the SUSPI pin must remain high and stable before the CL-GD7542 enters Suspend mode.

- The SUSPI debounce timer may be set for 1 to 15 seconds.
- A setting of 0000 disables the SUSPI debounce timer.

CR23				Setting for SUSPI Debounce Timer (seconds)
[3]	[2]	[1]	[0]	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	16

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Continued on next page.

6.7.69 CR23: SUSPI Debounce Timer *(cont.)*

Bit	Description
3	**FPBL Control Override:** Setting this bit to 1: • overrides the flat panel backlight (FPBL) Standby mode • enables CR23[2] to control the output state of the flat panel backlight
2	**FPBL Output State:** When CR23[3] = 1, this bit defines the flat panel backlight output state (1 or 0).
1	**FPVCC Control Override:** Setting this bit to 1: • overrides the flat panel VCC (FPVCC) Standby mode • enables CR23[0] to control the output state of the flat panel VCC
0	**FPVCC Output State:** When CR23[1] = 1, this bit defines the flat panel VCC output state (1 or 0).

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6.7.70 CR25: Manufacturing Revision ID Register

I/O Port Address: 3?5

Index: 25

Bit	Description	Reset State
7(MSB)	Manufacturing Revision ID [7]	'MFG revision'
6	Manufacturing Revision ID [6]	'MFG revision'
5	Manufacturing Revision ID [5]	'MFG revision'
4	Manufacturing Revision ID [4]	'MFG revision'
3	Manufacturing Revision ID [3]	'MFG revision'
2	Manufacturing Revision ID [2]	'MFG revision'
1	Manufacturing Revision ID [1]	'MFG revision'
0(LSB)	Manufacturing Revision ID [0]	'MFG revision'

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register is used for factory testing and internal tracking only. Application programs should not use this register.

Bit	Description
7:0	**Manufacturing Revision ID [7:0]:** • These bits are the least-significant eight bits of a ten-bit field that uniquely identifies the CL-GD7542 manufacturing revision level • The most-significant two bits are in CR27[1:0].

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6.7.71 CR27: Device ID and Manufacturing Revision ID Register

I/O Port Address: 3?5

Index: 27

Bit	Description	Reset State
7(MSB)	Device ID [5]	0
6	Device ID [4]	0
5	Device ID [3]	1
4	Device ID [2]	0
3	Device ID [1]	1
2	Device ID [0]	1
1	MFG Revision ID [9]	1
0(LSB)	MFG Revision ID [8]	1

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register will return in bits [7:2] a value that uniquely identifies the CL-GD7542.

Bit **Description**

7:2 **Device ID [5:0]:**
This five-bit field contains a unique value that identifies the CL-GD7542 as a Cirrus Logic product, according to the code below. The product code ID is given in both hex and binary values.

Product	Corresponding Product Code ID, in CR27[7:2]
CL-GD7542	28h (001011b)

1:0 **Manufacturing Revision ID [9:8]:**
- These bits are the two most-significant bits of a ten-bit field that uniquely identifies the CL-GD7542 manufacturing revision level
- The least-significant eight bits are in CR25[7:0].

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6.7.72 CR29: CL-GD7542 Configuration Status Register

I/O Port Address: 3?5

Index: 29

Bit	Description	Reset State
7(MSB)	Suspend Mode Status	0
6	32kHz Input Status	0
5	Power-Up/Power-Down Cycling Activity	0
4	Standby Mode Status	0
3	Reserved	
2	Reserved	
1	Reserved	
0(LSB)	Reserved	

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register identifies the configuration of the memory and bus interface selected for the chip.

Bit	Description
7	**Suspend Mode Status:** • This bit is 1 when the CL-GD7542 is in Suspend mode. This bit remains 1 from the time the clocks are stopped until 32 mseconds after the clocks are restarted, that is, until power-up sequencing is started. • While this bit is 1, the SUSPST# pin output remains low.
6	**32kHz Input Status:** This bit reflects the status of the 32-kHz input clock. • This bit is 1 when the 32-kHz input clock signal is high. • This bit is 0 when the 32-KHz input clock signal is low. • This bit can be used to create a software timer.
5	**Power-Up/Power-Down Cycling Activity:** • This bit is 1 while the CL-GD7542 is going through a power-up or power-down sequence. • This bit can be read in all modes except hardware-controlled Suspend mode, which locks out access to all registers.
4	**Standby Mode Status:** • This bit is 1 when the CL-GD7542 is in Standby mode. This bit remains 1 from the time the clocks are stopped until 32 mseconds after the clocks are restarted, that is, until power-up sequencing is started. • While this bit is 1, the SBYST# pin remains low.
3:0	Reserved

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6.7.73 CR2C: LCD Interface

I/O Port Address: 3?5

Index: 2C

Bit	Description	Reset State
7(MSB)	LCD Class Select [1]	0
6	LCD Class Select [0]	0
5	Write Protect Horizontal-Timing Shadow Registers	0
4	Select Set of Horizontal-Timing Shadow Registers	0
3	Write Protect CRT Controller Registers for LCD Timing	0
2	Reserved	
1	Invert LLCLK	0
0(LSB)	Invert LFS	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit **Description**

7:6 **LCD Class Select [1:0]:**
These two bits select the class of LCD to be connected. The following table lists available choices:

CR2C [7]	CR2C [6]	LCD Class Selected
0	0	Dual-scan monochrome LCD selected if CR2C[7:6] = 00 *and* R8X[5] = 0. Single-scan monochrome LCD selected if CR2C[7:6] = 00 *and* R8X[5] = 1.
0	1	Reserved
1	0	Dual-scan color STN LCD selected if CR2C[7:6] = 10 *and* SR21[6] = 1. Single-scan color STN LCD selected if CR2C[7:6] = 10 *and* SR21[6] = 0.
1	1	TFT-color LCDs selected.

5 **Write Protect Horizontal-Timing Shadow Registers:**

- When this bit is 0:
  - — The shadow horizontal timing registers RiY and RiZ (i = 0,2,3,4,5) are write-protected and cannot be accessed.
  - — Writing and reading applies only to standard VGA horizontal timing registers.
  - — Writing to standard VGA registers alone has no affect on CRTC timing.
- When this bit is 1:
  - — Writing is done to both the standard VGA horizontal timing registers and the shadow horizontal timing registers RiY and RiZ (i = 0,2,3,4,5).
  - — Reading is done only from the shadow registers.
- To access the standard VGA horizontal timing registers, this bit is a don't care.

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6.7.73 CR2C: LCD Interface *(cont.)*

Bit	Description
4	**Select Set of Horizontal-Timing Shadow Registers:** This bit selects which set of horizontal-timing shadow registers the CL-GD7542 uses. When CR2C[5] = 1 *and* this bit: • is 0, it selects registers R0Y to R5Y, used with the normal DCLK. • is 1, it selects registers R0Z to R5Z, used with DCLK ÷ 2. (For information on DCLK ÷ 2, refer to Sequencer Register SR1[3].)
3	**Write Protect CRT Controller Registers for LCD Timing:** For LCD operation, some CRT controller registers must be write protected, that is, the last data bits written are used for CRT controller timing control, and a read/write shadow register is enabled for any subsequent I/O. • When this bit is 1, the CRT Controller registers in the table below are write protected for LCD timing.
2	Reserved
1	**Invert LLCLK:** When this bit is 1, the LLCLK output is inverted.
0	**Invert LFS:** When this bit is 1, the LFS output is inverted.

CRT Controller Register / Bits	Description of CRT Controller Registers That Are Write Protected for LCD Timing
CR6 [7:0]	Vertical Total (Protected value is used.)
CR7 [7, 5, 2, 0]	Vertical Overflow bits for total and sync start
CR10 [7:0]	Vertical Retrace Start (Protected value is used for CRT VSYNC.)
CR11 [7:0]	Vertical Retrace End (Protected value is used for CRT VSYNC.)
CR15 [7:0]	Vertical Blanking Start
CR16 [7:0]	Vertical Blanking End

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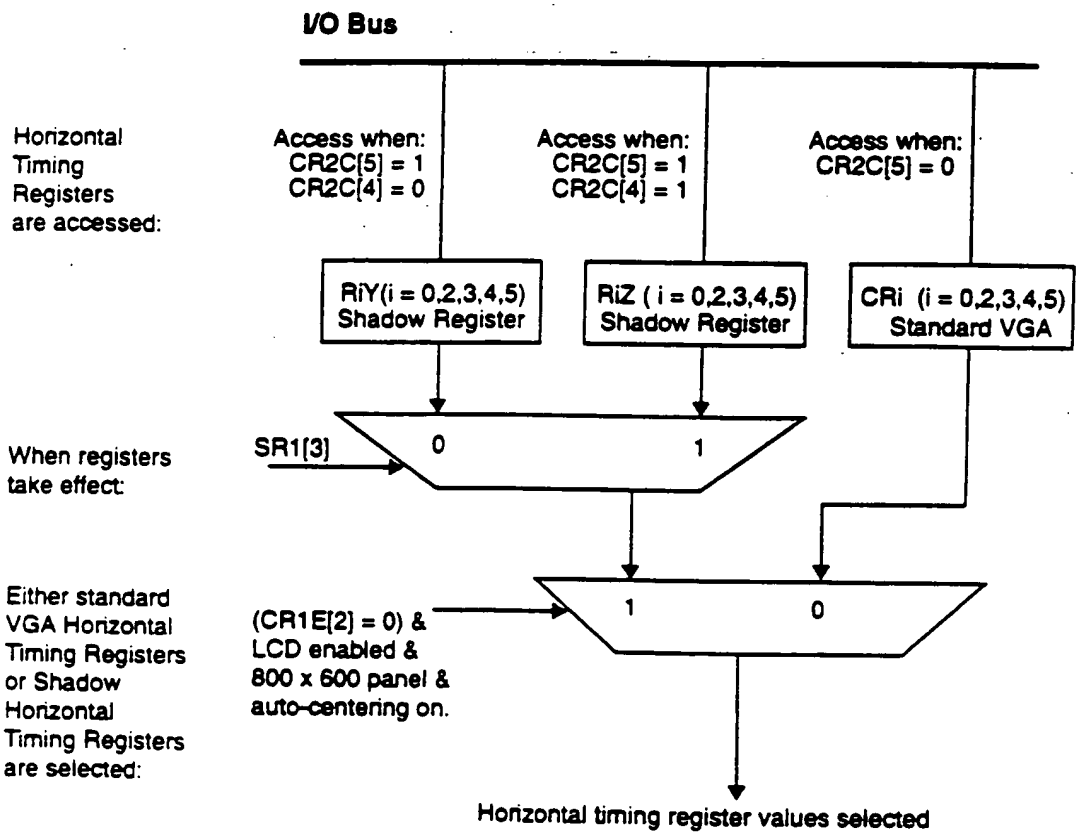


Figure 6–3 Horizontal Timing Register Values Selection

Table 6–7. Horizontal Timing Register References

CRi (Standard VGA) Horizontal (H) Timing Registers		Horizontal (H) Timing Shadow Registers			
		RiY Registers		RiZ Registers	
CR0	H Total	R0Y	H Total	R0Z	H Total
CR2	H Blanking Start	R2Y	H Blanking Start	R2Z	H Blanking Start
CR3	H Blanking End	R3Y	H Blanking End	R3Z	H Blanking End
CR4	H Sync Start	R4Y	H Sync Start	R4Z	H Sync Start
CR5	H Sync End	R5Y	H Sync End	R5Z	H Sync End

6.7.74 CR2D: LCD Display Controls

I/O Port Address: 3?5

Index: 2D

Bit	Description	Reset State
7(MSB)	Enable LCD Timing Registers	0
6	Enable ACTI to Reset Standby Timer	0
5	Enable VGA Access to Reset Standby Timer	0
4	Suspend Mode Clock Source	0
3	Enable ACTI to Reset Backlight Timer	0
2	Enable VGA Access to Reset Backlight Timer	0
1	Enable Vertical Auto-Expand for 640 x 480 LCDs	0
0(LSB)	Enable Auto-Center	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Enable LCD Timing Registers:** • The CRT Controller Index register (CRX) does not have bits to index the LCD timing registers (R2X to REX). Instead, CR2D[7] acts as an extra CRT Controller Index register bit to enable registers R2X to REX. • When this bit is 1, it enables read/write of the hidden LCD Timing Registers, R2X through REX, which are mapped at the standard CRTC locations. These special registers are used to control LLCLK, LFS, and other LCD control signals.
6	**Enable ACTI to Reset Standby Timer:** When this bit is set to 1, activity on the ACTI input pin will reset the internal Standby Timer.
5	**Enable VGA Access to Reset Standby Timer:** When this bit is set to 1, any valid VGA memory access will reset the internal Standby Timer.
4	**Suspend Mode Clock Source:** This bit selects the source for the clock used during Suspend mode. • When this bit is 0, a 32k-Hz clock must be connected to the 32-kHz pin. • When this bit is 0, *and* when the CL-GD7542 is in Suspend mode, the OSC input pin is disabled. • When this bit is set to 1, the 14M-Hz clock, required on the OSC input pin, will be divided by 432 to derive the 32k-Hz clock.
3	**Enable ACTI to Reset Backlight Timer:** When this bit is set to 1, activity on the ACTI input will reset the Backlight control timer for the LCD.
2	**Enable VGA Access to Reset Backlight Timer:** When this bit is set to 1, any valid VGA memory access will reset the Backlight control timer for the LCD.

Continued on next page.

6.7.74 CR2D: LCD Display Controls *(cont.)*

Bit **Description**

1 **Enable Vertical Auto-Expand for 640 x 480 LCDs:**
When this bit is 1, it enables automatic vertical expansion for 640 x 480 LCDs, as controlled by the sync polarity bits in External/General Register MISC[7:6].

MISC [7]	MISC [6]	Automatic Vertical Expansion
0	0	In CL-GD7542, used for 800 x 600 LCDs with more than 480 lines. Reserved in standard VGA.
0	1	400-line/200-line modes. 400-line mode is for text only. 200-line mode is for double-scanned graphics only.
1	0	350-line modes (text or graphics)
1	1	480-line mode (graphics only, no vertical expansion)

Expansion Method For Graphics Modes:

Original Number of Lines	Expansion Method for Graphics Modes
200	Pattern used is double-scan and triple-scan: 2,2,3,2,2,3,2,3 This pattern expands 200 lines to 475 lines by expanding every 8 lines to 19.
350	Pattern used is single-scan and double-scan: 1,1,2,1,1,2,1,2,1,1,2,1,1,2. This pattern expands 350 lines to 475 lines by expanding every 14 lines to 19.

Expansion Method For Text Modes:

Original Lines/ Font	Expansion Method for Text Modes
200 lines, 8 x 8 font	Normal double-scan is applied. An extra top line and 2 extra bottom lines are added to each character row (only when maximum row scan is set for 7 lines).
350 lines, 8 x 14 font	An extra 2 top lines and 3 extra bottom lines are added to each character row (only when maximum row scan is set for 14 lines).
400 lines, 8 x 16 font	An extra top line and 2 extra bottom lines are added to each character row (only when maximum row scan is set for 16 lines).

0 **Enable Auto-Center:**
When this bit is 1, and when auto-expand bit CR2D[1] is 0 (based on sync polarities), it enables LCD auto-centering. This action uses alternate LFS (Line-Frame Start) timing as programmed in LCD Timing registers R2X through REX.

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6.7.75 CR2E: High-Resolution LCD Control Register

I/O Port Address: 3?5

Index: 2E

Bit	Description	Reset State
7(MSB)	Expansion Select Override [1]	0
6	Expansion Select Override [0]	0
5	Horizontal Centering for 800 x 600 LCDs	0
4	10-Dot True Fonts	0
3	Horizontal Graphics Expansion for 800 x 600 LCDs	0
2	Horizontal Font Expansion for 800 x 600 LCDs	0
1	Vertical Graphics Expansion for 800 x 600 LCDs	0
0(LSB)	Text Expansion for 800 x 600 LCDs	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:6	**Expansion Select Override [1:0]:** • When these bits are 00, graphics expansion is controlled by CR2E[3,1]. • When these bits are 01, *and* R9X[3:2] bits are 01, an 800 x 600 LCD display size is selected. However, graphics expansion is disabled, even when bits CR2E[3,1] are set to 1. • Bit values 10 and 11 are reserved for future use.
5	**Horizontal Centering for 800 x 600 LCDs:** When this bit is 1, horizontal centering is enabled on 800 x 600 LCDs.
4	**10-Dot True Fonts:** When this bit is 1, and a text mode is selected, 10-dot true fonts are selected.
3	**Horizontal Graphics Expansion for 800 x 600 LCDs:** When this bit is 1, and a graphics mode is selected, horizontal graphics expansion is enabled, which replicates every fourth pixel. • For an 800 x 600 LCD, this bit is used to expand 640-pixel data of each scanline to 800-pixel data. • This bit does not work in 16-bit/pixel and 24-bit/pixel modes.
2	**Horizontal Font Expansion for 800 x 600 LCDs:** When this bit is 1, and a text mode is selected, 8-dot-wide true fonts are expanded to 10 dots wide (instead of the normal 9-dot-wide VGA expansion).
1	**Vertical Graphics Expansion for 800 x 600 LCDs:** When this bit is 1, and a graphics mode is selected, vertical graphics on 800 x 600 LCDs are expanded by: • doubling every odd scanline in 350-line and 400-line modes • replicating every fourth scanline in 480-line mode
0	**Text Expansion for 800 x 600 LCDs:** When this bit is 1, and a text mode is selected, the text font is expanded by: • doubling every odd scanline for 9 x 14 fonts or 8 x 16 fonts • tripling every scanline for 8 x 8 fonts

6.7.76 CR2F: Driver and BIOS Revision Register

I/O Port Address: 3?5

Index: 2F

Bit	Description	Reset State
7(MSB)	Driver Revision [3]	'Driver Revision'
6	Driver Revision [2]	'Driver Revision'
5	Driver Revision [1]	'Driver Revision'
4	Driver Revision [0]	'Driver Revision'
3	BIOS Revision [3]	'BIOS Revision'
2	BIOS Revision [2]	'BIOS Revision'
1	BIOS Revision [1]	'BIOS Revision'
0(LSB)	BIOS Revision [0]	'BIOS Revision'

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This read-only register will return two 4-bit codes that uniquely identifies the CL-GD7542 to drivers and to the BIOS.

Bit	Description
7:4	**Drivers Revision [3:0]:** This 4-bit field contains a 4-bit value that identifies the CL-GD7542 to various software drivers.
3:0	**BIOS Revision [3:0]:** This 4-bit field contains a 4-bit value that identifies the CL-GD7542 to the video BIOS.

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6.7.77 CR30: TV-OUT Control Register

I/O Port Address: 3?5

Index: 30

Bit	Description	Reset State
7(MSB)	PROG Pin-Level Control	0
6	Reserved	
5	Horizontal Total Dot-Clock Delay Control [1]	0
4	Horizontal Total Dot-Clock Delay Control [0]	0
3	TV-OUT Mode Enable	0
2	NTSC / PAL Output Control	0
1	CSYNC Dot-Clock Delay Control [1]	0
0(LSB)	CSYNC Dot-Clock Delay Control [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit — **Description**

7 — **PROG Pin-Level Control:**
This bit controls the logic level on the CL-GD7542 PROG output pin. When this bit is:
- a 1, the PROG pin level is high.
- a 0, the PROG pin level is low.

6 — Reserved

5:4 — **Horizontal Total Dot-Clock Delay Control [1:0]:**
The value in these bits control the dot-clock delay for the horizontal total signal according to the following table:

CR30		Dot-Clock Delay
[5]	[4]	
0	0	No Delay
0	1	Delay = 2 Dot Clocks
1	0	Delay = 4 Dot Clocks
1	1	Delay = 6 Dot Clocks

3 — **TV-OUT Mode Enable:**
- When this bit is 1, the TV-OUT mode is enabled, and TVON output is high.
- When this bit is 0, the NTSC/PAL, CSYNC, and TVON outputs are all forced low, and CR30[2] is disabled.
- When Extension Register External RAMDAC Address / Chip Select Enable SR25[6] = 1, the TVON pin is not controlled by CR30[3]. However, the TV-OUT feature can still be used without a power-down feature on CR30[3].

Continued on next page.

6.7.77 CR30: TV-OUT Control Register *(Cont.)*

Bit	Description
2	**NTSC / PAL Output Control:** This bit is programmed to reflect the required input levels to the NTSC/PAL encoder. When CR30[3]: • is 0, this bit is disabled. • is 1, *and* this bit: — is 0, this bit creates a low on the NTSC/PAL output pin. — is 1, this bit creates a high on the NTSC/PAL output pin
1:0	**CSYNC Dot-Clock Delay Control [1:0]:** The value in these bits control the dot-clock delay for the generation of a composite synchronization signal (CSYNC) according to the following table.

CR30		Horizontal CSYNC Start
[1]	[0]	
0	0	No Delay
0	1	Delay = 2 Dot Clocks
1	0	Delay = 4 Dot Clocks
1	1	Delay = 6 Dot Clocks

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6.7.78 CR33: MotionVideo™ Window Horizontal Start (XS) / Width (XW) Overflow

I/O Port Address: 3?5

Index: 33

Bit	Description	Reset State
7(MSB)	Reserved	0
6	MVW Horizontal Start (XS) [9]	0
5	MVW Horizontal Start (XS) [8]	0
4	Reserved	
3	MVW Horizontal Start (XW) [9]	0
2	MVW Horizontal Start (XW) [8]	0
1	Reserved	
0(LSB)	Enable Fast MVA FIFO Request	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

In the MVW (MotionVideo™ Window) architecture, the horizontal position is programmed using the number of memory cycles used by the surrounding pixel depth number environment.

Bit	Description
7	Reserved
6:5	**MVW Horizontal Start (XS) [9:8]:** These are the most-significant two bits of a ten-bit field that defines the horizontal starting position of the MotionVideo™ Window. For details, refer to Extension Register CR34.
4	Reserved
3:2	**MVW Horizontal Start (XW) [9:8]:** These are the most-significant two bits of a ten-bit field that defines the horizontal width of the MotionVideo™ Window. For details, refer to Extension Register CR35.
1	Reserved
0	**Enable Fast MVA FIFO Request:** This bit enables bypassing the synchronizer in the MotionVideo™ Window Architecture (MVA) circuitry to fill the FIFO faster.

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6.7.79 CR34: MotionVideo™ Window Horizontal Start (XS) Register

I/O Port Address: 3?5

Index: 34

Bit	Description	Reset State
7(MSB)	MVW Horizontal Start (XS) [7]	0
6	MVW Horizontal Start (XS) [6]	0
5	MVW Horizontal Start (XS) [5]	0
4	MVW Horizontal Start (XS) [4]	0
3	MVW Horizontal Start (XS) [3]	0
2	MVW Horizontal Start (XS) [2]	0
1	MVW Horizontal Start (XS) [1]	0
0(LSB)	MVW Horizontal Start (XS) [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

In the MVW (MotionVideo™ Window), the starting horizontal position is programmed by using the number of memory fetch cycles in the surrounding pixel-depth environment.

Bit	Description
7:0	**MVW Horizontal-Start (XS) [7:0]:** • These eight bits are the least-significant bits of a ten-bit field. • CR33[6:5] are the most-significant two bits of this field. To program XS, the horizontal coordinate to start the MVW on the screen: • Determine the number of the pixel at which the MVW will start. • Determine the surrounding pixel-depth environment, in bits per pixel. • Determine the size of the memory bus, which determines how many bits each memory fetch cycle transfers. • Obtain the number of pixels per memory fetch cycle by dividing the size of the memory bus by the number of bits in the surrounding pixel-depth environment. (If the memory bus is 32 bits wide, and 4 bits per pixel is used for the surrounding pixel-depth environment, then the number of pixels per memory fetch cycle is 8.) • Divide the number of the pixel at which the MVW will start by the number of pixels per memory fetch cycle. • Program the resulting value into CR34[7:0]. For example. If: A MVW is to start at pixel 16. The surrounding pixel-depth environment is 4 bits per pixel. The memory bus transfers 32 bits (32-bit memory fetch cycle). Then: The number of pixels per memory fetch cycle is 32 ÷ 4 = 8 . The number of memory fetch cycles needed for a MWV starting at pixel 16 will be 2. (Starting MVW value pixel number 16 ÷ 8 pixels per memory fetch cycle = 2 memory fetch cycles.) Program: into CR34[7:0] the value 2 as the number of memory fetch cycles needed for a MVW starting at pixel 16.

0 CR35: MotionVideo™ Window Horizontal Width (XW) Register

I/O Port Address: 3?5

Index: 35

Bit	Description	Reset State
7(MSB)	MVW Horizontal Width (XW) [7]	0
6	MVW Horizontal Width (XW) [6]	0
5	MVW Horizontal Width (XW) [5]	0
4	MVW Horizontal Width (XW) [4]	0
3	MVW Horizontal Width (XW) [3]	0
2	MVW Horizontal Width (XW) [2]	0
1	MVW Horizontal Width (XW) [1]	0
0(LSB)	MVW Horizontal Width (XW) [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

In the MVW (MotionVideo™ Window) architecture, the horizontal width of the MVW is calculated in memory fetch cycles, as explained below.

Bit	Description
7:0	**MVW Horizontal Width (XW) [7:0]:** • These eight bits are the least-significant bits of a ten-bit field. This field must be programmed for the MVW, even when the MVW is displayed on the full screen. • The most-significant bits of this field are in CR33[3:2]. To program the number of memory fetch cycles needed for the value of XW, the horizontal width: • Determine the panel's width in pixels. • Determine the color depth of the MVW display, in bits per pixel. • Determine the size of the memory bus, which determines how many bits each memory fetch cycle transfers. • Multiply the panel's width in pixels times the pixel depth. • Divide the above quantity by the number of bits each memory fetch cycle transfers. • Program the resulting value into CR35[7:0]. For example, if a panel is 320 pixels wide, the MVW display has a color depth of 16 bits per pixel, and the memory bus transfers 32 bits (32-bit memory fetch cycle) then: in memory fetch cycles, the MVW horizontal width is 160. [(320 pixels) x (16 bits/pixel)] ÷ [32 bits/memory fetch cycle] = 160 memory fetch cycles, which is the number to program into CR35[7:0].

EX

6.7

6.7.81 CR36: YUV-to-RGB Conversion and MVW Vertical-Position High Register

I/O Port Address: 3?5

Index: 36

Bit	Description	Reset State
7(MSB)	Force Linear Display Memory Map	0
6	Convert YUV to RGB with Standard Algorithm or Other	0
5	Convert YUV to RGB with Excess 128 or 2's Complement	0
4	MVW Memory-Address Offset [8]	0
3	MVW Vertical End (YE) Position [9]	0
2	MVW Vertical End (YE) Position [8]	0
1	MVW Vertical Start (YS) Position [9]	0
0(LSB)	MVW Vertical Start (YS) Position [8]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Force Linear Display Memory Map:** This bit is used to simplify the use of MVA drivers by providing a unique way of accessing the memory for MVW, from the CPU side. • When this bit is 1, the CPU linearly writes data to the display memory, the same way as in extended 8-bit-per-pixel packed-pixel modes. • Set this bit to 1, when writing to MVW memory and running Microsoft® Windows in 4-bit-per-pixel planar mode, to ensure that writes to MVW memory execute independently of surrounding graphics. • After executing writes to the MVW memory area, the Windows driver must set this bit to 0.
6	**Convert YUV to RGB with Standard Algorithm or Other:** • When this bit is 1, the YUV-to-RGB conversion uses the algorithm. R = Y + V; G = Y - 0.25U - 0.5V; B = Y + U • When this bit is 0, the YUV-to-RGB conversion uses the standard algorithm R = Y+ 1.375V; G = Y-.375U-.75V; B = Y+1.75U
5	**Convert YUV to RGB with Excess 128 or 2's Complement:** These conversions assume that U and V are expressed in either excess 128 or 2's complement notation. • When this bit is 1, the YUV-to-RGB conversion uses excess 128 notation. • When this bit is 0, the YUV-to-RGB conversion uses the 2's complement notation (that is, Philips SAA15B and SAA9051 TV decoders).
4	**MVW Memory-Address Offset [8]:** This is the most-significant bit of the MVW Memory-Address Offset Register CR3B.
3 2	**MVW Vertical End (YE) Position [9:8]:** These are the most-significant bits of the MVW Vertical End Register CR38.
1 0	**MVW Vertical Start (YS) Position [9:8]:** These are the most-significant bits of the MVW Vertical Start Register CR37.

6.7.82 CR37: MVW Vertical Start (YS) Position Register

I/O Port Address: 3?5

Index: 37

Bit	Description	Reset State
7(MSB)	MVW Vertical Start (YS) Position [7]	0
6	MVW Vertical Start (YS) Position [6]	0
5	MVW Vertical Start (YS) Position [5]	0
4	MVW Vertical Start (YS) Position [4]	0
3	MVW Vertical Start (YS) Position [3]	0
2	MVW Vertical Start (YS) Position [2]	0
1	MVW Vertical Start (YS) Position [1]	0
0(LSB)	MVW Vertical Start (YS) Position [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**MVW Vertical Start (YS) Position [7:0]:** • These are the 8 least-significant bits of the 10-bit field for the MVW Vertical Start (YS) Position. • The ten bits of this field: — define actual scanlines — are not affected by scanline doubling or LCD vertical expansion • The most-significant two bits are in register CR36[1:0].

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6.7.83 CR38: MVW Vertical End (YE) Position Register

I/O Port Address: 3?5

Index: 38

Bit	Description	Reset State
7(MSB)	MVW Vertical End (YE) Position [7]	0
6	MVW Vertical End (YE) Position [6]	0
5	MVW Vertical End (YE) Position [5]	0
4	MVW Vertical End (YE) Position [4]	0
3	MVW Vertical End (YE) Position [3]	0
2	MVW Vertical End (YE) Position [2]	0
1	MVW Vertical End (YE) Position [1]	0
0(LSB)	MVW Vertical End (YE) Position [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**MVW Vertical End (YE) Position [7:0]:** • These are the 8 least-significant bits of the 10-bit field for the MVW Vertical End (YE) Position. • The ten bits of this field: — define actual scanline — are not affected by scanline doubling or LCD vertical expansion • The most-significant two bits are in register CR36[3:2].

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6.7.84 CR39: MVW Surrounding-Address Offset Register

I/O Port Address: 3?5

Index: 39

Bit	Description	Reset State
7(MSB)	MVW Surrounding-Address Offset [7]	0
6	MVW Surrounding-Address Offset [6]	0
5	MVW Surrounding-Address Offset [5]	0
4	MVW Surrounding-Address Offset [4]	0
3	MVW Surrounding-Address Offset [3]	0
2	MVW Surrounding-Address Offset [2]	0
1	MVW Surrounding-Address Offset [1]	0
0(LSB)	MVW Surrounding-Address Offset [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines a value that is added to the CRT address counter of the display, so the counter value skips over the MotionVideo™ Window. This action allows the surrounding restart address to be defined without having to count through MVW.

Bit	Description
7:0	**MVW Surrounding-Address Offset [7:0]:** • The offset value in this register is added to the CRT address counter to allow the counter to skip over the area for the MotionVideo™ Window without having to count through it. • This offset value depends on the resolution of the surrounding mode. For example: Assume a scanline of 1024 pixels, and 8 bits/pixel (4 pixels/address). As a result, the largest offset value is 256 addresses. • To obtain a desired address offset, program this register for one-half of the desired offset. Example: Assume a 320-pixel-wide window with a surrounding resolution of 4 bits/ pixel. — A memory fetch has 8 pixels. — 320 pixels ÷ 8 pixels/address = 40-address offset — One-half of 40 is 20 decimal. — As a result, program 14h for the surrounding-address offset.

6.7.85 CR3A: MVW Memory-Address Start Register

I/O Port Address: 3?5

Index: 3A

Bit	Description	Reset State
7(MSB)	Reserved	
6	MVW Memory-Address Start [6]	0
5	MVW Memory-Address Start [5]	0
4	MVW Memory-Address Start [4]	0
3	MVW Memory-Address Start [3]	0
2	MVW Memory-Address Start [2]	0
1	MVW Memory-Address Start [1]	0
0(LSB)	MVW Memory-Address Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	Reserved
6:0	**MVW Memory-Address Start [6:0]:** This address is programmed in increments of 16 Kbytes (4K words). For example: • For 1 Mbyte, the physical address is 00000:3FFF F from the start of display memory. • For 2 Mbytes, the physical address is 00000:7FFF F from the start of display memory. Note: This start address must be aligned at a 16-Kbyte boundary in the CPU host address space.

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6.7.86 CR3B: MVW Memory-Address Offset Register

I/O Port Address: 3?5

Index: 3B

Bit	Description	Reset State
7(MSB)	MVW Memory-Address Offset [7]	0
6	MVW Memory-Address Offset [6]	0
5	MVW Memory-Address Offset [5]	0
4	MVW Memory-Address Offset [4]	0
3	MVW Memory-Address Offset [3]	0
2	MVW Memory-Address Offset [2]	0
1	MVW Memory-Address Offset [1]	0
0(LSB)	MVW Memory-Address Offset [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, along with the most-significant bit in CR36[4], defines an offset value.

Bit	Description
7:0	**MVW Memory-Address Offset [7:0]:** • These are the 8 least-significant bits of the 9-bit MVW memory-address offset value. This offset value is added to the present MVW Memory Start Address to get the next MVW Memory-Start Address. ADD: Present MVW Memory-Start Address AND: + MVW Memory-Address Offset (9-bit value) TO GET: = Next MVW Memory-Start Address • Using the MVW Memory-Address Offset to define the next memory-start address of the MVW allows panning through a large area of the MVW. The actual image stored in memory may be as large as 2K pixels at 16 bits/pixel. • The most-significant bit is in register CR36[4].

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6.7.87 CR3C: MVW Zoom, MVW Enable, and MVW Encoding Format Register

I/O Port Address: 3?5

Index: 3C

Bit	Description	Reset State
7(MSB)	MVW Horizontal Zoom	0
6	MVW Vertical Zoom	0
5	Full-Screen Live-Video Enable	0
4	MotionVideo™ Window Enable	0
3	Encoding Format for MotionVideo™ Window [3]	0
2	Encoding Format for MotionVideo™ Window [2]	0
1	Encoding Format for MotionVideo™ Window [1]	0
0(LSB)	Encoding Format for MotionVideo™ Window [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**MVW Horizontal Zoom:** When this bit is 1, each pixel is duplicated horizontally.
6	**MVW Vertical Zoom:** When this bit is 1, each pixel is duplicated vertically.
5	**Full-Screen Live-Video Enable:** When this bit is 1, the entire screen displays live video.
4	**MotionVideo™ Window Enable:** When this bit is 1, access is enabled to the MotionVideo™ Window registers CR33 through CR3B.
3:0	**Encoding Format for MotionVideo™ Window:** These bits define in which format the MVW is encoded.

CR3C[3:0]		Encoding Format for MVW
0h	0000	8-bit RGB 3:3:2 (data go through the palette RAMDAC)
1h	0001	16-bit RGB (5:5:5)
2h	0010	16-bit RGB XGA (5:6:5)
3h	0011	4:2:2 YUV Y0UY1V
4h	0100	4:1:1 YUV Linear Y0Y1Y2Y3UV
5h	0101	4:1:1 YUV Array Y0Y1Y2Y3UV, but Y2Y3 are in next scanline
8h	1000	24-bit RGB through MVA™
9h to 15h	1001 to 1111	Reserved for future formats

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6.7.88 CR3D: MotionVideo™ Window Horizontal-Pixel-Width Register

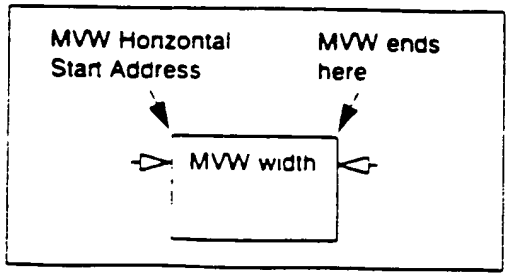
I/O Port Address: 3?5

Index: 3D

Bit	Description	Reset State
7(MSB)	Reserved	
6	MotionVideo™ Window Horizontal Pixel Width [6]	0
5	MotionVideo™ Window Horizontal Pixel Width [5]	0
4	MotionVideo™ Window Horizontal Pixel Width [4]	0
3	MotionVideo™ Window Horizontal Pixel Width [3]	0
2	MotionVideo™ Window Horizontal Pixel Width [2]	0
1	MotionVideo™ Window Horizontal Pixel Width [1]	0
0(LSB)	MotionVideo™ Window Horizontal Pixel Width [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	Reserved
6:0	**MotionVideo™ Window Horizontal Pixel Width [6:0]:** These bits contain a hex value used to define the MotionVideo™ Window width for each scanline the MVW is enabled. To calculate the value: • Determine the MVW's desired width, which must be at least 32 pixels wide. • From the desired width, subtract 24 pixels (three sets of eight pixels). • Divide the resulting number by 8-pixel increments. • Translate the resulting decimal number into a hex number. For example, to calculate the hex value for a 320-pixel wide MVW: DIVIDE: The quantity (320 pixels - 24 pixels = 296 pixels) BY: ÷ 8-pixel increments TO GET: = Value for a 320-pixel-wide MVW, which = 37 (decimal) = 25h Note: For CL-GD7542 version BC or later, the MVW width will be able to be expressed in 2-pixel increments.



LCD Display. with MotionVideo Window

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6.7.89 CR40: LCD Horizontal-Display-Enable Start Register – No Centering

I/O Port Address: 3?5

Index: 40

Bit	Description	Reset State
7(MSB)	LCD HDE Start [7]	0
6	LCD HDE Start [6]	0
5	LCD HDE Start [5]	0
4	LCD HDE Start [4]	0
3	LCD HDE Start [3]	0
2	LCD HDE Start [2]	0
1	LCD HDE Start [1]	0
0(LSB)	LCD HDE Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is one of four registers – CR40, CR41, CR42, and CR43 – used both to generate LCD horizontal timing and to center 640 x 480 and 800 x 600 LCDs.

Three registers – CR40, CR41, and CR42 – are complementary and mutually exclusive. They store the same timing-signal parameters, but values for the timing-signal parameters are usually different.

- Only one of these three registers is enabled at any time.
- The selection of which of these three registers control the LCD is done automatically, based on the conditions explained for each register.
- These three registers are generally programmed only once at power-on self-test.

The CR40 register is the default LCD HDE start register. The CL-GD7542 automatically selects it if:

- either CR41 or CR42 *are not* selected, or
- horizontal expansion *is* selected

In normal 24-bit LCD modes, the CL-GD7542 starts to send data to the LCD immediately after HDE start, which may cause problems for some graphics modes. These three registers may be programmed to avoid the problems.

For typical timing relationships, refer to Figure 6–4.

Continued on next page.

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6.7.89 CR40: LCD Horizontal-Display-Enable Start Register – No Centering *(Cont.)*

Bit	Description
7:0	**LCD HDE Start [7:0]:** When no horizontal centering is needed, this register defines: • LCD HDE start, the rising edge of the LCD horizontal display enable signal, relative to the previous CRT HDE start. • LLCLK, the rising edge of the LCD line clock signal, which starts one DCLK (dot clock) after the LCD HDE start. The LCD HDE start is expressed in 4-DCLK units, with CR43[1:0] defining a fine adjustment in 1-DCLK units. To calculate the LCD HDE start: DIVIDE: [(Number of CRT Horizontal Total pixels) minus 32 pixels BY: ÷ 4 (Number of 4-DCLK units) TO GET: = LCD HDE Start where Horizontal Total = CRT horizontal total in DCLK units. For example, for a 640 x 480 CRT, Horizontal Total = 800. LCD Line-Clock Start and the LCD HDE start signal for both 640 x 480 and 800 x 600 LCDs. A fine (dot-clock) adjustment for this register is in CR43[1:0].

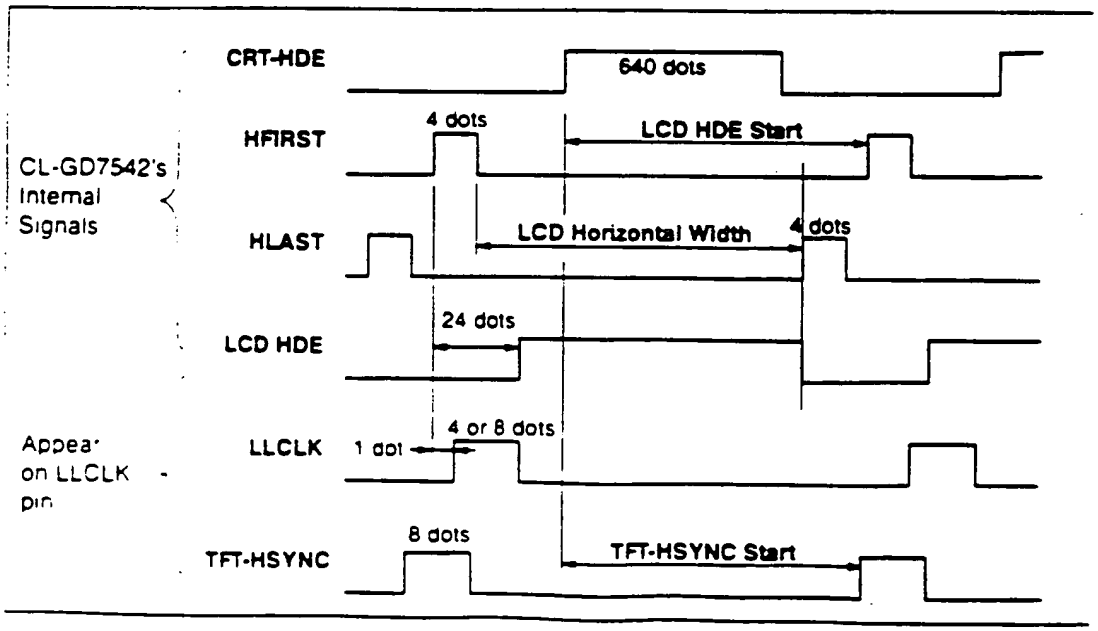


Figure 6–4 Horizontal Timing for 800 x 600 LCD Displaying 640 x 480 Picture

6.7.90 CR41: LCD Horizontal-Display-Enable Start to Center 720-Dot Display

I/O Port Address: 3?5

Index: 41

Bit	Description	Reset State
7(MSB)	LCD HDE Start to Center 720-Dot Display [7]	0
6	LCD HDE Start to Center 720-Dot Display [6]	0
5	LCD HDE Start to Center 720-Dot Display [5]	0
4	LCD HDE Start to Center 720-Dot Display [4]	0
3	LCD HDE Start to Center 720-Dot Display [3]	0
2	LCD HDE Start to Center 720-Dot Display [2]	0
1	LCD HDE Start to Center 720-Dot Display [1]	0
0(LSB)	LCD HDE Start to Center 720-Dot Display [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is one of four registers – CR40, CR41, CR42, and CR43 – used both to generate LCD horizontal timing and to center 640 x 480 and 800 x 600 LCDs. (For a description of all four registers and for the formula to calculate the LCD HDE start, refer to CR40.)

The CL-GD7542 automatically uses this register to provide centering of a 720-dot display (text or graphics) when all the following conditions are met:

- The LCD is an 800 x 600.
- The LCD is not using 800 x 600 graphics modes.
- The LCD is using a character clock of 9-DCLK cycles (in text mode), or CRT HDE > 50h (in graphics mode).
- The LCD is not using horizontal expansion.

Bit	Description
7:0	**LCD HDE Start to Center 720-Dot Display [7:0]:** This register provides centering of a 720-dot display (text or RiX graphics mode) on a 800 x 600 LCD by defining the present LCD HDE start signal. • This register defines the present HDE start signal, relative to the previous HDE start signal, in 4-DCLK increments. (The DCLK is never divided by two.) • The value programmed in this register is in 4-DCLK increments, and this value is one less than the HDE start parameter. • On a 800 x 600 LCD, the value in this register defines both the LCD line-clock start and the LCD HDE start signals. A fine adjustment for this register is in CR43[3:2]. • When horizontal expansion is enabled, instead of using this register to define the LCD HDE start signal, the value in CR40 is used to define the LCD HDE start signal.

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6.7.91 CR42: LCD Horizontal-Display-Enable Start to Center 640-Dot Display

I/O Port Address: 3?5

Index: 42

Bit	Description	Reset State
7(MSB)	LCD HDE Start to Center 640-Dot Display [7]	0
6	LCD HDE Start to Center 640-Dot Display [6]	0
5	LCD HDE Start to Center 640-Dot Display [5]	0
4	LCD HDE Start to Center 640-Dot Display [4]	0
3	LCD HDE Start to Center 640-Dot Display [3]	0
2	LCD HDE Start to Center 640-Dot Display [2]	0
1	LCD HDE Start to Center 640-Dot Display [1]	0
0(LSB)	LCD HDE Start to Center 640-Dot Display [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is one of four registers – CR40, CR41, CR42, and CR43 – used both to generate LCD horizontal timing and to center 640 x 480 and 800 x 600 LCDs. (For a description of all four registers and for the formula to calculate the LCD HDE start, refer to CR40.)

The CL-GD7542 automatically uses this register to provide centering of a 640-dot display (text or graphics) when all the following conditions are met:

- The LCD is an 800 x 600.
- The LCD is not using 800 x 600 graphics modes.
- The LCD is using a character clock of 8-DCLK cycles, and CRT HDE ≤ 50h.
- The LCD is not using horizontal expansion.

Bit	Description
7:0	**LCD HDE Start to Center 640-Dot Display [7:0]:** This register provides centering of a 640-dot display on a 800 x 600 LCD by defining the present LCD HDE start signal. • This register defines the present HDE start signal, relative to the previous HDE start signal, in 4-DCLK increments. (The DCLK is never divided by two.) • The value programmed in this register is in 4-DCLK increments, and this value is one less than the HDE start parameter. • On a 800 x 600 LCD, the value in this register defines both the LCD line-clock start and the LCD HDE start signals. A fine adjustment for this register is in CR43[5:4]. • When horizontal expansion is enabled, instead of using this register to define the LCD HDE start signal, the value in CR40 is used to define the LCD HDE start signal.

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6.7.92 CR43: LCD Dot-Clock-Delay Control Register

I/O Port Address: 3?5

Index: 43

Bit	Description	Reset State
7(MSB)	LCD Line-Clock Width [1]	0
6	LCD Line-Clock Width [0]	0
5	CR42 Fine Dot-Clock Delay [1]	0
4	CR42 Fine Dot-Clock Delay [0]	0
3	CR41 Fine Dot-Clock Delay [1]	0
2	CR41 Fine Dot-Clock Delay [0]	0
1	CR40 Fine Dot-Clock Delay [1]	0
0(LSB)	CR40 Fine Dot-Clock Delay [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is one of four registers – CR40, CR41, CR42, and CR43 – used both to generate LCD horizontal timing and to center 640 x 480 and 800 x 600 LCDs. (For a description of all four registers and for the formula to calculate the LCD HDE start, refer to CR40.)

Bits [7:6] set the LCD line clock width.

Bits [5:0] make up three fields that when required, compensate for the CL-GD7542's internal delays of the LCD horizontal display enable (HDE) start signal.

- For the different types of LCDs, these three fields make it possible to change the LCD horizontal display enable (HDE) start by adjusting the fine dot-clock delay in 1-DCLK units.
- When it is necessary to change the LCD horizontal display enable (HDE) start, automatic switching takes place between these three fields. The switching is based on the following:
  - — values in the CRT controller registers
  - — value in the sequencer registers
  - — the type of LCD used (that is, 640 x 480 or 800 x 600)

Note: Because LCD counters are reset 1 dot clock after resetting the CRT HDE Total counter, values in LCD registers must be programmed with a delay of one less than the model.

Bit	Description
7 6	**LCD Line-Clock Width [1:0]:** This two-bit field sets the LCK line-clock width in dot clocks, as shown in the following table.

CR43 [7]	CR43 [6]	LCD Line-Clock Width (in dot clocks)
0	0	4 dot clocks
0	1	8 dot clocks
1	0	Reserved
1	1	Reserved

Continued on next page.

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6.7.92 CR43: LCD Dot-Clock Delay-Control Register *(Cont.)*

Bit	Description
5:4	**CR42 Fine Dot-Clock Delay [1:0]:** To program the LCD HDE start signal for a dot-clock delay, refer to Table 6–8.
3:2	**CR41 Fine Dot-Clock Delay [1:0]:** To program the LCD HDE start signal for a dot-clock delay, refer to Table 6–8.
1:0	**CR40 Fine Dot-Clock Delay [1:0]:** To program the LCD HDE start signal for a dot-clock delay, refer to Table 6–8.

Table 6–8. Fine Dot-Clock Delay Options for LCD HDE Start Signals

CR43		Fine Dot-Clock Delay for:
[5]	[4]	CR42
[3]	[2]	CR41
[1]	[0]	CR40
0	0	No Delay
0	1	Delay LCD HDE Start by one DCLK
1	0	Delay LCD HDE Start by two DCLKs
1	1	Delay LCD HDE Start by three DCLKs

6.7.93 CR44: LCD Horizontal Display Width Register

I/O Port Address: 3?5

Index: 44

Bit	Description	Reset State
7(MSB)	LCD Horizontal Display Width [7]	0
6	LCD Horizontal Display Width [6]	0
5	LCD Horizontal Display Width [5]	0
4	LCD Horizontal Display Width [4]	0
3	LCD Horizontal Display Width [3]	0
2	LCD Horizontal Display Width [2]	0
1	LCD Horizontal Display Width [1]	0
0(LSB)	LCD Horizontal Display Width [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines the LCD horizontal width.

Bit	Description
7:0	**LCD Horizontal Display Width [7:0]:** The value programmed in this register: • defines the LCD horizontal display width, which can be different from the stored picture width. • is used to compensate for internal delays when displaying a narrow picture on a wide screen. • is never expressed in units of DCLK ÷ 2. • is the desired width (expressed in 4 DCLK increments), plus four, all expressed in hex. — For example, for a 640 (horizontal) x 480 (vertical) LCD, program A4h. — When the width of 640 is expressed in 4 DCLK increments = 640 ÷ 4 = 160, the desired width in 4 DCLK increments. — Desired width of 160, plus 4 = 164 decimal. — In hex, 164 decimal = A4 hex.

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6.7.94 CR47: TFT HSYNC Horizontal Start Position Register

I/O Port Address: 3?5

Index: 47

Bit	Description	Reset State
7(MSB)	TFT HSYNC Horizontal Start Position [7]	0
6	TFT HSYNC Horizontal Start Position [6]	0
5	TFT HSYNC Horizontal Start Position [5]	0
4	TFT HSYNC Horizontal Start Position [4]	0
3	TFT HSYNC Horizontal Start Position [3]	0
2	TFT HSYNC Horizontal Start Position [2]	0
1	TFT HSYNC Horizontal Start Position [1]	0
0(LSB)	TFT HSYNC Horizontal Start Position [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines the start of the TFT HSYNC signal. This register is not dependent on character-clock width or DCLK/2 control.

Bit	Description
7:0	**TFT HSYNC Horizontal Start Position [7:0]:** This register defines the exact starting position of the TFT HSYNC signal. The TFT HSYNC Horizontal Start Position: • is relative to the previous LCD CRT horizontal display enable (HDE) start, in DCLK/4 increments. • is about 144 dot clocks before the start of the LCD HDE start signal, which is also relative to the CRT HDE start. • can be adjusted in 1-DCLK increments with CR48[1:0] • When R7X[2] = 1, . — the TFT HSYNC signal, instead of the LLCLK signal, appears on the LLCLK pin. (The LLCLK signal always starts 1 DCLK after the LCD HDE start.) — This setup is needed to support TFT LCDs that require 144 dot clocks between LLCLK and the first shift clock on a scanline. Note: Some LCD manufacturers call the LLCLK signal HSYNC. Cirrus Logic calls this signal TFT HSYNC, to differentiate it from the CRT HSYNC signal.

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6.7.95 CR48: TFT HSYNC and LCD-Height Overflow Register

I/O Port Address: 3?5

Index: 48

Bit	Description	Reset State
7(MSB)	Reserved	
6	Reserved	
5	Vertical Size for LCDs [9]	0
4	Vertical Size for LCDs [8]	0
3	Reserved	
2	Vertical Size for Upper Half of Dual-Scan STN LCDs [8]	0
1	TFT HSYNC Dot-Clock Delay [1]	0
0(LSB)	TFT HSYNC Dot-Clock Delay [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:6	Reserved
5:4	**Vertical Size for LCDs [9:8]:** • These bits are the most-significant two bits of a ten-bit field that defines in scanlines the vertical size for one of the following: — the lower half of a dual-scan STN LCD — the total size of a single-scan LCD, either STN or TFT • The eight least-significant bits are in Extension Register CR4A[7:0].
3	Reserved
2	**Vertical Size for Upper Half of Dual-Scan STN LCDs [8]:** • This is the most-significant bit of a nine-bit field that defines in scanlines the vertical size for the upper half of a dual-scan STN LCD. • The least-significant eight bits are in Extension Register CR49[7:0].
1:0	**TFT HSYNC Dot-Clock Delay [1:0]:** • These bits provide further control, in 1-DCLK increments, for the TFT HSYNC horizontal start position defined in CR47 in 4-DCLK increments. • These bits control the dot-clock delay in 1-DCLK increments, according to the following table:

CR48		Dot-Clock Delay
[1]	[0]	
0	0	No Delay
0	1	Delay = 1 Dot Clock
1	0	Delay = 2 Dot Clocks
1	1	Delay = 3 Dot Clocks

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6.7.96 CR49: Vertical Size for Upper Half of Dual-Scan STN LCDs

I/O Port Address: 3?5

Index: 49

Bit	Description	Reset State
7(MSB)	Vertical Size for Upper Half of Dual-Scan STN LCDs [7]	0
6	Vertical Size for Upper Half of Dual-Scan STN LCDs [6]	0
5	Vertical Size for Upper Half of Dual-Scan STN LCDs [5]	0
4	Vertical Size for Upper Half of Dual-Scan STN LCDs [4]	0
3	Vertical Size for Upper Half of Dual-Scan STN LCDs [3]	0
2	Vertical Size for Upper Half of Dual-Scan STN LCDs [2]	0
1	Vertical Size for Upper Half of Dual-Scan STN LCDs [1]	0
0(LSB)	Vertical Size for Upper Half of Dual-Scan STN LCDs [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Vertical Size for Upper Half of Dual-Scan STN LCDs [7:0]:** • These bits are the least-significant eight bits of a nine-bit field that defines the vertical size in scanlines. • The most-significant ninth bit of this field is in CR48[2]. • This vertical display position is relative to the start of the first vertical pulse, which is ahead of the actual vertical display when the centering feature is enabled (using registers CR40 through CR43). • Up to 511 scanlines can be defined for display on the upper half of a dual-scan STN LCD. • The actual value in this register will be one less than the lines displayed. For example: — For an LCD using a 480-line mode, program 239. (1/2 x 480) = 240 lines being displayed for upper half. 240 - 1 = 239 — For an LCD using a 600-line mode, program 299. (1/2 x 600) = 300 lines being displayed for upper half. 300 - 1 = 299 Note: The number of lines programmed in this register represents actual displayed lines.

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CL 28754

6.7.97 CR4A: Vertical Size for LCDs

I/O Port Address: 3?5

Index: 4A

Bit	Description	Reset State
7(MSB)	Vertical Size for LCDs [7]	0
6	Vertical Size for LCDs [6]	0
5	Vertical Size for LCDs [5]	0
4	Vertical Size for LCDs [4]	0
3	Vertical Size for LCDs [3]	0
2	Vertical Size for LCDs [2]	0
1	Vertical Size for LCDs [1]	0
0(LSB)	Vertical Size for LCDs [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Vertical Size for LCDs [7:0]:** • These bits are the least-significant eight bits of a ten-bit field that defines the overall vertical size in scanlines for the LCD, regardless of whether the LCD is dual scan or single scan. • The vertical display position is relative to: — the start of the vertical mid-point on dual-scan LCDs — the first vertical pulse on single-scan LCDs • The actual value in this register will be two less than the total lines being displayed. (For example, for a 480-line display, program 478 lines.) • Dual-scan LCDs normally have the same amount of scanlines in both the upper and lower halves of the LCD. • The most-significant two bits of this field are in CR48[5:4].

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6.7.98 CR4B: Reserved — Scratch Pad Register

I/O Port Address: 3?5

Index: 4B

Bit	Description	Reset State
7(MSB)	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0(LSB)	Reserved	

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is reserved for the exclusive use of the CL-GD7542 BIOS, and must never be written by any application program.

Bit	Description
7:0	Reserved. This register is used as a scratch-pad register by the BIOS.

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6.7.99 CR4C: Input-Resolution Override for Dithering

I/O Port Address: 3?5

Index: 4C

Bit	Description	Reset State
7(MSB)	Input-Resolution Override Enable	0
6	Reserved	
5	Reserved	
4	Reserved	
3	Input Resolution Override [3]	0
2	Input Resolution Override [2]	0
1	Input Resolution Override [1]	0
0(LSB)	Input Resolution Override [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register, which is used with both TFT and STN LCDs, is used to change the CL-GD7542's default input resolution settings for the data sent to the dither block.

- When the MVA is enabled, this override register affects only the surrounding area.
- The MVW display is controlled by independent input and output resolution control bits.
- This register supports a maximum of 6 x 6 dithering.

Bit **Description**

7 **Input-Resolution Override Enable:**
When this bit:

- is 0, the settings from HDR (the Hidden DAC Register) apply, including the default input resolution settings shown in the table below:

Dithering Matrix	Default Input Resolution Settings
8 bits/gun	8-8-8 True Color Mode
6 bits/gun	All VGA-compatibility color modes
	All extended color modes that go through the palette RAMDAC
	5-6-5 High Color Mode
5 bits/gun	5-5-5 High Color Mode
3 bits/gun	3-3-2 Color Mode (does not go through the palette RAMDAC)

  - For the default input resolution settings, the CL-GD7542 dithers to maximize the number of colors displayed on an LCD.
- is 1, the default input resolution settings are overridden, and new input resolution values are defined in CR4C[3:0].
  - If the default input resolution settings are not desired, the BIOS can override them by programming any number between 0h and Fh. As a result, the CL-GD7542 can dither more or less than the default case.
  - As long as the dithering matrix is smaller than or equal to 6 x 6, the CL-GD7542 can support a combination of input and output resolutions.

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6.7.99 CR4C: Input-Resolution Override for Dithering *(Cont.)*

Bit	Description
6:4	Reserved
3:0	**Input Resolution Override [3:0]:** • When the CR4C[7] override enable bit is 1, the CR4C[3:0] bits define the new input-resolution values for data sent to the dithering block. • The hex value programmed in these bits define the number of bits per gun that the CL-GD7542 uses to control the dithering on an LCD, independent of the following: — the output resolution — the dithering state (enabled vs. disabled) — the CL-GD7542 mode (graphics vs. text)

CR4C				Dithering Result for LCD
[3]	[2]	[1]	[0]	
0	0	1	1	3 bits/gun
0	1	0	0	4 bits/gun
0	1	0	1	5 bits/gun
0	1	1	0	6 bits/gun
0	1	1	1	7 bits/gun
1	0	0	0	8 bits/gun

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6.7.99 CR4C: Input-Resolution Override for Dithering *(Cont.)*

Bit	Description
3:0 *(cont.)*	**Override Input Resolution [3:0]:**

Example 1:

When the given conditions are:
- Data comes from the 18-bit palette DAC color look-up table as 6 bits/gun.
- Colors displayed are 256.
- There are 8 bits/pixel.
- LCD is a 3 bits/gun TFT.

Then:
- The CL-GD7542 default input resolution is 6 bits/gun.
- The CL-GD7542 output resolution is 3 bits/gun.
- When 2 x 2 dithering is enough:
  - — The 6 bits/gun default input resolution is overridden with one of 5 bits/gun.
  - — Since 5 bits/gun - 3 bits/gun = 2 bits/gun, this leads to a 2 x 2 dithering and the equivalent of 5 bits/gun (2^5 = 32 colors per gun, or 32K colors).
- When 256K colors is not enough and a better effect is desired:
  - — More dithering is possible by programming an input resolution of 7 bits/gun.
  - — Since 7 bits/gun - 3 bits/gun = 4 bits/gun, this leads to a 4 x 4 dithering and the equivalent of 7 bits/gun (2^7 = 128 colors per gun, or 2M colors).

Example 2:

When the given conditions are:
- Colors displayed are 16.
- There are 8 bits/pixel.
- LCD is a color STN.
- The output resolution is programmed as 4 bits/gun (2^4 = 16).

Then:
- The CL-GD7542 default input resolution is 6 bits/gun.
  (Combining 2^4 = 16 colors with 2^2 = 4 color dithering results in $2^4 \times 2^2 = 2^6$ = 6 bits/gun.)
- By changing the output resolution to 3 bits/gun, the CL-GD7542 generates 2^3 = 8 colors.
- When the input resolution is 6 bits/gun, the CL-GD7542 does more dithering to get 6 bits/gun.
- When the input resolution is 4 bits/gun, the CL-GD7542 needs only 1 x 1 dithering to get a total of 16 equivalent colors per gun.

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CL 28759

6.7.100 CR4D: Output Resolution for Dithering

I/O Port Address: 3?5

Index: 4D

Bit	Description	Reset State
7(MSB)	MVA Output Resolution for Dithering [3]	0
6	MVA Output Resolution for Dithering [2]	0
5	MVA Output Resolution for Dithering [1]	0
4	MVA Output Resolution for Dithering [0]	0
3	Output Resolution for Dithering [3]	0
2	Output Resolution for Dithering [2]	0
1	Output Resolution for Dithering [1]	0
0(LSB)	Output Resolution for Dithering [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:4	**MVA Output Resolution for Dithering [3:0]:** These bits define the output resolution value for dithering exactly the same as CR4D[3:0] below, except they apply to the MotionVideo™ Window (MVW). These bits are active even when the MVW is displayed on the entire screen.
3:0	**Output Resolution for Dithering [3:0]:** These bits define typical output resolution values for dithering various LCDs. The hex value programmed in these bits define the number of bits per gun used by the CL-GD7542.

CR4D				Output Resolution for Dithering LCDs:	
[3]	[2]	[1]	[0]	TFT LCDs (No Frame-Rate Modulation)	STN LCDs (Frame-Rate Modulation Occurs)
0	0	0	1	Not applicable	2-shade STN LCDs: 1 bit/gun
0	0	1	0	Not applicable	4-shade STN LCDs: 2 bits/gun
0	0	1	1	3 bits/gun	8-shade STN LCDs: 3 bits/gun
0	1	0	0	4 bits/gun	16-shade STN LCDs: 4 bits/gun
0	1	1	0	6 bits/gun	Not applicable
1	0	0	0	8 bits/gun	Not applicable

Note: Programming values other than the ones specified in the above table may have unpredictable results. Also, the Reset value of zero is not a valid value. Therefore, **this register must be programmed at start-up with the correct output resolution for the LCD used (TFT or STN).**

6.7.101 CR4E: MVA Input-Resolution Override for Dithering

I/O Port Address: 3?5

Index: 4E

Bit	Description	Reset State
7(MSB)	MVA Input-Resolution Override Enable	0
6	Enable Dithering for the MVA	0
5	Reserved	
4	Reserved	
3	MVA Input Resolution Override [3]	0
2	MVA Input Resolution Override [2]	0
1	MVA Input Resolution Override [1]	0
0(LSB)	MVA Input Resolution Override [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is used to change the CL-GD7542's default resolution settings for the data sent to the dither block, either for the MVA window or for when the MVA fills the entire screen.

Bit — **Description**

7 — **MVA Input-Resolution Override Enable:**
When this bit:

- is 0, the settings from HDR (the Hidden DAC Register) apply, including the default input resolution settings shown in the table below:

Dithering Matrix	Default Input Resolution Settings
8 bits/gun	8-8-8 True Color Mode
6 bits/gun	All VGA-compatibility color modes
	All extended color modes that go through the palette RAMDAC
	5-6-5 High Color Mode
5 bits/gun	5-5-5 High Color Mode
3 bits/gun	3-3-2 Color Mode (does not go through the palette RAMDAC)

- is 1, the default input resolution settings for the MVA are overridden, and new values are defined in CR4E[3:0].

6 — **Enable Dithering for the MVA:**
When this bit is 1, MVA dithering is enabled.

5 4 — Reserved

Continued on next page.

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6.7.101 CR4E: MVA Input-Resolution Override for Dithering *(Cont.)*

Bit	Description
3:0	**MVA Input Resolution Override [3:0]:** • When the CR4E[7] override enable bit is 1, the CR4E[3:0] bits define the new input-resolution values for data sent to the dithering block, so that the amount of colors in MVW can differ from the surrounding area. • The hex value programmed can be any number between 1h and Fh. • The value programmed in these bits define the number of bits per gun that the CL-GD7542 uses to control the dithering on an LCD, independent of the following: — the output resolution — the dithering state (enabled vs. disabled) — the CL-GD7542 mode (graphics vs. text)

CR4E				Dithering Result for LCD
[3]	[2]	[1]	[0]	
0	0	1	1	3 bits/gun
0	1	0	0	4 bits/gun
0	1	0	1	5 bits/gun
0	1	1	0	6 bits/gun All data goes through the palette RAMDAC. Data may be either 4 or 8 bits/pixel.)
0	1	1	1	7 bits/gun
1	0	0	0	8 bits/gun. Includes: 8-8-8 RGB True Color Mode 8-bit True Color Mode YUV 4-2-2

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6.7.102 HDR: Hidden DAC Register

I/O Port Address: 3C6

Index: (n/a)

Bit	Description	Reset State
7	5-5-5 Extended Color Mode Enable	0
6	Extended Color Mode Select Bits Enable	0
5	Clocking Mode	0
4	32K Extended Color Mode Control	0
3	Extended Color Mode Select [3]	0
2	Extended Color Mode Select [2]	0
1	Extended Color Mode Select [1]	0
0	Extended Color Mode Select [0]	0

This register:

- is used to enable extended color modes, including the following:
  - — 15-bit/pixel extended color mode
  - — 16-bit/pixel extended color mode
  - — 24-bit/pixel extended color mode
- is accessed by reading four times in succession the External/General 3C6 Pixel Mask Register. The next write or read at 3C6 will then access the Hidden DAC Register.
  - — A *write* to the Hidden DAC Register resets the internal counter, and the four dummy reads of the 3C6 Pixel Mask Register must be executed again.
  - — A *read* from the Hidden DAC Register resets the internal counter, and the four dummy reads of the 3C6 Pixel Mask Register must be executed again.
  - — Reads from the 3C6 do not lock the Hidden DAC Register.
- is cleared to all zeroes at reset, putting the CL-GD7542 in VGA-compatibility mode.
- does not affect Motion Video Architecture modes.

Bit	Description
7	**5-5-5 Extended Color Mode Enable:** • When this bit is 0: — The extended color modes are disabled. — The Palette DAC is VGA-compatible. • When this bit is 1: — it enables the extended color modes (including the 5-5-5 extended color mode), as chosen by bit [6] and bits [3:0] of this register
6	**Extended Color Mode Select Bits Enable:** When bit [7] = 1, and this bit is: • 0, the extended color mode select bits [3:0] of this register are ignored, and the extended color mode will be the 5-5-5 mode. • 1, the extended color mode select bits [3:0] of this register are enabled to select an extended color mode (other than the 5-5-5 mode).

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6.7.102 HDR: Hidden DAC Register *(cont.)*

Bit **Description**

5 **Clocking Mode:**

- When this bit is 0, Clocking Mode 1 will be chosen. In Clocking Mode 1:
  - — 16-bit/pixel modes will use both edges of DCLK to latch data.
  - — The rising edge of DCLK will latch the least-significant byte, and the falling edge of DCLK will latch the most-significant byte.
- When this bit is 1, Clocking Mode 2 will be chosen. In Clocking Mode 2:
  - — 16-bit/pixel modes will use only the rising edge of DCLK to latch data.
  - — The DCLK must be supplied at twice the pixel rate.
  - — The first rising edge of DCLK will latch the least-significant byte, and the second rising edge of DCLK will latch the most-significant byte.

NOTE: All modes other than 16-bit/pixel use only the rising DCLK edge, regardless of this bit.

4 **32K Extended Color Mode Control:**

When this bit:

- is 0, a 5-5-5 extended color mode operation will take place normally.
- is 1 *and* Pixel Data Bit [15]:
  - — is a 0, then the 5-5-5 extended color mode operation that is chosen allows 5-5-5 data to overlay 256-color images on a pixel-by-pixel basis.
  - — is a 1, then Pixel Data Bits [7:0] choose a palette entry and Pixel Data Bits [14:8] are ignored.

3:0 **Extended Color Mode Select [3:0]:**

When HDR[7:6] = 11, this four-bit field selects an extended color mode according to the following table:

HDR						Color Mode	
[7]	[6]	[3]	[2]	[1]	[0]		
0	X	X	X	X	X	VGA Compatibility Color Mode	
1	0	X	X	X	X	Extended Color Modes	5-5-5
1	1	0	0	0	1		5-6-5 XGA™
1	1	0	1	0	1		8-8-8 16-million Color
1	1	0	1	1	X		DAC Power-Down
1	1	1	0	0	0		8-bit Grayscale
1	1	1	0	0	1		3-3-2 8-bit RGB

NOTE: Any undefined settings are reserved.

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6.7.103 R2X: LCD Timing — LFS Vertical Position #1 (MISC[7:6] = 11)

I/O Port Address: 3?5

Index: 2 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	LFS Vertical Position [7]	R/W	0
6	LFS Vertical Position [6]	R/W	0
5	LFS Vertical Position [5]	R/W	0
4	LFS Vertical Position [4]	R/W	0
3	LFS Vertical Position [3]	R/W	0
2	LFS Vertical Position [2]	R/W	0
1	LFS Vertical Position [1]	R/W	0
0(LSB)	LFS Vertical Position [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Register R2X (and Registers R3X, R4X, R5X, and RCX with overflow bits in R6X and REX) define in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal.

- At power-on self-test, these registers are programmed according to the type of LCD used.
- Which registers are automatically selected depends on the graphic modes that are selected and which expansion and centering options are selected.
- Refer to Table 6–10 for selection options.

Bit	Description
7:0	**LFS Vertical Position #1 [7:0]:** • These bits are the least-significant eight bits of a 10-bit field. The field's value defines in scanlines the vertical position of the line frame start (LFS) signal, relative to the CRT frame start signal. • For 640 x 480 LCDs, the R2X field is used when: — CR2D[1] = 0 (automatic vertical expansion is disabled). — CR2D[0] = 0 (automatic centering is disabled). — External/General Register MISC[7:6] = 11 (480 lines are displayed). • For 640 x 480 LCDs, the R2X field is used for *all* modes when: — CR2D[1] = 1 (automatic vertical expansion is enabled). — CR2D[0] = 0 (automatic centering is disabled). • For 800 x 600 LCDs, the R2X field is used in all cases: — CR2D[1] = 0 (automatic vertical expansion is disabled). — CR2D[0] = 0 (automatic centering is disabled). — *except* when External/General Register MISC[7:6] = 10 (350 lines are displayed). • The most-significant two bits of this field are stored in register R6X[7:6]. • For LFS Vertical-Position-Selection Logic Diagram, refer to Figure 6–5.

Continued on next page

6.7.103 R2X: LCD Timing — LFS Vertical Position #1 (MISC[7:6] = 11) – *(Cont.)*

Table 6–9. LFS Vertical Position Register Automatic Selection

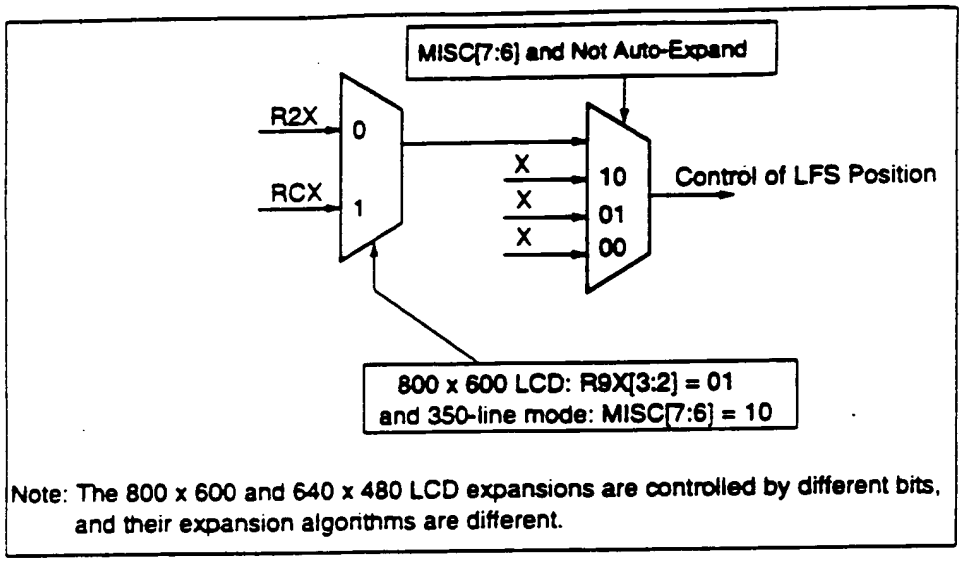
LFS Vertical Position Register Selected	Auto Vertical Expand	Auto Center	MISC[7:6]	Display Resolution Mode	LCD Size
R2X[7:0] and R6X[7:6]	Off	On	11	640 x 480	640 x 480
	On CR2D[1]	X	X	All display resolution modes	640 x 480
	On CR2E[1:0]	X	11, 01, 00	All display resolution modes except for 350 lines	800 x 600
R3X[7:0] and R6X[5:4]	Off	On CR2D[0]	10	640 x 350	640 x 480 or 800 x 600
R4X[7:0] and R6X[3:2]	Off	On CR2D[0]	01	640 x 400	640 x 480 or 800 x 600
	Off	On	01	720 x 400	800 x 600
R5X[7:0] and R6X[1:0]	Off	On	00	800 x 600	800 x 600
RCX[7:0] and REX[1:0]	On	X	10	640 x 350	800 x 600

a. Automatic vertical expansion is controlled by different registers, depending on the LCD size selected.
"Off" means all the appropriate bits are set to 0.
"On" means all the appropriate bits are set to 1.

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CL 28766

6.7.103 R2X: LCD Timing — LFS Vertical Position #1 (MISC[7:6] = 11) – *(Cont.)*



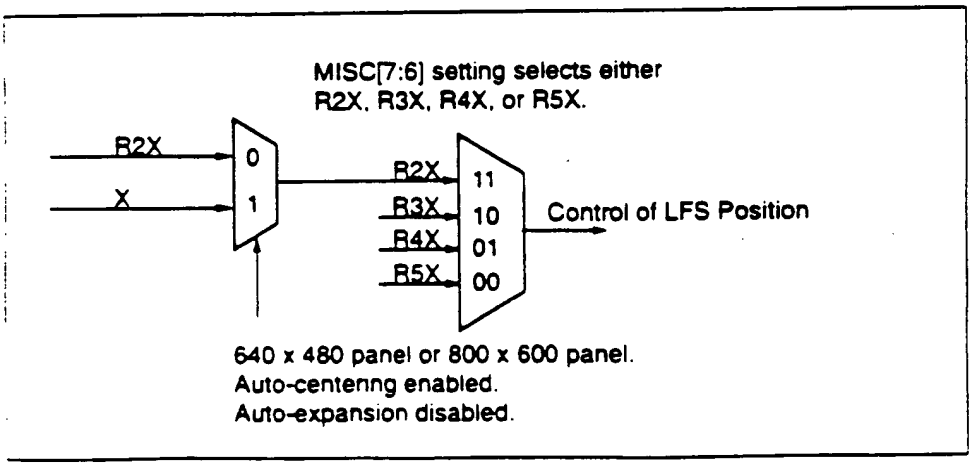


Figure 6–5. LFS Vertical-Position-Selection Logic Diagrams

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CL 28767

6.7.103 R2X: LCD Timing — LFS Vertical Position #1 (MISC[7:6] = 11) – *(Cont.)*

Table 6–10. LFS Vertical Position Register Automatic Selection

LFS Vertical Position Register Selected	Automatic Vertical Expansion	Automatic Centering	MISC [7]	MISC [6]	Display Resolution Mode	LCD Size
R2X[7:0] and R6X[7:6]	Off	On	1	1	640 x 480	640 x 480
	On CR2D[1]	X	X	X	All display resolution modes	640 x 480
	On CR2E[1:0]	X	1	1	All display resolution modes except for 350 lines	800 x 600
		X	0	1		
		X	0	0		
R3X[7:0] and R6X[5:4]	Off	On CR2D[0]	1	0	640 x 350	640 x 480 or 800 x 600
R4X[7:0] and R6X[3:2]	Off	On CR2D[0]	0	1	640 x 400	640 x 480 or 800 x 600
	Off	On	0	1	720 x 400	800 x 600
R5X[7:0] and R6X[1:0]	Off	On	0	0	800 x 600	800 x 600
RCX[7:0] and REX[1:0]	On	X	1	0	640 x 350	800 x 600

a. Automatic vertical expansion is controlled by different registers, depending on the LCD size selected.
"Off" means all the appropriate bits are set to 0.
"On" means all the appropriate bits are set to 1.

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6.7.104 R3X: LCD Timing — LFS Vertical Position #2 (MISC[7:6] = 10)

I/O Port Address: 3?5

Index: 3 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	LFS Vertical Position #2 [7]	R/W	0
6	LFS Vertical Position #2 [6]	R/W	0
5	LFS Vertical Position #2 [5]	R/W	0
4	LFS Vertical Position #2 [4]	R/W	0
3	LFS Vertical Position #2 [3]	R/W	0
2	LFS Vertical Position #2 [2]	R/W	0
1	LFS Vertical Position #2 [1]	R/W	0
0(LSB)	LFS Vertical Position #2 [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position #2 [7:0]:** • These bits are the least-significant eight bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — External/General Register MISC[7:6] = 10 (350 lines are displayed). — Extension Register CR2D[1] = 0 (automatic vertical expansion is disabled). — Extension Register CR2D[0] = 1 (automatic centering is enabled, when CR2D[1] = 0). • The most-significant two bits are stored in register R6X[5:4]. • For selection options, refer to Table 6–10.

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6.7.105 R4X: LCD Timing — LFS Vertical Position #3 (MISC[7:6] = 01)

I/O Port Address: 3?5

Index: 4 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	LFS Vertical Position #3 [7]	R/W	0
6	LFS Vertical Position #3 [6]	R/W	0
5	LFS Vertical Position #3 [5]	R/W	0
4	LFS Vertical Position #3 [4]	R/W	0
3	LFS Vertical Position #3 [3]	R/W	0
2	LFS Vertical Position #3 [2]	R/W	0
1	LFS Vertical Position #3 [1]	R/W	0
0(LSB)	LFS Vertical Position #3 [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position #3 [7:0]:** • These bits are the least-significant eight bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — External/General Register MISC[7:6] = 01 (400 lines are displayed). — Extension Register CR2D[1] = 0 (automatic vertical expansion is disabled). — Extension Register CR2D[0] = 1 (automatic centering is enabled, when CR2D[1] = 0). • The most-significant two bits are stored in register R6X[3:2]. • For selection options, refer to Table 6–10.

6.7.106 R5X: LCD Timing — LFS Vertical Position #4 (MISC[7:6] = 00)

I/O Port Address: 3?5

Index: 5 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	LFS Vertical Position #4 [7]	R/W	0
6	LFS Vertical Position #4 [6]	R/W	0
5	LFS Vertical Position #4 [5]	R/W	0
4	LFS Vertical Position #4 [4]	R/W	0
3	LFS Vertical Position #4 [3]	R/W	0
2	LFS Vertical Position #4 [2]	R/W	0
1	LFS Vertical Position #4 [1]	R/W	0
0(LSB)	LFS Vertical Position #4 [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position #4 [7:0]:** • These bits are the least-significant eight bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — External/General Register MISC[7:6] = 00. — Extension Register CR2D[1] = 0 (automatic vertical expansion is disabled). — Extension Register CR2D[0] = 1 (automatic centering is enabled, when CR2D[1] = 0). • The most-significant two bits are stored in register R6X[1:0]. • For selection options, refer to Table 6–10.

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CL 28771

6.7.107 R6X: LCD Timing — Overflow Bits for LFS Signal Compare

I/O Port Address: 3?5

Index: 6 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	R2X LFS Vertical Position #1 [9]	R/W	0
6	R2X LFS Vertical Position #1 [8]	R/W	0
5	R3X LFS Vertical Position #2 [9]	R/W	0
4	R3X LFS Vertical Position #2 [8]	R/W	0
3	R4X LFS Vertical Position #3 [9]	R/W	0
2	R4X LFS Vertical Position #3 [8]	R/W	0
1	R5X LFS Vertical Position #4 [9]	R/W	0
0(LSB)	R5X LFS Vertical Position #4 [8]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register defines the two most-significant overflow bits for the LFS Vertical Position registers R2X, R3X, R4X, and R5X.

Bit	Description
7:6	**R2X LFS Vertical Position #1 [9:8]:** When External/General Register MISC[7:6] = 11, these are the most-significant two bits of register R2X, creating a 10-bit value.
5:4	**R3X LFS Vertical Position #2 [9:8]:** When External/General Register MISC[7:6] = 10, these are the most-significant two bits of register R3X, creating a 10-bit value.
3:2	**R4X LFS Vertical Position #3 [9:8]:** When External/General Register MISC[7:6] = 01, these are the most-significant two bits of register R4X, creating a 10-bit value.
1:0	**R5X LFS Vertical Position #4 [9:8]:** When External/General Register MISC[7:6] = 00, these are the most-significant two bits of register R5X, creating a 10-bit value.

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CL 28772

6.7.108 R7X: LCD Timing — LCD Signal Control for Color TFT LCDs

I/O Port Address: 3?5

Index: 7 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	LFS Output	R/W	0
2	LLCLK Output	R/W	0
1	FPVDCLK Inversion	R/W	0
0(LSB)	Free-Running FPVDCLK for TFT LCDs	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:4	Reserved
3	**LFS Output:** In both of the following cases, the line frame signal (LFS) output is controlled by the first vertical pulse, which marks the beginning of the LCD display. • When this bit is 0: — the LFS output pin drives both STN and DE-type TFT LCDs. — the LFS output (which may also be called FLM) is one line wide and is programmable. • When this bit is 1: — the LFS output pin drives the VSYNC input for non-DE-type TFT LCDs. — the LFS output (which may also be called TFT-VSYNC) is two lines wide and can support only single-scan LCDs. • Set this bit to 1 for Matsushita TFT LCDs.

Continued on next page.

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CL 28773

6.7.108 R7X: LCD Timing — LCD Signal Control for Color TFT LCDs *(Cont.)*

Bit	Description
2	**LLCLK Output:** • When this bit is 0: — The LLCLK output pin drives both STN and DE-type TFT LCDs. — The LLCLK signal position is controlled by "LCD Horizontal Display Enable Start" values stored in Extension Registers CR40 to CR42, and Extension Register CR43 is used for fine positioning. — The LLCLK signal starts with the HFirst pulse. (Refer to the timing diagram within the description of the Extension Register CR40.) — The LLCLK signal is always 25 dot clocks before the LCD display enable start signal. • When this bit is 1: — Tie LFS to VSYNC. (Refer to Extension Register R7X[3].) • This bit must be set to 1 for: — non-DE-type TFT LCDs. — LCDs that require an offset different than 25 dot clocks between the LLCLK (or LCD HSYNC) signal and the LCD display enable start signal. For instance, some LCDs require an offset of 144 dot clocks between LLCLK and the first LCD shift clock. In this case, set R7X[2] = 1, which places the LLCLK output under the control of Extension Register CR47[7:0].
1	**FPVDCLK Inversion:** This bit can be used with all LCDs. • When this bit is: — 1, the FPVDCLK signal is inverted, and LCD data are latched on the low-to-high transition of FPVDCLK. — 0, the FPVDCLK signal is not inverted, and LCD data are latched on the high-to-low transition of FPVDCLK. • During Suspend mode, FPVDCLK is forced low, independent of this bit's polarity.
0	**Free-Running FPVDCLK Enable for TFT LCDs:** Set this bit to 1 only for TFT LCDs that have a display enable input pin. When this bit: • = 1, and when the LCD power sequence is on, FPVDCLK is always active (free-running) for TFT LCDs. • = 0, FPVDCLK is gated by the display enable signal and remains active only during display time.

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CL 28774

6.7.109 R8X: LCD Timing — Shift Clock and Data Format Select for STN LCDs

I/O Port Address: 3?5

Index: 8 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	Horizontal Cross-Talk Reduction Enable	R/W	0
6	Vertical Cross-Talk Reduction Disable	R/W	0
5	Dual-Scan/Single-Scan Monochrome LCD Select	R/W	0
4	Foreground-Only Text Enhancement	R/W	0
3	Reserved		0
2	Reserved		
1	Dual/Single Shift-Clock Select for STN LCDs	R/W	0
0(LSB)	16-Bit / 8-Bit Data-Interface Select for STN LCDs	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Horizontal Cross-Talk Reduction Enable:** When this bit is 1, horizontal cross-talk reduction is enabled. This bit is a test bit, and it must never be written by any application program. It is listed here only for completeness.
6	**Vertical Cross-Talk Reduction Disable:** When this bit is 1, vertical cross-talk reduction is disabled. This bit is a test bit, and it must never be written by any application program. It is listed here only for completeness.
5	**Dual-Scan/Single-Scan Monochrome LCD Select:** • When this bit is 0, dual-scan monochrome LCDs are selected. • When this bit is 1, single-scan monochrome LCDs are selected.
4	**Foreground-Only Text Enhancement:** • When this bit is 0, normal text is displayed. • When this bit is 1 and Extension Register CR1E[1] = 1, the foreground-only text enhancement is enabled.
3:2	Reserved
1	**Dual/Single Shift-Clock Select for STN LCDs:** On an STN LCD, when this bit: • = 0, a single-shift clock is supplied to the FPVDCLK pin. • = 1, dual-shift clocks are supplied to the FPVDCLK and FPDE pins.
0	**16-Bit / 8-Bit Data-Interface Select for STN LCDs:** • On an STN LCD, when this bit is 0, a 16-bit data LCD interface is selected. • On an STN LCD, when this bit is 1, an 8-bit data LCD interface is selected.

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6.7.110 R9X: LCD Size and TFT LCD Data Format

I/O Port Address: 3?5

Index: 9 — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	LCD Size [1]	R/W	0
2	LCD Size [0]	R/W	0
1	TFT LCD Data Format [1]	R/W	0
0(LSB)	TFT LCD Data Format [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit 7:4 — Reserved

Bit 3:2 — LCD Size [1:0]:
These two bits select the LCD size as shown in the table below. For information on specific LCD types and for detailed connection information, refer to the *Guide to Interfacing Panels to the CL-GD7542*.

R9X [3]	R9X [2]	LCD Size	LCD Types to Which LCD Size Can Be Applied
0	0	640 x 480	STN and TFT
0	1	800 x 600	STN and TFT
1	0	Reserved	—
1	1	Reserved	—

Bit 1:0 — TFT LCD Data Format [1:0]:
These two bits select the data format for TFT LCDs as shown in the table below. For information on specific LCD types and for detailed connection information, refer to the *Guide to Interfacing Panels to the CL-GD7542*.

R9X [1]	R9X [0]	TFT LCD Data Format
0	0	9-bit (333)
0	1	12-bit (444)
1	0	18-bit (666)
1	1	24-bit (888)

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CL 28776

6.7.111 RBX: Shade Conversion and Extra LCD Line Clock Insertion

I/O Port Address: 3?5

Index: B — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Shades 7 and 9 Convert	R/W	0
3	Shades 5 and 11 Convert	R/W	0
2	Extra LCD Line Clock Enable [2]	R/W	0
1	Extra LCD Line Clock Enable [1]	R/W	0
0(LSB)	Extra LCD Line Clock Enable [0]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:5	Reserved
4	**Shades 7 and 9 Convert:** When this bit is 1: • shade 7 is converted to shade 6. • shade 9 is converted to shade 8.
3	**Shades 5 and 11 Convert:** When this bit is 1: • shade 5 is converted to shade 4. • shade 11 is converted to shade 10.
2:0	**Extra LCD Line Clock Enable [2:0]:** The hex value in these three bits define up to five extra LCD line clocks, which can be inserted between the upper and lower half of a dual-scan LCD. • Extra line clocks are needed for those LCD manufacturers who disconnect the first one or two row drivers on the lower half of a dual-scan LCD. • These bits generate extra line clocks for disconnected row drivers.

RBX			Result
[2]	[1]	[0]	
0	0	0	0 extra LCD line clocks
0	0	1	1 extra LCD line clock
0	1	0	2 extra LCD line clocks
0	1	1	3 extra LCD line clocks
1	0	0	4 extra LCD line clocks
1	0	1	5 extra LCD line clocks

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CL 28777

6.7.112 RCX: LFS Vertical Position for 525-Line Modes

I/O Port Address: 3?5

Index: C — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Reset State
7	LFS Vertical Position for 525-Line Modes [7]	0
6	LFS Vertical Position for 525-Line Modes [6]	0
5	LFS Vertical Position for 525-Line Modes [5]	0
4	LFS Vertical Position for 525-Line Modes [4]	0
3	LFS Vertical Position for 525-Line Modes [3]	0
2	LFS Vertical Position for 525-Line Modes [2]	0
1	LFS Vertical Position for 525-Line Modes [1]	0
0	LFS Vertical Position for 525-Line Modes [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

For 800 x 600 LCDs, this register is used:

- to expand the 350 lines resulting from a 350-line mode to 525 lines and then to center the 525 lines
- to define in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position for 525-Line Modes [7:0]:** • These bits are the least-significant eight bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — The LCD is a 525-line LCD, or the LCD is one that uses a 525-line mode that has been expanded to 600 lines. — External/General Register MISC[7:6] = 10 (350 lines are displayed). — Video modes 10 or F are being used. (These modes display 350 lines.) — Extension Register CR2D[1] = 1 (automatic vertical expansion is enabled). • The most-significant two bits of this field are in REX[1:0]. • For selection options, refer to to Table 6–10.

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CL 28778

6.7.113 RDX: LCD Timing — LFS Vertical Position #6

I/O Port Address: 3?5

Index: D — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Reserved		
0(LSB)	Reserved		

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

This register is reserved.

Bit	Description
7:0	Reserved

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CL 28779

6.7.114 REX: Overflow Bits for RCX Register

I/O Port Address: 3?5

Index: E — This register is accessible only when Extension Register CR2D[7] = 1.

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	RCX: LFS Vertical Position for 525-Line Modes [9]	R/W	0
0	RCX: LFS Vertical Position for 525-Line Modes [8]	R/W	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:2	Reserved
1:0	**RCX LFS Vertical Position for 525-Line Modes [9:8]:** • These two overflow bits are the most-significant bits of a 10-bit field, LFS Vertical Position for 525-line modes. • For more information, refer to RCX[7:0], which contain the least-significant bits for this field.

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CL 28780

6.7.115 R0Y: Horizontal Total Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 10.

Bit	Description	Reset State
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

The RiY (i = 0,2,3,4,5) Extension Registers are horizontal timing shadow registers.

- These registers are used to automatically control the CRT controller on 640 x 480 and 800 x 600 LCDs, for both low-resolution and high-resolution applications.
- These registers control LCD timing independent of VGA modes.

Bit	Description
7:0	**Horizontal Total [7:0]:** When Sequencer Register SR1[3] = 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller Register CR0[7:0]).

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CL 28781

6.7.116 R2Y: Horizontal Blanking Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 10.

Bit	Description	Reset State
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** When Sequencer Register SR1[3] = 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller Register CR2[7:0].

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CL 28782

6.7.117 R3Y: Horizontal Blanking End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 10.

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:5	Reserved
4:0	**Horizontal Blanking End [4:0]:** When Sequencer Register SR1[3] = 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller Register CR3[4:0]. • These bits are the least-significant five bits of a 6-bit word controlling the horizontal blanking end signal. • The most-significant bit that controls the horizontal blanking end signal is in Extension Register R5Y[7].

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CL 28783

6.7.118 R4Y: Horizontal Sync Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 10.

Bit	Description	Reset State
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** When Sequencer Register SR1[3] = 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller Register CR4[7:0].

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CL 28784

6.7.119 R5Y: Horizontal Sync End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 10.

Bit	Description	Reset State
7	Horizontal Blanking End [5]	0
6	Reserved	
5	Reserved	
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Horizontal Blanking End [5]:** • This is the most-significant bit for the six-bit horizontal blanking end signal. • The least-significant five bits of the horizontal blanking end signal are in Extension Register R3Y[4:0].
6	Reserved
4:0	**Horizontal Sync End [4:0]:** When Sequencer Register SR1[3] = 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller Register CR5[4:0].

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CL 28785

6.7.120 R0Z: Horizontal Total Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 11.

Bit	Description	Reset State
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

The RiZ (i = 0,2,3,4,5) Extension Registers are horizontal timing shadow registers.

- These registers are used to automatically control the CRT controller on 640 x 480 and 800 x 600 LCDs, for both low-resolution and high-resolution applications.
- These registers control LCD timing independent of VGA modes.

Bit	Description
7:0	**Horizontal Total [7:0]:** When Sequencer Register SR1[3] = 1 (VCLK is divided by 2), this register performs the same function as CRT Controller Register CR0[7:0].

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6.7.121 R2Z: Horizontal Blanking Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 11.

Bit	Description	Reset State
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** When Sequencer Register SR1[3] = 1 (VCLK is divided by 2), this register performs the same function as CRT Controller Register CR2[7:0].

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6.7.122 R3Z: Horizontal Blanking End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 11.

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:5	Reserved
4:0	**Horizontal Blanking End [4:0]:** When Sequencer Registser SR1[3] = 1 (VCLK is divided by 2), these bits perform the same function as CR3[4:0]. • These bits are the least-significant five bits of a 6-bit word controlling the horizontal blanking end signal. • The most-significant sixth bit that controls the horizontal blanking end signal is in register R5Z[7].

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6.7.123 R4Z: Horizontal Sync Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 11.

Bit	Description	Reset State
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** When Sequencer Register SR1[3] = 1 (VCLK is divided by 2), this register performs the same function as CRT Controller Register CR4[7:0].

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6.7.124 R5Z: Horizontal Sync End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] = 11.

Bit	Description	Reset State
7	Horizontal Blanking End [5]	0
6	Reserved	
5	Reserved	
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

NOTE: The '?' in the above register address is 'B' in Monochrome Mode and 'D' in Color Mode.

Bit	Description
7	**Horizontal Blanking End [5]:** • This is the most-significant bit of the six-bit horizontal blanking end signal. • The least-significant five bits of the horizontal blanking end signal are in Extension Register R3Z[4:0].
6	Reserved
4:0	**Horizontal Sync End [4:0]:** When Sequencer Register SR1[3] = 1 (VCLK is divided by 2), this register performs the same function as Controller Register CR5[4:0].

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7. Electrical Specifications

7.1 Absolute Maximum Ratings

Table 7-1. Absolute Maximum Ratings

Specification	Maximum Rating
Ambient temperature while operating (T_A)	0° to 70° C
Storage temperature	-65° to 150°
Voltage on any pin	V_{SS} -0.5V to V_{DD} + 0.5V
Operating power dissipation	1.5 Watts
Power supply voltage	7.0 Volts
Injection current (latch-up testing)	100 mA

NOTES:

1) System components should be operated within the limits of the absolute maximum ratings. If system components are run at ratings at or outside these limits, the system components may be permanently damaged.
2) Functional operation at or outside any of the conditions indicated in the absolute maximum ratings is not implied.
3) Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

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7.2 DC Specifications

7.2.1 DC Specifications: Digital

In the table below, VDD = 5.0V ± 0.25V (or V_{DD} = 3.3V ± 0.3V) and T_A = 0° to 70° C, unless otherwise specified.)

Table 7–2. DC Digital Specifications

Symbol	Parameter	MIN	MAX	Conditions	Note
V_{DD} (5 V)	Power Supply Voltage (TTL)	4.75 Volts	5.25 Volts	Normal Operation	
V_{DD} (3.3V)	Power Supply Voltage (CMOS)	3.00 Volts	3.60 Volts	Normal Operation	
V_{IL}	Input Low Voltage (TTL)	0 Volts	0.8 Volts	3.0V < V_{DD} < 5.25V	
V_{IH}	Input High Voltage (TTL)	2.0 Volts	V_{DD} + 5% V_{DD} (Volts)	3.0V < V_{DD} < 5.25V	
V_{IHC}	Input High Voltage (CMOS)	0.7V_{DD} (Volts)	V_{DD} + 5% V_{DD} (Volts)	3.0V < V_{DD} < 5.25V	
V_{ILC}	Input Low Voltage (CMOS)	-0.5 Volts	0.3V_{DD} (Volts)	3.0V < V_{DD} < 5.25V	
V_{OL}	Output Low Voltage (TTL)		0.4 Volts	I_{OL} = (Refer to Table 7–6.)	1
V_{OH}	Output High Voltage (TTL)	2.4 Volts		I_{OH} = (Refer to Table 7–6.)	2
V_{OHC}	Output High Voltage (CMOS)	0.9V_{DD} (Volts)		I_{OHC} = -200 µA	
V_{OLC}	Output Low Voltage (CMOS)		0.1V_{DD} (Volts)	I_{OLC} = 3.2 mA	
I_{CC1}	Power Supply Current		150 mA	CRT-only Operation	3
I_{CC2}	Power Supply Current		100 mA	LCD-only Operation	3
I_{CC3}	Power Supply Current		1.0 mA	Hardware-Controlled Suspend mode	3
I_{IL}	Input Low Current		-10 µA	V_{IN} = 0.0V	
I_{IH}	Input High Current		10 µA	V_{IN} = V_{DD}	
I_{OZ}	Output Leakage Current	-10 µA	10 µA	0 < V_{OUT} < V_{DD}	4
C_{IN}	Input Capacitance		10 pF		5
C_{OUT}	Output Capacitance		10 pF		5

NOTES:

1) Data outputs (D[31:0]) rated at I_{OL} = 12 mA at V_{OL} = 0.4V, will sink I_{OL} = 24 mA at V_{OL} = 0.5V.

2) Data outputs (D[31:0]) rated at I_{OH} = -3.0 mA at V_{OH} = 2.4V, will source I_{OH} = -15 mA at V_{OH} = 2.0V.

3) These current values occur when V_{DD} = 3.3V, FPVDCLK = 28 MHz, and MCLK = 45 MHz.

4) This current is a measure of 3-state output leakage current when in high-impedance (high-Z) mode.

5) This capacitance is periodically sampled and tested.

7.2.2 DC Specifications: Loading Values

Table 7–3. Loading Values for 7542 Output Pins

Pin Number	Pin Name	I_{OH} (mA)	I_{OL} (mA)	Load (pF)
3	LDEV#	—	20.0	200
4	RDY#	-3.0	20.0	200
5	INTR (INTR/INTR#)	-3.0	20.0	200
22	STOP#	-3.0	8.0	200
23	PAR	-3.0	8.0	200
43:46, 48:51, 53:61, 63:66, 68:72, 74:79, 136:135, 138:137,139:140	AD / D [31:0]	-3.0	12.0	240
91	VSYNC	-12	12	50
93	HSYNC	-12	12	50
94	NTSC/PAL	-12	12	50
140:133, 131:125, 123:122, 120:114	FP[23:0]	-12	12	50
95	CSYNC	-12	12	50
144:141,134,133,125,123	FCP[7:0]	-12	12	50
101	FCBLANK#	-12	12	50
102	FPVEE	-12	12	35
103	VCLK	-12	12	240
106	FPVCC	-12	12	35
108	FPDE	-12	12	50
110	LFS[a]	-12	12	50
112	LLCLK[a]	-12	12	50
113	FPVDCLK	-12	12	50
115	OVRW# (FP[1] / OVRW#)	-12	12	35
117	MOD (FP[3] / MOD)	-3.0	3.0	20
123	SBYST#	-6.0	6.0	35
125	SUSPST#	-6.0	6.0	35
146	TVON	-12	12	50
148	PROG	-6.0	6.0	35
151 161,163 167,186:191,193,196,202:204, 206,208,1,2	MD[31:0]	-12	12	50
169 170, 195, 194	CAS#[3:0]#	-12	12	50
169 170, 195, 194	WE#[3:0]	-12	12	50
171 180	MA[9:0]	-12	12	50
181	CAS#/WE#	-12	12	50
182	OE#	-12	12	50
184 183	RAS#[1:0]#	-12	12	50

[a] The LLCLK and FPVDCLK values depend on the bit setting of Extension Register SR2B[7].
When this bit = 0, the values for these pins are: IOH = -12 mA, IOL = 12 mA, and the load is 50 pF.
When this bit = 1, the values for these pins are: IOH = -24mA, IOL = 24 mA, and the load remains 50 pF.

7.2.3 DC Specifications: Palette DAC

In the table below, VDD = 5.0V ± 0.25V (or V_{DD} = 3.3V ± 0.3V) and T_A = 0° to 70° C, unless otherwise specified.

Table 7–4. Palette DAC Specifications

Symbol	Parameter	MIN	MAX	Units	Conditions
DACVDD (5.0V)	DAC Supply Voltage	4.75	5.25	Volts	Normal Operation
DACVDD (3.3V)	DAC Supply Voltage	3.00	3.60	Volts	Normal Operation
$AI_{DD2.3}$ (5.0V)	Analog Supply Current		*tbd*	mA	$AV_{DD2.3}$ = 5.25V
$AI_{DD2.3}$ (3.3V)	Analog Supply Current		*tbd*	mA	$AV_{DD2.3}$ = 3.6V
I_{REF}[1]	DAC Reference Current	-3	-10	mA	

NOTE:

1) Refer to the detailed pin description in Chapter 2. for information regarding nominal I_{REF}.

7.2.4 DC Specifications: Frequency Synthesizer

In the table below, V_{DD} = 3.3V ± 0.3V and T_A = 0° to 70° C, unless otherwise specified.

Table 7–5. Frequency Synthesizer Specifications

Symbol	Parameter	MIN	MAX	Units	Conditions
MAV_{DD} VAV_{DD}	Synthesizer Supply Voltage	3.00	3.60	Volts	
MAI_{DD} + VAI_{DD}	Analog Supply Current		*tbd*[6]	mA	MAV_{DD} = VAV_{DD} = 3.6V

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7.3 DAC Characteristics

In the table below, V_{DD} = 3.3V ± 0.3V and T_A = 0° to 70° C, unless otherwise specified.

Table 7–6. DAC Characteristics

Symbol	Parameter	MIN	MAX	Units	Conditions	Notes
Res	Resolution		6	Bits		
I_O	Output Current		30	mA	V_O < 1V	
t_D	Analog Output Delay		*tbd*[8]	ns		Notes 1, 2, 3
t_r, t_f	Analog Output Rise/Fall Time		8	ns		Notes 2, 3, 4
t_s	Analog Output Settling Time		15	ns		Notes 2, 3, 5
t_{SK}	Analog Output Skew		*tbd*	ns		Notes 2, 3, 6
FT	Clock and Data Feed-through		*tbd*	db		Notes 2, 3, 6
DT	DAC-to-DAC Correlation		*tbd*	%		Notes 6, 7
GI	Glitch Impulse		*tbd*	pV/sec.		Notes 2, 3, 6
CT	DAC-to-DAC Crosstalk		*tbd*	db		Notes 2, 3, 4

NOTES:

1) t_D is measured from the 50% point of VCLK to 50% point of full-scale transition.
2) Load is 50 ohms and 30 pF per analog output.
3) I_{REF} = to be determined from measures taken according to the IREF application note
4) t_r and t_f are measured from 10% to 90% full-scale.
5) t_s is measured from 50% of full-scale transition to output remaining within 2% of final value.
6) Outputs loaded identically.
7) About the mid-point of the distribution of the three DACs measured at full-scale output.
8) *tbd* = to be determined.

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7.4 AC Parameters: Listing

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7.4.1 Bus Configuration: Reset Timing

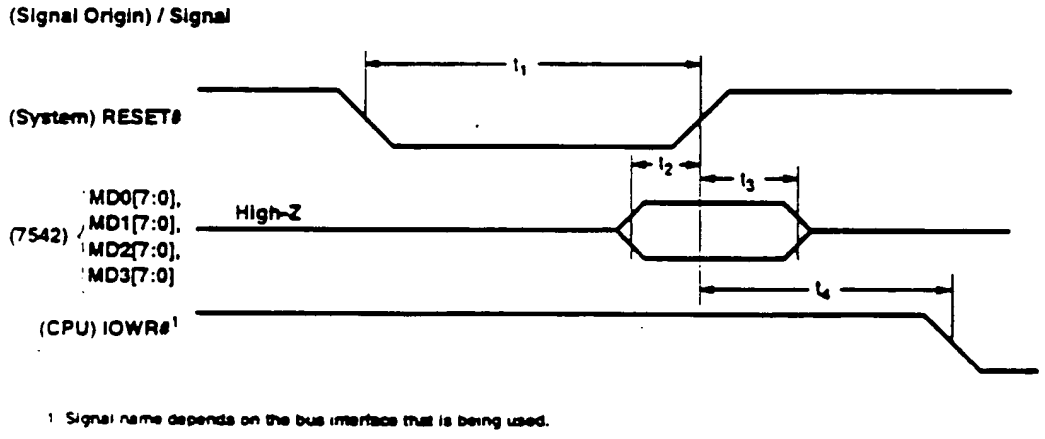
The timing diagram in this section is for the bus configuration, which takes place during setup.

Table 7–7 and Figure 7–1 refer to information from the SW0, SW1, and SW2 pins, which are read by SR24[2:0] and used by the memory data lines to configure the CL-GD7542.

Table 7–7. Bus Configuration: Reset# Timing

Symbol	Parameter	MIN	MAX
t_1	Reset Pulse Width	12t	–
t_2	Memory Data Setup time to Reset rising edge	2ns	–
t_3	Memory Data Hold time from Reset rising edge	5ns	–
t_4	Reset High to first I/O Read/Write Command	12t	–

Note: 't' is the period for MCLK, a clock that is internal to the CL-GD7542.



1 Signal name depends on the bus interface that is being used.

Figure 7–1. Bus Configuration: Reset# Timing

7.4.2 Local Bus: Timing Diagrams

The timing diagrams in this section apply to the '486 local bus and VESA local bus (the VL bus) interfaces to the CL-GD7542.

Table 7–8. Local Bus: LCLK Timing

Symbol	Parameter	CLK1X	
		MIN	MAX
t_1	Rise Time	0.5ns	4.0ns
t_2	Fall Time	0.5ns	4.0ns
t_3	Positive High Pulse Width	40% t_5	60% t_5
t_4	Negative Low Pulse Width	40% t_5	60% t_5
t_5	Period	30ns	To be determined

Note: T is the period for MCLK, a clock that is internal to the CL-GD7542.

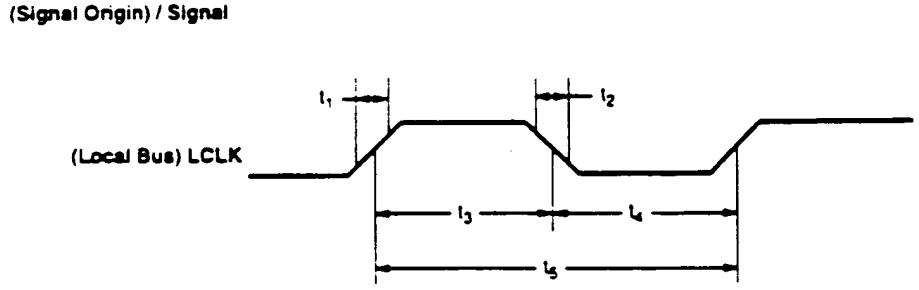


Figure 7–2. Local Bus: LCLK Timing

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Table 7–9. Local Bus: ADS# and LDEV# Timing

Symbol	Parameter	MIN	MAX
t_1	Address, Status, ADS# Setup to LCLK	5ns	–
t_2	LDEV# Low Delay from Address, Status (20-pF loading)	–	15ns
t_3	LDEV# High Delay from Address, Status	–	18ns

Note: Ŧ is the period for MCLK, a clock that is internal to the CL-GD7542.

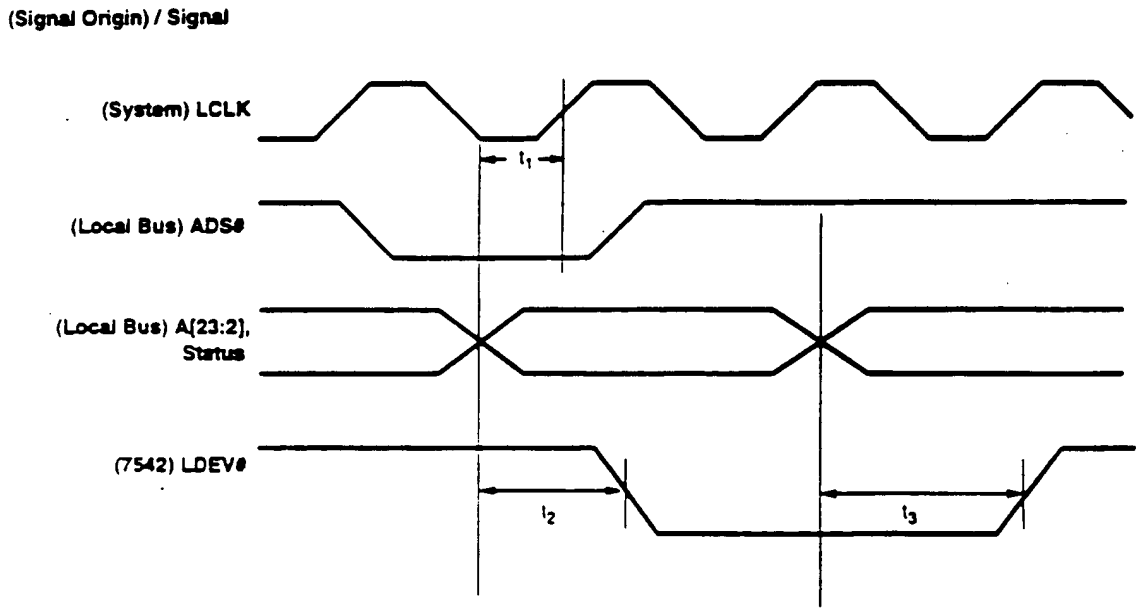


Figure 7–3. Local Bus: ADS# and LDEV# Timing

Table 7–10. Local Bus: RDY# and Read-Data Timing

Symbol	Parameter	MIN	MAX
t_1	RDY# Low Delay from LCLK	0	12ns
t_2	RDY# High Delay from LCLK	0	12ns
t_3	RDY# High Pulse Width before High-Z	1/2 LCLK	–
t_4	Read Data Setup to RDY# Low	0ns	–
t_5	Read Data Hold from RDYRTN# High	12ns	To be determined

Note: τ is the period for MCLK, a clock that is internal to the CL-GD7542.

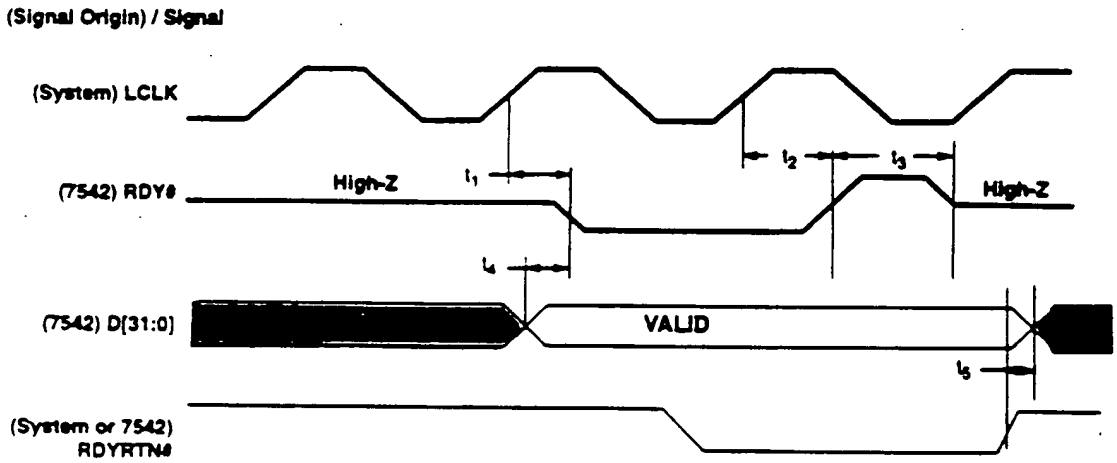


Figure 7–4. Local Bus: RDY# and Read-Data Timing

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Table 7–11. Local Bus: RDYRTN# Timing

Symbol	Parameter	MIN	MAX
t_1	RDYRTN# Setup time to LCLK	5ns	-
t_2	RDYRTN# Hold time from LCLK	2ns	-

Note: T is the period for MCLK, a clock that is internal to the CL-GD7542.

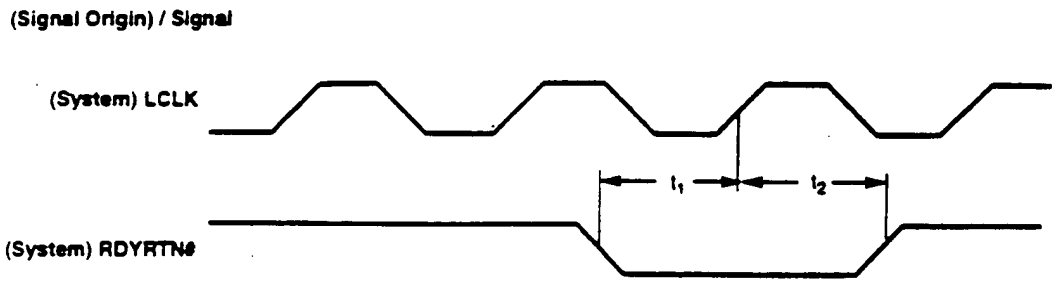


Figure 7–5. Local Bus: RDYRTN# Timing

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Table 7–12. Local Bus: Write Data Timing

Symbol	Parameter	MIN	MAX
t_1	Data Setup time to LCLK	7ns	
t_2	Data Hold time from LCLK	2ns	

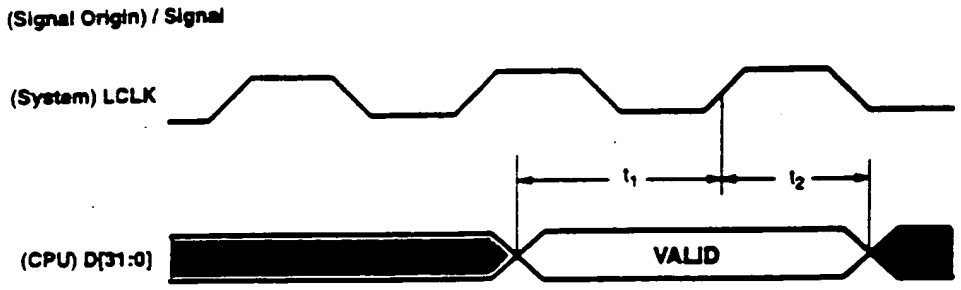


Figure 7–6. Local Bus: Write Data Timing

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7.4.3 PCI Bus: Timing Diagrams

The timing diagrams in this section apply to a PCI bus interface to the CL-GD7542.

Table 7–13. PCI Bus: FRAME#, DEVSEL#, AD[31:0], and C/BE#[3:0] Timing (Write)

Symbol	Parameter	MIN	MAX
t_1	FRAME# Setup to CLK	7 ns	–
t_2	AD[31:0] (Address) Setup to CLK	7 ns	–
t_3	AD[31:0] (Address) Hold from CLK	0 ns	–
t_4	AD[31:0] (Data) Setup to CLK (Write)	7 ns	–
t_5	AD[31:0] (Data) Hold from CLK (Write)	0 ns	–
t_6	C/BE#[3:0] (Bus CMD) Setup to CLK	7 ns	–
t_7	C/BE#[31:0] (Bus CMD) Hold from CLK	0 ns	–
t_8	C/BE#[3:0] (Byte Enable) Setup to CLK	7 ns	–
t_9	DEVSEL# Delay from CLK	0 ns	11
t_{10}	DEVSEL# High before HI-Z	1 CLK	–

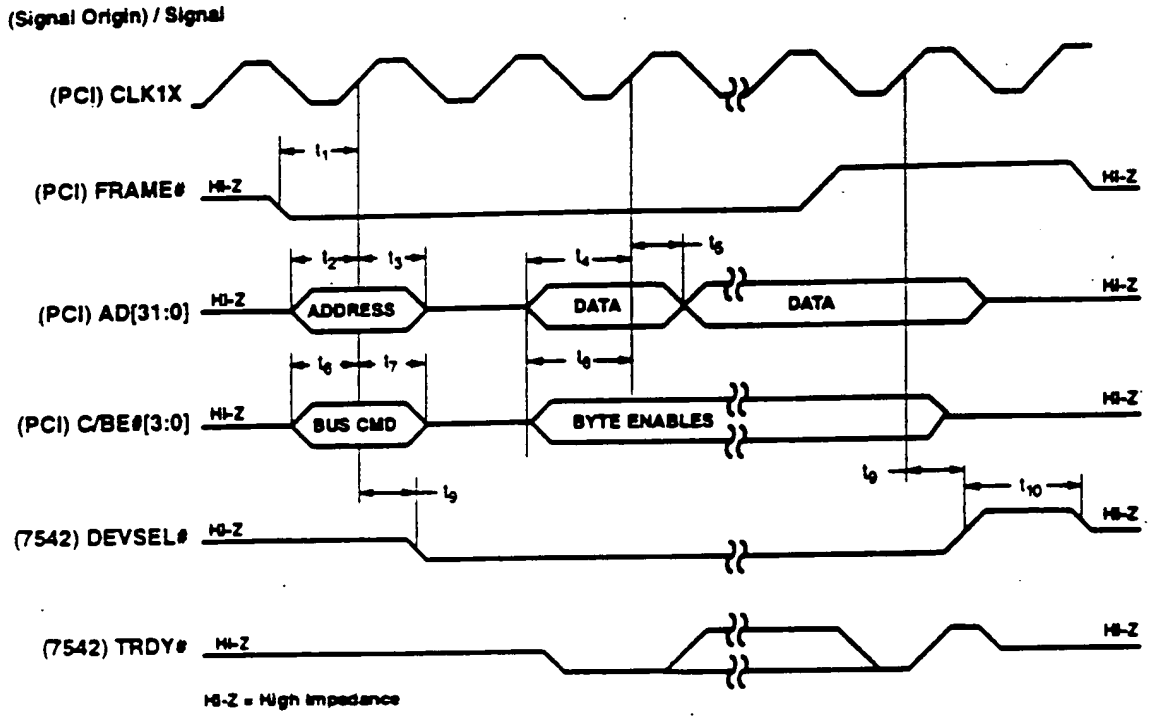


Figure 7-7. PCI Bus: FRAME#, DEVSEL#, AD[31:0], and C/BE#[3:0] Timing (Write)

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Table 7-14. PCI Bus: FRAME#, DEVSEL#, AD[31:0], and C/BE#[3:0] Timing (Read)

Symbol	Parameter	MIN	MAX
t_1	FRAME# Setup to CLK	7ns	-
t_2	AD[31:0] (Address) Setup to CLK	7ns	-
t_3	AD[31:0] (Address) Hold from CLK	0ns	-
t_4	AD[31:0], C/BE#[3:0] HI-Z from CLK (Read)	0ns	28ns
t_5	C/BE#[3:0] (Bus CMD) Setup to CLK	7ns	-
t_6	C/BE#[31:0] (Bus CMD) Hold from CLK	0ns	-
t_7	C/BE#[3:0] (Byte Enable) Setup to CLK	7ns	-
t_8	DEVSEL# Delay from CLK	0ns	11
t_9	DEVSEL# High before HI-Z	1 CLK	-
t_{10}	Data Delay from CLK (Read)	2ns	11ns
t_{11}	Data Hold from CLK (Read)	0ns	To be determined

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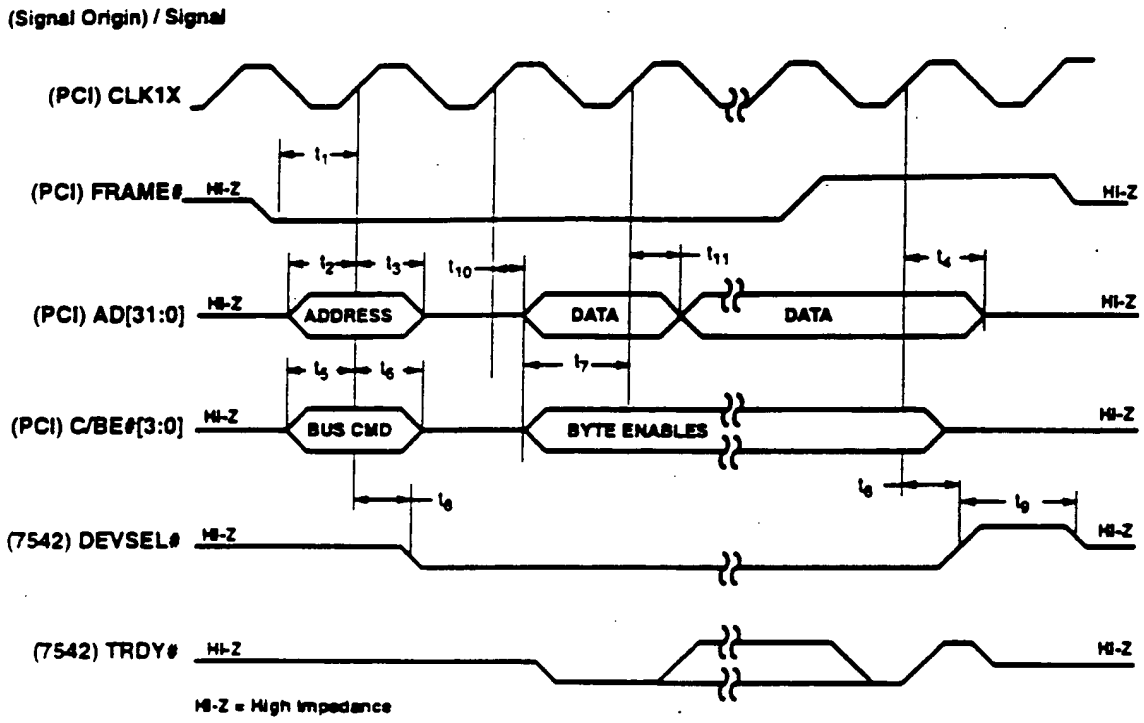


Figure 7–8. PCI Bus: FRAME#, DEVSEL#, AD[31:0], and C/BE#[3:0] Timing (Read)

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Table 7–15. PCI Bus: TRDY# Delay Timing

Symbol	Parameter	MIN	MAX
t_1	TRDY# Low Delay from CLK	0ns	15ns
t_2	TRDY# High Delay from CLK	0ns	15ns
t_3	TRDY# High pulse before HI-Z	1 CLK	–

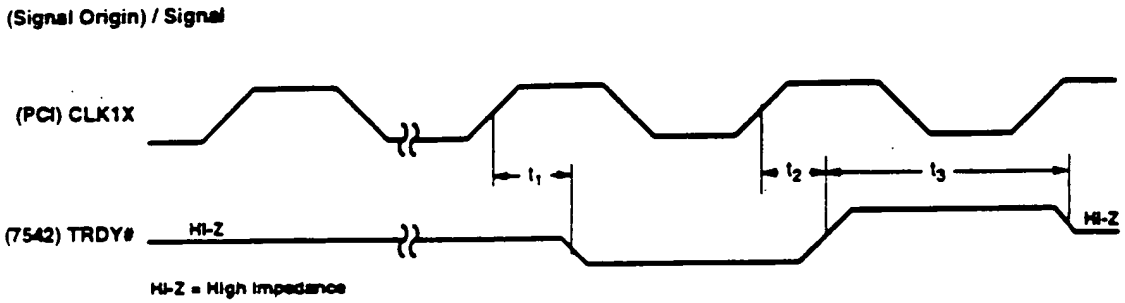


Figure 7–9. PCI Bus: TRDY# Delay Timing

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Table 7–16. PCI Bus: Read Data / IRDY# Timing

Symbol	Parameter	MIN	MAX
t_1	IRDY# Setup to CLK	7ns	–
t_2	IRDY# Hold from CLK	0ns	–

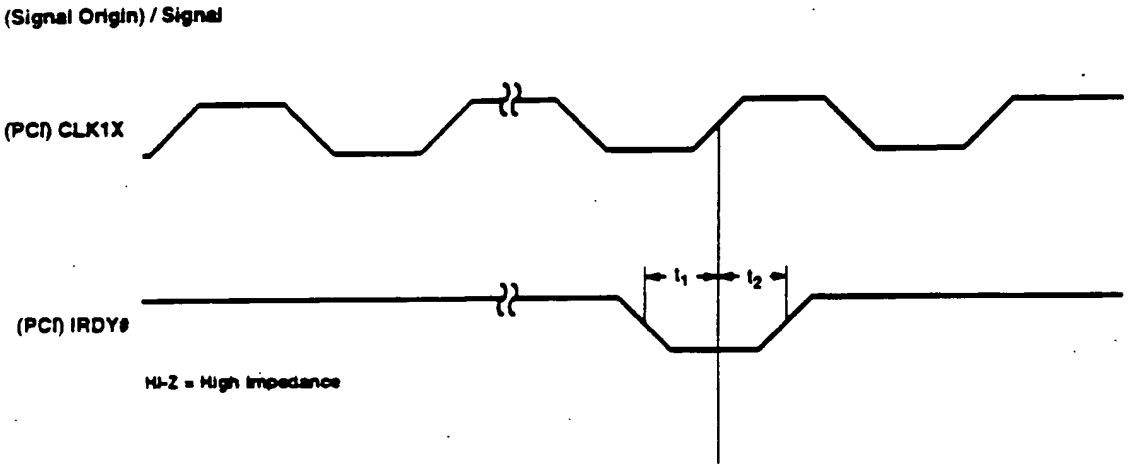


Figure 7–10. PCI Bus: Read Data / IRDY# Timing

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Table 7–17. PCI Bus: STOP# Delay Timing

Symbol	Parameter	MIN	MAX
t_1	STOP# Low Delay from CLK	2ns	11ns
t_2	STOP# High Delay from CLK	2ns	11ns
t_3	STOP# High pulse before HI-Z	1 CLK	–

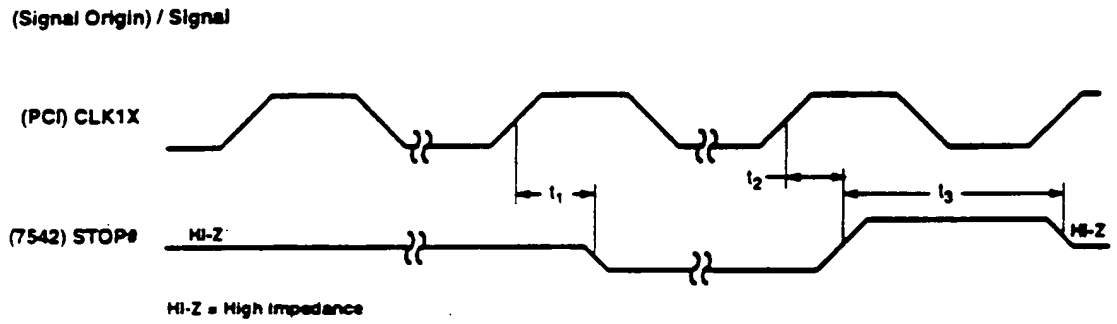


Figure 7–11. PCI Bus: STOP# Delay Timing

Table 7–18. PCI Bus: IDSEL Timing

Symbol	Parameter	MIN	MAX
t_1	IDSEL Setup to CLK	7ns	–
t_2	IDSEL Hold	0ns	–

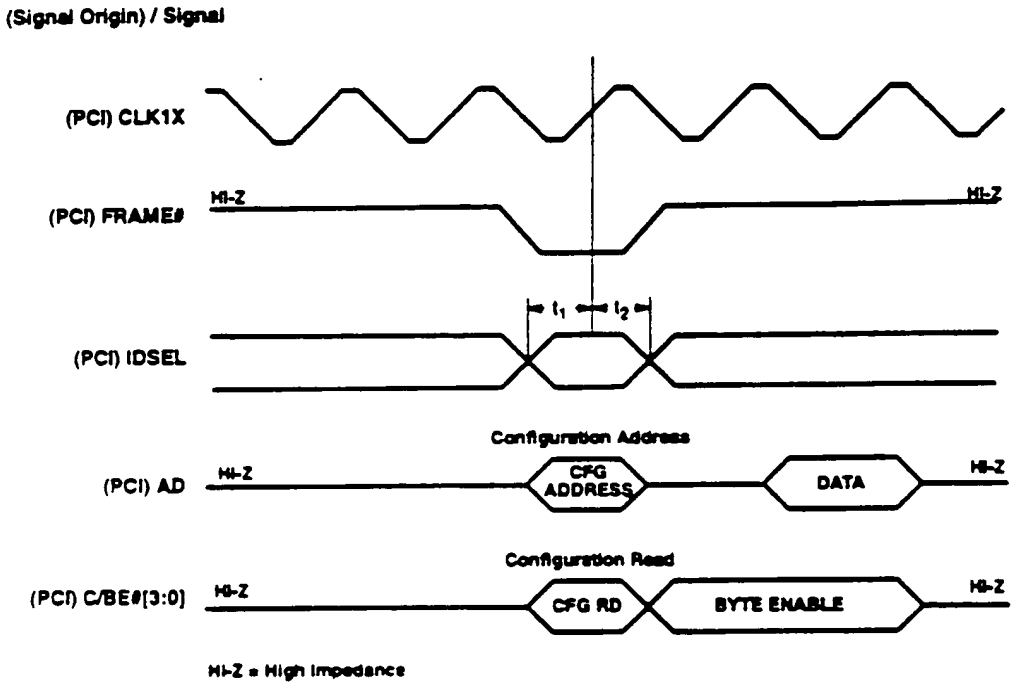


Figure 7–12. PCI Bus: IDSEL Timing

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Table 7–19. PCI Bus: PAR Timing (Write)

Symbol	Parameter	MIN	MAX
t_1	Address PAR Setup from CLK (Input to CL-GD7542)	7ns	–
t_2	Address PAR Hold from CLK (Input to CL-GD7542)	0ns	–
t_3	Data PAR Setup from CLK (Input to CL-GD7542)	7ns	–
t_4	Data PAR Hold from CLK (Input to CL-GD7542)	0ns	–

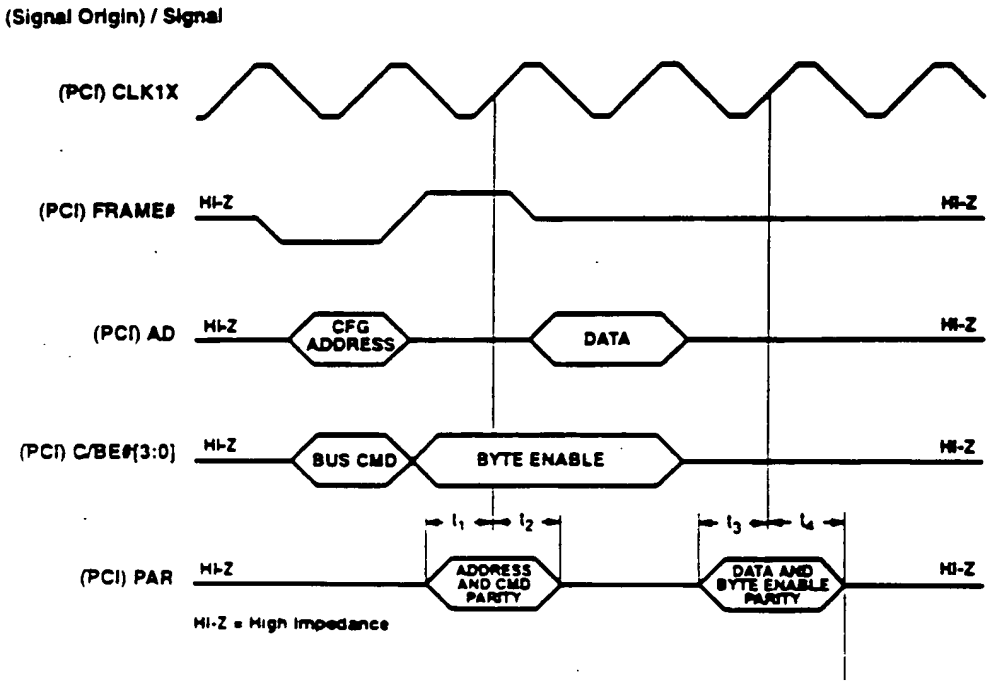


Figure 7–13. PCI Bus: PAR Timing (Write)

Table 7–20. PCI Bus: PAR Timing (Read)

Symbol	Parameter	MIN	MAX
t_1	PAR Setup from CLK (Input to CL-GD7542)	7ns	–
t_2	PAR Hold from CLK (Input to CL-GD7542)	0ns	–
t_3	PAR Delay from CLK (Output to CL-GD7542)	2ns	11ns
t_4	PAR Off Delay from CLK (Output to CL-GD7542)	–	28ns

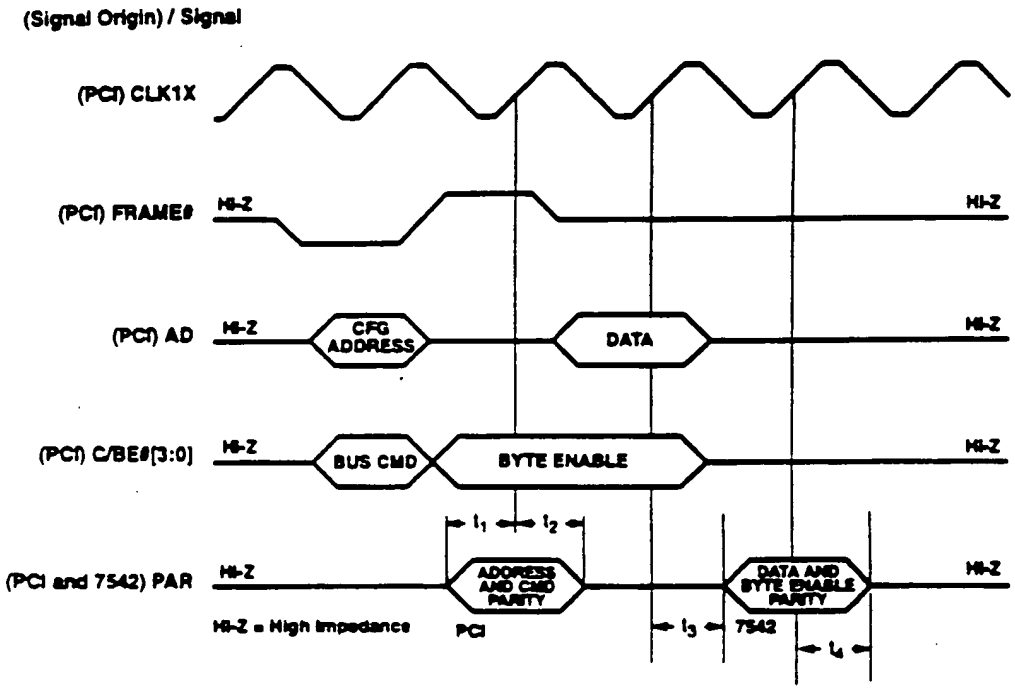


Figure 7–14. PCI Bus: PAR Timing (Read)

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7.4.4 Display Memory Bus: Timing Diagrams

The timing diagrams in this section apply to the CL-GD7542 bus interface to the display memory.

Table 7–21. Display Memory Bus: Read Timing (t^a = MCLK)

Symbol	Parameter	MIN	MAX
t_1	Address Setup to RAS# Low	1.5t- 9ns	–
t_2	Address Setup to CAS# Low	1.0t - 3ns	–
t_3	RAS# Low to CAS# Low Delay (Standard RAS#)	2.5t - 7.5ns	
t_3	RAS# Low to CAS# Low Delay (Extended RAS#)	3.0t	
t_4	Row Address Hold from RAS# Low	1.5t - 5ns	–
t_5	Column Address Hold from CAS# Low	1.0t	–
t_6	Data Valid from RAS# Low (Standard RAS#)	–	4.0t -1ns
t_6	Data Valid from RAS# Low (Extended RAS#)	–	4.5t -1ns
t_7	Data Valid from CAS# Low	–	1.0t + 3ns
t_8	Data Valid from Column Address Valid	–	2t
t_9	RAS# Precharge (RAS# Pulse Width High) (Std. RAS#)	2.5t + 4.5ns	–
t_9	RAS# Precharge (RAS# Pulse Width High) (Ext. RAS#)	3.0t - 1.5ns	–
t_{10}	Read Cycle Time (Standard RAS#)	6.0t	–
t_{10}	Read Cycle Time (Extended RAS#)	7.0t	–
t_{11}	Read Command Hold from CAS# High	0.5t - 7.5ns	0.5t - 5ns
t_{12}	CAS# Precharge (CAS# Pulse Width High)	1.0t - 6ns	1.0t - 3ns
t_{13}	RAS# Pulse Width Low (Standard RAS#)	3.5t - 8.5ns	–
	RAS# Pulse Width Low (Page-Mode)	–	32µs
t_{14}	CAS# Pulse Width Low	1.0t + 3ns	32µs
t_{15}	Read Data Hold from CAS# High	10ns	–
t_{22}	CAS# Cycle Time	2.0t	–
t_{23}	Read Data Hold from OE# High	10ns	–

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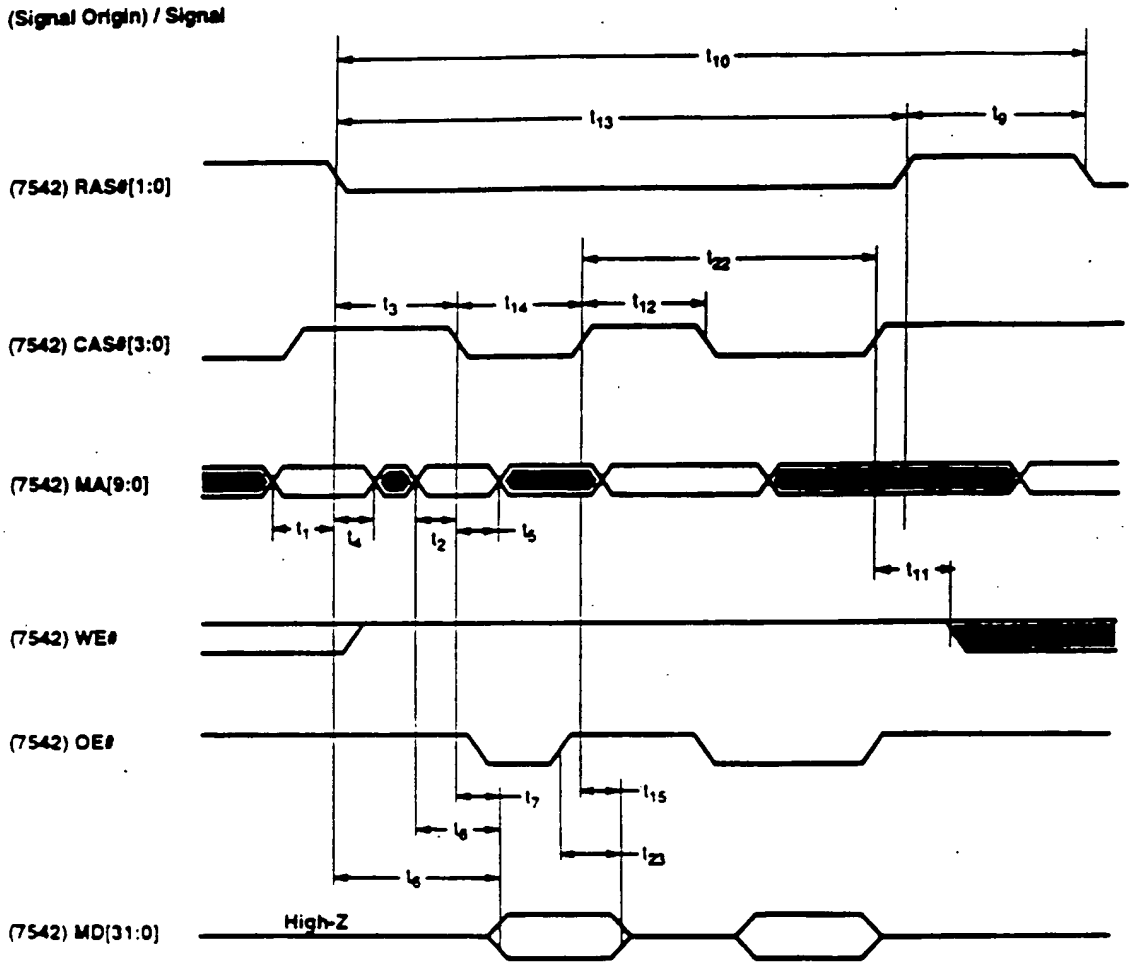


Figure 7–15. Display Memory Bus: Read Timing

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Table 7-22. Display Memory Bus: Write Timing (t^b = MCLK)[a]

Symbol	Parameter	MIN	MAX
t_1	Address Setup to RAS# Low	1.5t - 9ns	–
t_2	Address Setup to CAS# Low	1.5t - 3ns	–
t_3	RAS# Low to CAS# Low Delay (Standard RAS)	2.5t - 7.5ns	–
t_3	RAS# Low to CAS# Low Delay (Extended RAS)	3.0t	–
t_4	Row Address Hold from RAS# Low	1.5t - 5ns	–
t_5	Column Address Hold from CAS# Low	1t	–
t_6	RAS# Precharge (RAS# Pulse Width High) (Std. RAS)	2.5t + 4.5ns	–
t_6	RAS# Precharge (RAS# Pulse Width High) (Ext. RAS)	3.0t - 1.5ns	–
t_7	Write Cycle Time (Standard RAS#)	6.0t	–
t_7	Write Cycle Time (Extended RAS#)	7.0t	–
t_8	CAS# Precharge (CAS# Pulse Width High)	1.0t - 6ns	–
t_{11}	CAS# Cycle Time	2.0t	–
t_{12}	CAS# Pulse Width Low	1.0t + 3ns	32µs
t_{13}	RAS# Pulse Width Low (Standard RAS#)	3.5t - 8.5ns	
	RAS# Pulse Width Low (Page Mode)		32µs
t_{14}	WE# Low Setup to CAS# Low	1.0t - 0.5ns	–
t_{15}	WE# Low Hold to CAS# Low	1.5t - 2ns	–
t_{16}	WE# Low Pulse Width	2.5t - 2ns	–
t_{17}	Write Data Setup to CAS# Low	1.0t + 0.5ns	–
t_{18}	Write Data Hold from CAS# Low	1.0t - 8ns	–

a. The memory interface specifications are valid from 0° to 70° C at operating voltages of 3.3 volts ± 0.3 volts and 5 volts ± 0.5 volts.

b. t = MCLK period an internal clock.

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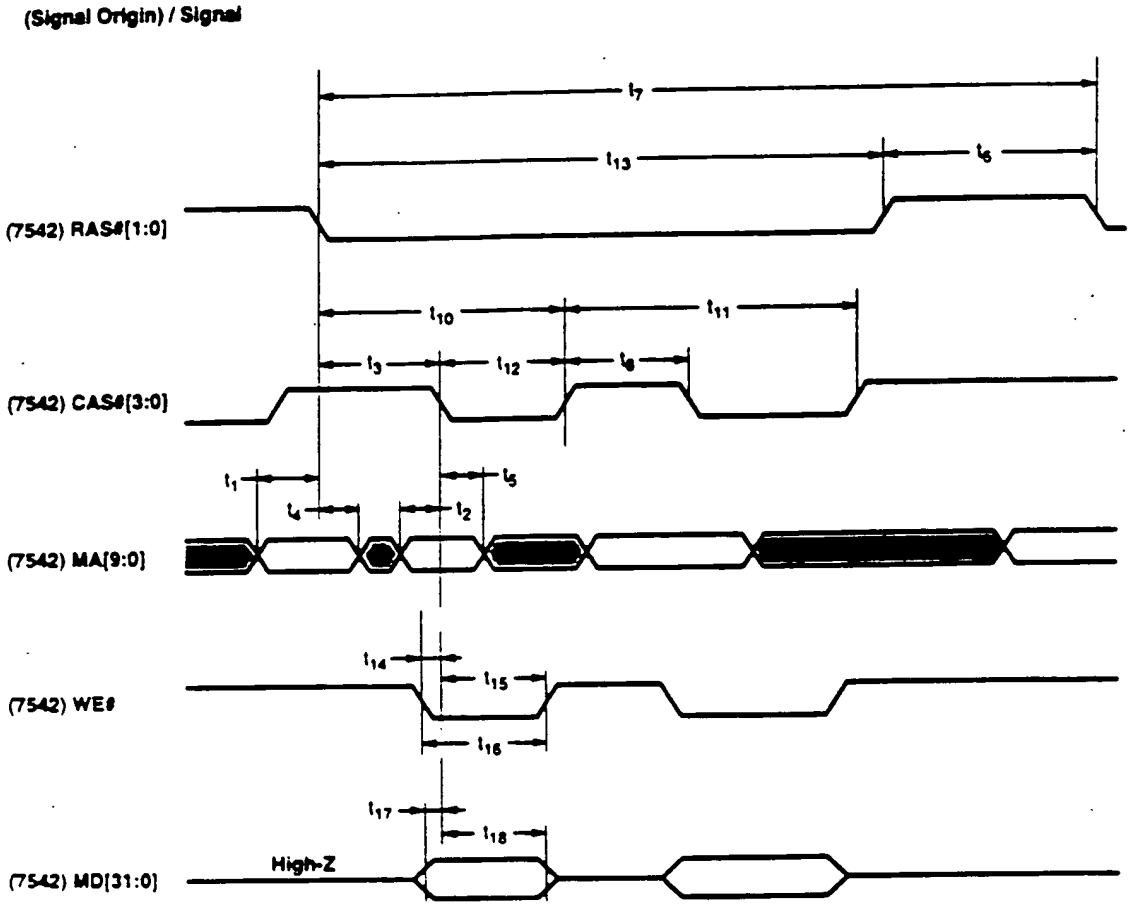


Figure 7–16. Display Memory Bus: Write Timing

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Table 7-23. Display Memory Bus: CAS#-Before-RAS# Refresh Timing[a]

Symbol	Parameter	MIN	MAX	Units
t_1	CAS# Low Setup time to RAS# Active1	1	–	t^b
t_2	RAS# Low Pulse Width	4	–	t^b
t_3	RAS# High Pulse Width	3	–	t^b
t_4	CAS# Hold time for Refresh	1.5	–	t^b
t_5	Refresh Cycle Period	7	–	t^b
t_6	CAS# Pulse Width High (Precharge time)	2	–	t^b
t_7	RAS# High to CAS# Low (Precharge time)	1	–	t^b

a. There will be either three or five RAS# pulses while CAS# remains Low.
b. 't' is the MCLK period, an internal clock.

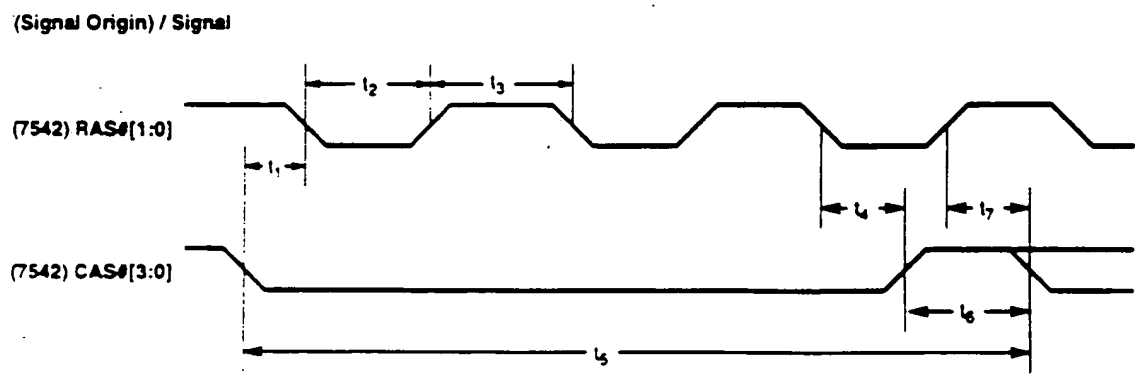


Figure 7-17. Display Memory Bus: CAS#-Before-RAS# Refresh Timing

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7.4.5 Feature Connector: Timing Diagrams

The timing diagrams in this section apply to the CL-GD7542 interface to the Feature Connector (FC).

Table 7–24. Feature Connector: Timing with Clock and Data Driven Externally

Symbol	Parameter	MIN	MAX
t_1	FCP[7:0] Setup to FCVCLK	6ns	–
t_2	FCP[7:0] Hold from FCVCLK	6ns	–

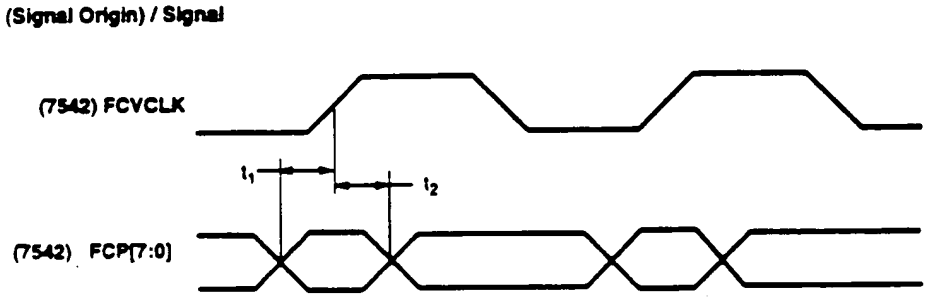


Figure 7–18. Feature Connector: Timing with Clock and Data Driven Externally

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Table 7–25. Feature Connector: FCVCLK Input Timing Requirements

Symbol	Parameter	MIN	MAX
t_1	Rise Time (FCVCLK)	–	3ns
t_2	Fall Time (FCVCLK)	–	3ns
t_3	High Period (FCVCLK)	40% of t_5	60% of t_5
t_4	Low Period (FCVCLK)	40% of t_5	60% of t_5
t_5	Period (FCVCLK)	26ns	–

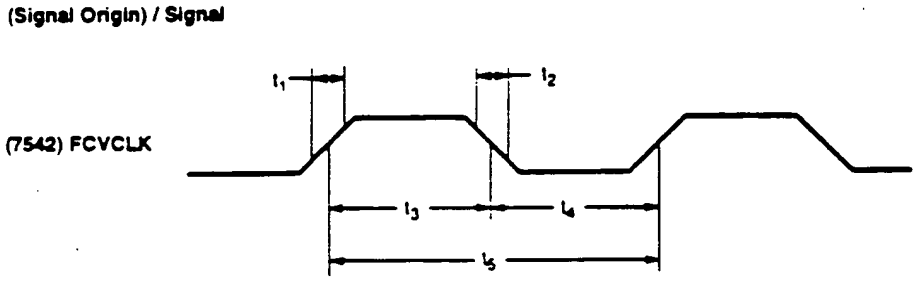


Figure 7–19. Feature Connector: FCVCLK Input Timing Requirements

7.4.6 LCD Interface: Timing Diagrams

The timing diagrams in this section apply to the CL-GD7542 interface to LCD flat panels.

Table 7–26. LCD Interface: Timing for STN Monochrome and Color-Passive LCD[a]

Symbol	Parameter	M2DD-8	M2SS-8	C8DD-16	C8DD-8	C8SS-16	M2DD-16	C8SS-di-8
		Mono.	Mono.	Color	Color	Color	Mono. Hi-Res.	Color
t_1	FPVDCLK period	4t	8t	2.5t	t	5t	8t	5t
t_2	FPVDCLK high time	2t - 6ns	4t - 6ns	t - 6ns	0.5t - 6ns	2t - 6ns	4t - 6ns	t - 6ns
t_3	FPVDCLK low time	2t - 6ns	4t - 6ns	t - 6ns	0.5t - 6ns	2t - 6ns	4t - 6ns	4t - 6ns
t_4	FPVDCLK rise and fall time (maximum)	6ns	6ns	6ns	6ns	6ns	6ns	6ns
t_5	Data setup time	2t - 10ns	4t - 10ns	t - 6ns	0.5t - 6ns	2t - 10ns	4t - 10ns	t - 10ns
t_6	Data hold time	2t - 10ns	4t - 10ns	t - 6ns	0.5t - 6ns	2t - 10ns	4t - 10ns	t - 10ns
t_7	FPVDCLK low to LLCLK low	4t - 10ns	8t -10ns	t - 6ns	2t - 10ns	4t - 10ns	8t -10ns	2t - 10ns
t_8	FPVDCLK low from LLCLK low	4t - 10ns	8t - 10ns	t - 6ns	2t - 10ns	4t - 10ns	8t - 10ns	2t - 10ns
t_9	LLCLK high time	3t - 6ns	t - 6ns	3t - 6ns	3t - 6ns	3t - 6ns	t - 6ns	3t - 6ns
t_{10}	LFS high setup to LLCLK low (typical)	2t	t	2t	2t	2t	t	2t
t_{11}	LFS high hold time to LLCLK low (typical)	2t	2t	2t	2t	2t	2t	2t
t_{12}	MOD delay from FPVDCLK high (maximum)	300ns	300ns	300ns	300ns	300ns	300ns	300ns

a Values are MINIMUM unless otherwise specified.

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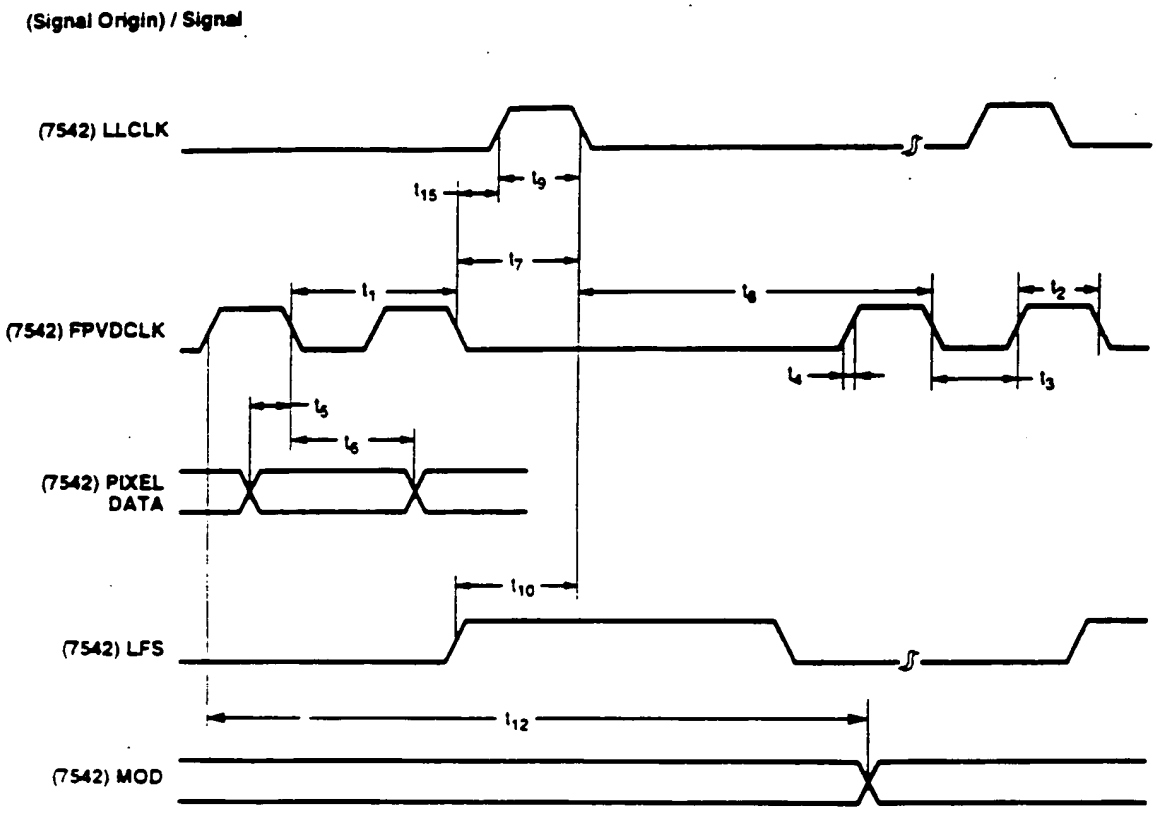
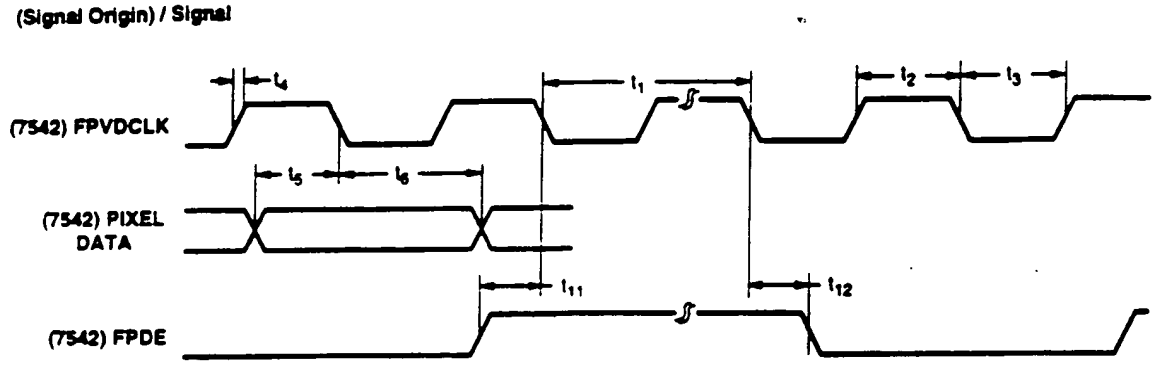


Figure 7-20. LCD Interface: Timing for STN Monochrome and Color-Passive LCD

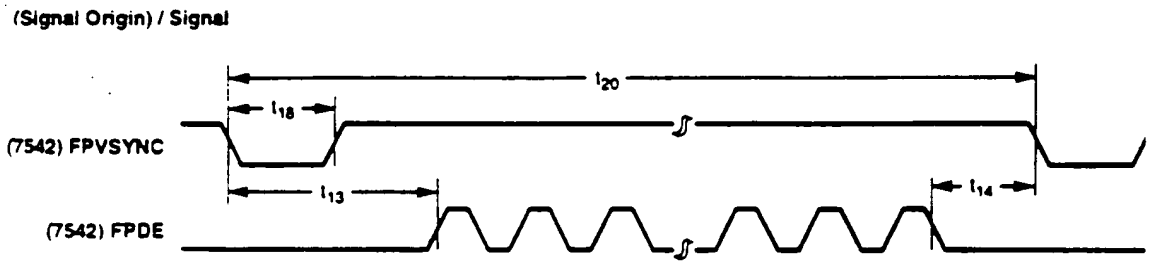
Table 7–27. LCD Interface: Timing for TFT Color LCD

Symbol	Parameter	TFT: C512SS / C4KSS / C256KSS / C16MSS / C64SSI	
		Minimum	Maximum
t_1	FPVDCLK period	t_1	
t_2	FPVDCLK high pulse width	.5t - 6ns	
t_3	FPVDCLK low pulse width	.5t - 6ns	
t_4	FPVDCLK rise and fall time		10ns
t_5	Data setup time	.5t - 6ns	
t_6	Data hold time	.5t - 6ns	
t_7	FPHSYNC setup to FPVDCLK	.25t	
t_8	FPHSYNC hold to FPVDCLK	.25t	
t_9	FPVSYNC setup to FPHSYNC	$1.5t_1$	
t_{10}	FPVSYNC hold to FPHSYNC	$1t_1$	
t_{11}	FPDE setup to FPVDCLK	.25t	
t_{12}	FPDE hold to FPVDCLK	.25t	
t_{13}	Vertical front porch	0 lines	30 lines
t_{14}	Vertical back porch	1 line	31 lines
t_{15}	Horizontal front porch	0ns	$96t_1$
t_{16}	Horizontal back porch	$32t_1$	$128t_1$
t_{17}	FPHSYNC width	$32t_1$	$128t_1$
t_{18}	FPVSYNC width	2 lines	2 lines

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TFT Line Timing



TFT Frame Timing

Figure 7–21. LCD Interface: Timing for Single-Scan TFT Color LCD

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7.4.7 Frequency Synthesizer: Input Timing Diagrams

The timing diagram in this section applies to the inputs to the frequency synthesizer.

Table 7-28. Frequency Synthesizer: Input Timing

Symbol	Parameter	3.3V		5.0V	
		MIN	MAX	MIN	MAX
t_1	Input Clock Rise Time	1 ns	7 ns	1 ns	7 ns
t_2	Input Clock Fall Time	1 ns	7 ns	1 ns	7 ns
t_3	Input Clock Low Period	$t_{CLKP}/2$ - 10% t_5	t_{CLKP} + 10% t_5	t_{CLKP} - 10% t_5	t_{CLKP} + 10% t_5
t_4	Input Clock High Period	$t_{CLKP}/2$ - 10% t_5	t_{CLKP} + 10% t_5	t_{CLKP} - 10% t_5	t_{CLKP} + 10% t_5
t_5	Input Clock Frequency/Period	69.84 ns - 0.1%	69.84 ns + 0.1%	69.84 ns - 0.1%	69.84 ns + 0.1%
V_{IH}	Input High Voltage	2.0 volts	Vcc	2.0 volts	Vcc
V_{IL}	Input Low Voltage	GND	0.5 volts	GND	0.8 volts

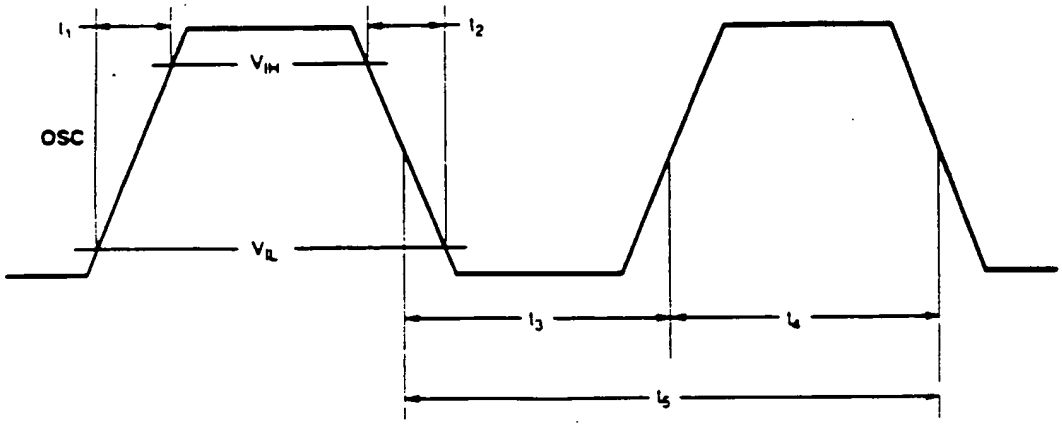


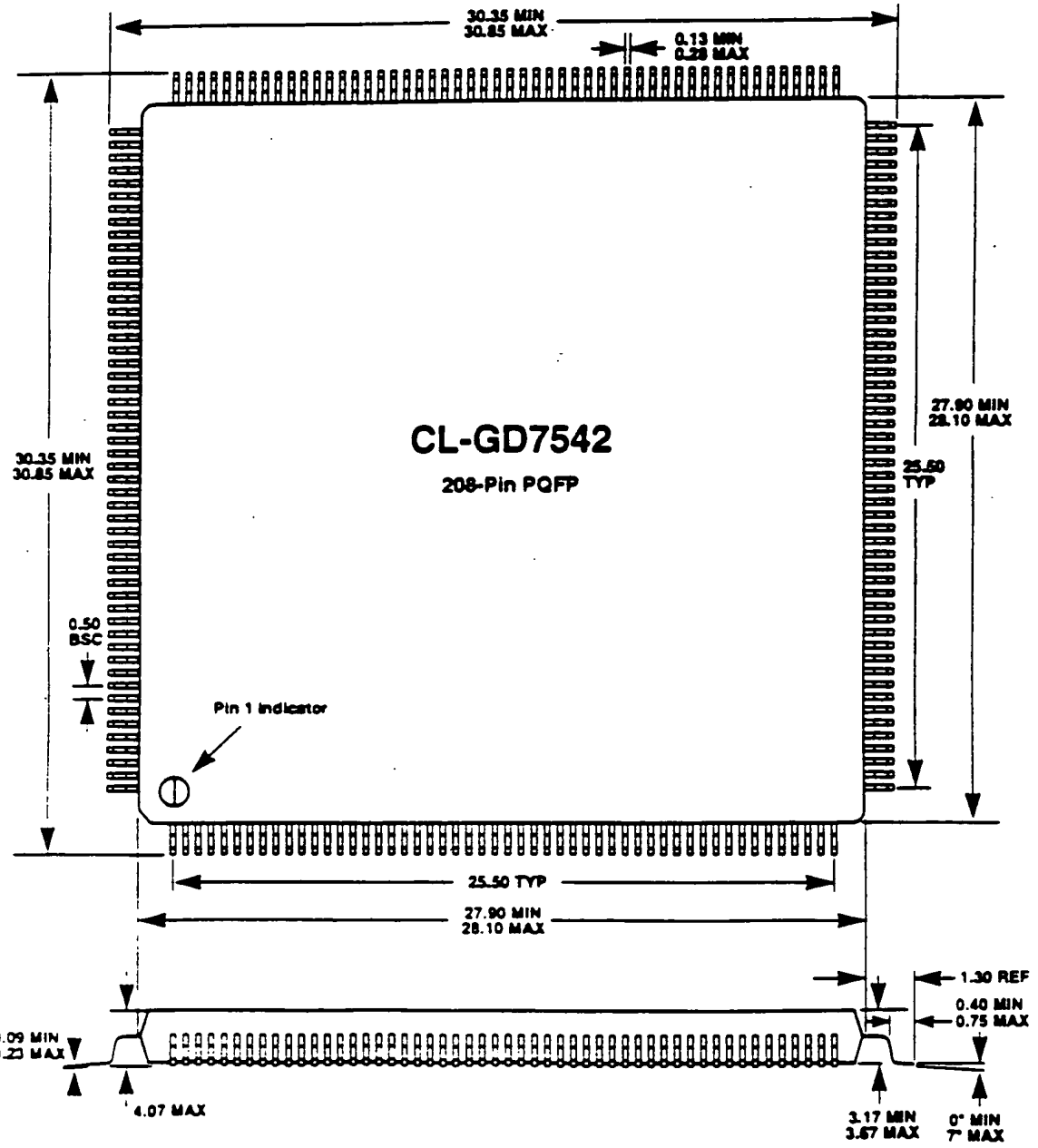
Figure 7-22. Frequency Synthesizer: Input Timing

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8. Package Dimensions



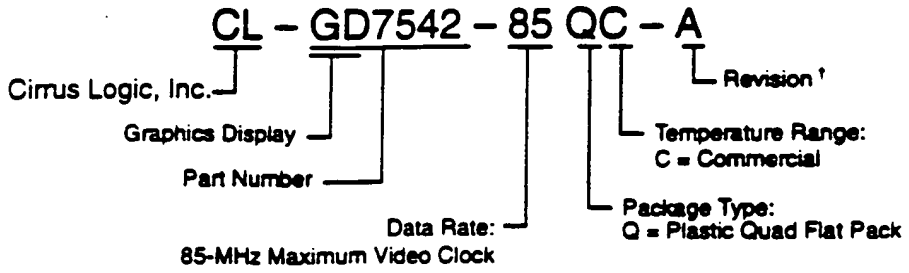
NOTES: 1) All units are in millimeters unless otherwise noted.
2) BSC = Basic dimension.

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9. Ordering Information

9.1 Package Marking Numbering Guide



† Contact Cirrus Logic, Inc. for up-to-date information on revisions.

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Appendix A1

BitBLT Engine

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A1. BitBLT Engine

A1.1 Introduction

BitBLT (Bit Block Transfer) is an operation in which one area (source area) of display memory or system memory is copied to another area (destination area) of display memory or system memory.

The CL-GD7542's BitBLT engine can not only move bytes from the source area to the destination area but also perform 16 logical raster operations to combine the source bytes with the destination bytes. In addition, it can expand a monochrome image into a color image and replicate a single 8-pixel-by-8-pixel pattern to fill a large area. These operations are done with minimum CPU intervention.

A1.2 Definitions

Source Area:

The source area of a BitBLT is the area from which the data are copied. The source area has the following characteristics:

- located either in display memory or system memory depending on its address.
- may be a monochrome image which is expanded into a color image.
- may be a single 8-pixel-by-8-pixel pattern that is replicated to fill a larger area.

The source area is never written into except in special cases where the source area and the destination area overlap in display memory.

Destination Area:

The destination area of a BitBLT is the area into which the data are written. The destination area may be in display or system memory.

Width:

The width of a BitBLT refers to the number of bytes (not pixels) of destination that are processed before adding the pitch values to the address values. Refer to Figure A1-1.

- When the destination area is on the active display screen (that is, when it is a rasterized area that is displayed), the width is the number of bytes (not necessarily pixels) in each scanline.
- When the destination area is off-screen (or in system memory) and the source is a rasterized area and there is no pattern copy or color expansion, the width is the number of bytes per scanline of the source.
- When neither the destination nor source is a rasterized area, width is simply the number of bytes that are processed before the pitch values are added to the address values, and has no special meaning.

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Width is specified in the register pair GR20/GR21. The number written into this register pair is one less than the actual desired width. This value is 11 bits, allowing a maximum width of 2048 bytes.

Height:

The height of a BitBLT refers to the number of times the pitch values are added to the address values. Refer to Figure A1-1.

- When the destination area, source area, or both are on the screen, (that is, when either is a rasterized area that is displayed), the height is the number of scanlines in that area.
- When both areas are off-screen, height is simply the number of times the pitch values are added to the address values, and it has no special meaning. In this case, width and height are simply two numbers that are multiplied together to define the number of bytes in the destination.

Height is specified in the register pair GR22/GR23. This value is 10 bits, allowing a maximum height of 1024 scanlines. The number written into the register pair is one less than the actual desired height. The contents of the registers containing the height are not modified during the operation.

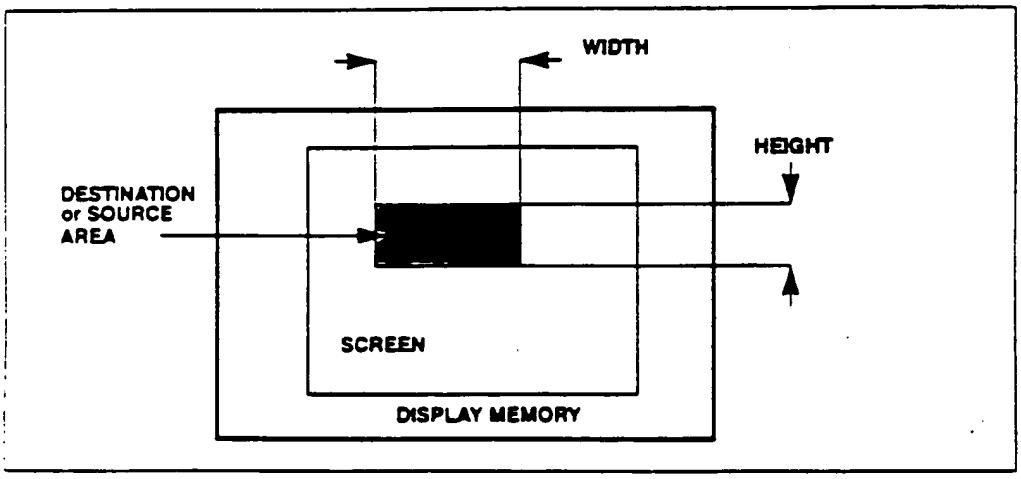


Figure A1–1. Width and Height

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Pitch:

The destination pitch and source pitch are the values that are added to the respective addresses after the bytes of each scanline in a destination area have been processed. For the case of a rasterized image, refer to Figure A1-2. The destination pitch and the source pitch are specified separately.

- When an area is a rasterized image, the respective pitch is the number of bytes between vertically adjacent pixels. This number is the number of bytes between the (first) pixels of scanline 'n' and scanline 'n+1', that is, the number that is added to the address to get from one scanline to the next.
- When an area is off-screen display memory, the scanlines are often stored in contiguous locations, which minimizes fragmentation. In this case, the respective pitch would be set equal to (width +1).
- When an area is in system memory, the respective pitch is unused and is a 'don't care'.

When executing BLTs with pattern copy or color expansion, the source area is assumed to be linear, and the source pitch is a 'don't care'.

- The source pitch is specified in register pair GR26/GR27.
- The destination pitch is specified in register pair GR24/GR25.

For the CL-GD7542, both register pairs are 12-bit values, allowing a pitch of 4095 bytes.

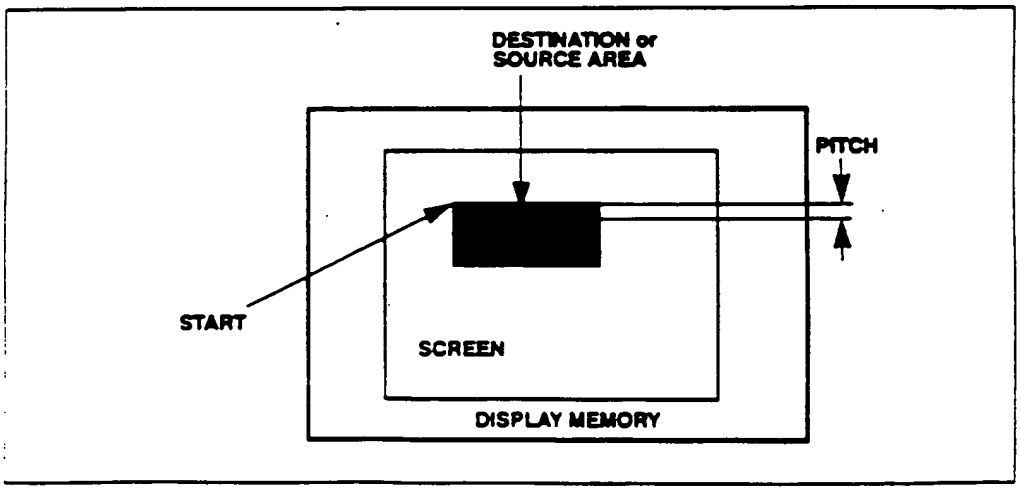


Figure A1–2. Pitch and Start

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Start:

Start refers to the address of the first byte of a destination or source area, which is a byte offset from the beginning of display memory. Refer to Figure A1-2.

- The destination area start address is specified in register triplet GR28 / GR29 / GR2A.
- The source area start address is specified in register triplet GR2C/GR2D/GR2E.

Each start address is a 21-bit value, allowing up to 2 Mbytes of display memory. The destination-start address is shown in Figure A1-2.

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A1.3 Example of Display-Memory-To-Display-Memory BitBLT

Table A1-1 shows how the BLT registers must be programmed for a very simple BLT operation of copying a 128-byte x 64-scanline area into display memory. In this example, the CL-GD7542 is assumed to be programmed in video mode 65 (800 x 600, 16-bits per pixel). Therefore, each 128-byte scanline represents 64 pixels. The source area of this operation begins at location 0. The destination area begins at location 160200 (100 scanlines from the top of the screen, 100 pixels from the left edge).

Table A1–1. Register Programming for Source Copy BitBLT Operation

Register(s)	Contents	Field	How Calculated
GR0 / GR10	Don't care	Background color	-
GR1 / GR11	Don't care	Foreground color	-
GR20 / GR21	127 (decimal)	Width	(64 x 2) -1
GR22 / GR23	63 (decimal)	Height	64 - 1
GR24 / GR25	1600 (decimal)	Destination Pitch	800 x 2
GR26 / GR27	1600 (decimal)	Source Pitch	800 x 2
GR28 / GR29 / GR2A	160200 (decimal)	Destination Start	(100 x 1600) + (100 x 2)
GR2C / GR2D / GR2E	0 (decimal)	Source Start	Beginning of display memory
GR30	00 (hex)	BLT Mode	Display to display No color expansion No pattern copy
GR31	02 (hex)	Start / Status	Set bit 1 to 1
GR32	0D (hex)	Raster Operation	Source Copy

This BLT is executed as indicated in the following fragment of pseudo-code:

```
sourceAdrs = sourceStartAdrs;
destAdrs = destStartAdrs;
for (i = 0; i < Height; i++)              /*for each scanline*/
    {
    workingSourceAdrs = sourceAdrs
    workingDestAdrs = destAdrs
    for (j =0; j < Width; j++)            /*for each byte*/
        {
        Process one byte of Destination;
        workingDestAdrs++;                /*to next byte*/
        workingSourceAdrs++;
        }
    sourceAdrs = sourceAdrs + sourcePitch; /*next scanline*/
    destAdrs = destAdrs + destPitch;
    }
```

The BLT engine processes the bytes of a scanline in a destination area, incrementing temporary source and destination addresses after each byte. Multiple bytes are processed in parallel. At the end of each scanline, the respective pitch values are added to the addresses as they were at the beginning of the scanline, moving on to the next scanline. This operation is iterated for the "height" number of times.

All BitBLTs are processed in this general manner. However, some variations include the following:

- For color expansion, the source address is incremented as a bit address rather than a byte address.
- For pattern copies, the source address is incremented until the end of the pattern and is returned to the the source start address, so that the pattern is used over and over.
- When the decrement bit is set, the address is decremented rather than incremented.

A1.4 Raster Operations (ROPS)

In addition to moving bytes from the source area to the destination area, the CL-GD7542's BitBLT engine can use various logical raster operations to combine the source or pattern bytes with the destination bytes. Further, bytes in either the source area or the destination area, or both, can be ignored.

Table A1-2 enumerates the 16 ways in which the source bit (or the pattern bit) and the destination bit can be logically combined. The same value for GR32 is used regardless of whether the operation uses Source or Pattern.

The CL-GD7542's BitBLT engine directly implements all 16 ways of logically combining two operands as shown in Table A1-2. Combinations of three operands can be synthesized from these in the unusual cases where this is necessary.

Table A1–2. Logical Combinations of Bits Using the BitBLT Engine

Source Operation	Microsoft® Name / Raster Operation	Pattern Operation	Microsoft® Name / Raster Operation	GR32 (Hex)
0	BLACKNESS 00000042	0	BLACKNESS 00000042	00
~S.~P	NOTSRCERASE 001100A6	~P.~S	– 000600A9	90
~S.D	– 00220326	~P.D	– 000A0329	50
~S	NOTSRCCOPY 00330008	~P	– 000F0001	D0
S.~D	SRCERASE 00440328	P.~D	– 00500325	09
~D	DSTINVERT 00550009	~D	DSTINVERT 00550009	08
S~=D	SRCINVERT 00660046	P~=D	PATINVERT 005A0049	59
~S~=D	– 007700E6	~P~=D	– 005F00E9	DA
S.D	SRCAND 008800C6	P.D	– 00A000C9	05
S=D	– 00990066	P=D	– 00A50065	95
D	– 00AA0029	D	– 00AA0029	06
~S+D	MERGEPAINT 00BB0226	~P+D	– 00AF0229	D6
S	SRCCOPY 00CC0020	S	PATCOPY 00F00021	0D
S+~D	– 00DD0228	P+~D	– 00F50225	AD
S+D	SRCPAINT 00EE0086	P+D	– 00FA0089	6D
1	WHITENESS 00FF0062	1	WHITENESS 00FF0062	0E

NOTE: S = Source, D = Destination, P = Pattern.

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A1.5 Color Expansion

When GR30[7] is 1, the source input to the ROPS is not actual data from the source area, but is *color-expanded* data. The source area is a monochrome image. Since the source image is a single bit per pixel, substantial performance benefits are possible, especially when the source is being expanded to 16 bits. Color expansion can be used any time a single foreground color, or a single foreground color and a single background color, are to appear in the destination.

The CL-GD7542 supports color expansion for 8-bit-per-pixel and 16-bit-per-pixel modes. The source can be monochrome data from either display memory or system memory. When the source is in display memory, it must be located on a four-byte boundary. When the source is an 8 x 8 pattern, it must be on an eight-byte boundary.

- A 1 in the source area results in the *foreground* color being written into the corresponding byte(s) of the destination area.
- A 0 in the source area results in either the *background* color being written into the corresponding byte(s) of the destination area, or no alteration to the destination area (transparency).

For color expansion, the destination must be in the display memory that is displayed and the direction must be increment. Any ROP may be used, although SRCCOPY is most common when using color expansion.

The most-significant bit of the first source byte is expanded into the ROP source data for the first pixel of the destination. Depending on the contents of GR30[4], it is expanded to one or two bytes. Table A1-3 indicates the registers that contain the expansion colors.

Table A1–3. Color Expansion Registers

GR30[4]	Width	Background Expansion (0 in Source Area)		Foreground Expansion (1 in Source Area)	
		GR0	GR10	GR1	GR11
0	8-bit	Color	Don't care	Color	Don't care
1	16-bit	Low byte	High byte	Low byte	High byte

The next bit of source data is processed for the next one or two bytes of destination, and so on, until the bytes of the scanline in the destination area have been processed. Unused source bits are discarded

The destination address is modified by the destination pitch. The source pitch is ignored since the source is taken to be a linear string of bytes. The next byte of source is the first eight pixels for the next scanline

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A1.6 Color Expansion With Transparency

When GR30[3] is 1, transparency comparison is enabled. Results of a ROP are compared to the contents of the Transparent Color Registers (GR34 / 35) for each pixel. When the results are compared in all bit positions for which the Transparent Compare Mask Registers (GR38/39) are 0, the results are *not* written to display memory. In 8 bits/pixel modes (GR30[4] = 0), registers GR34 and GR35 *must* be programmed identically, as must GR38 and GR39.

When color expansion is used with an opaque foreground and a transparent background (analogous to Extended Write mode 4), the transparency feature must be used, and the transparent color must be set to the background color. The registers used for foreground color expansion with transparency are the same as the color expansion registers with 1 in the source. (Refer to Figure A1-3.)

A1.7 Pattern Fills

In some cases it is necessary to fill an area with a repeating pattern. The CL-GD7542 BitBLT engine has provisions for pattern replication with or without color expansion. The pattern size is 8 pixels x 8 pixels, chosen for compatibility with Microsoft Windows.

When GR30[6] is 1, the source is defined as an array of 8 pixels x 8 pixels. This array is repeatedly copied to the destination area, with color expansion if necessary. For any scanline, the same eight pixels of source data are used repeatedly. The source pitch is ignored. The number of bytes in the source pattern is a function of the operating mode, as indicated in Table A1-4. The starting address boundary of a source pattern is equal to the number of bytes.

Table A1–4. Pattern-Fill Data Size

Operating Mode	Number of Bytes in Source Pattern	Starting Address Boundary
Color Expansion	8 bytes of monochrome data for 64 pixels	8 bytes
8-bit pixels	64 bytes of color data for 64 pixels	64 bytes
16-bit pixels	128 bytes of color data for 64 pixels	128 bytes
32-bit pixels	256 bytes of color data for 64 pixels	256 bytes

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A1.8 BLT Direction

If source and destination areas overlap in display memory, as explained below, ensure that the BitBLT operation progresses so that the source area is not overwritten prior to being used.

Refer to Figure A1-3. If the BitBLT operation were to begin with the upper-left corner of the source and destination, the contents of the overlapped area would be overwritten before being used.

To avoid this effect, GR30[0] must be set to 1 so that the direction in which the BitBLT operation progresses is reversed. As shown in Figure A1-3, the bytes are therefore processed right to left and bottom to top, guaranteeing that bytes of the source are used prior to being changed. Note that in this case, the start addresses are the highest in the areas, not the lowest.

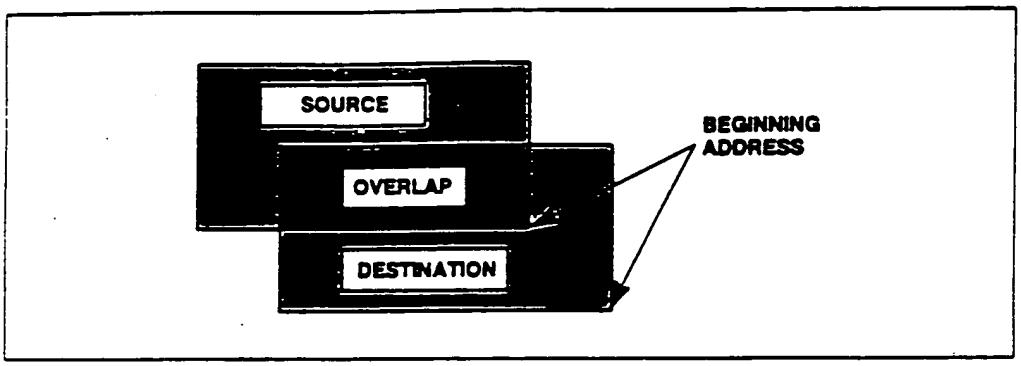


Figure A1–3. Source and Destination Memory Area Overlap – Start Address

A1.9 System Memory

The source area or the destination area, but not both, of a BitBLT can be in system memory. In either case, the CPU must perform the bus transfers in that the CL-GD7542 is never a bus master. For such transfers, the address provided by the CPU is ignored (except it must be in the range being decoded as display memory). The CPU *must* execute DWORD transfers.

- When GR30[2] is a 1, the BLT source is system memory.
  - For system-to-screen BitBLTs, up to three bytes of the last transfer for each scanline are ignored (depending on width of the source and the destination areas). The next scanline begins with the next DWORD transfer.
- When GR30[1] is a 1, the BLT destination is system memory.
  - The CL-GD7542 pads each scanline with up to three indeterminate bytes (depending on width of the source and the destination areas). BLTs involving color expansion or pattern copy cannot use this mode.

A1.10 Start / Suspend / Reset Controls

Once the parameters have been loaded into the registers, the BitBLT can be started, suspended, and then resumed. It is also possible to unconditionally reset the BitBLT engine. These functions are controlled by bits in GR31.

- To start a BitBLT, program GR31[1] to 1. As long as the BLT is in progress, GR31[0] is a 1. When the BLT has completed, GR31[0] changes to a 0.

  Monitoring GR31[0] is the most straight-forward way to synchronize with the BitBLT engine. While the BLT is in progress, the CL-GD7542 display memory and BLT registers (except GR31) must not be accessed for read or write.

- To suspend a BLT, program GR31[1] to 0. Register GR31[0] must be monitored to determine when the BLT has actually been suspended, and it is safe to access display memory. When register GR31[0] is a 0, then the BLT has been successfully suspended or has been completed.

  When a BLT has been suspended, the CPU may access display memory only for write operations. If the program reads display memory during a suspended BLT, working registers are overwritten, and the first few bytes of the BLT will use invalid data, when it is resumed.

  The CPU can determine whether a suspended BLT was actually suspended, or gone to completion coincidentally with the suspension, by reading GR31[3].
  - When GR31[3] is a 1, the BLT was suspended and must be resumed.
  - When GR31[3] is a 0, the BLT was actually completed and need not be resumed.

- To resume, the BLT is resumed by programming GR31[1] to 1. BLTs can be suspended and resumed multiple times.

- To unconditionally stop the current operation, and reset the entire BitBLT engine, programGR31[2] to 1. GR31[3] and GR31[0] are forced to 0 and the operation stops after the next write. This operation may result in partial pixels being written.

  Note that BitBLT operation that is reset *cannot* be resumed.

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A1.11 Complete BLT Register Listing

Table A1-5 lists every register associated with the BitBLT engine.

Table A1–5. BLT Register Listing

Register	How Used	Size (Bits)	Modified?
GR0	Background Color byte 0	8	No
GR1	Foreground Color byte 0	8	No
GR10	Background Color byte 1	8	No
GR11	Foreground Color byte 1	8	No
GR20	Width byte 0	8	–
GR21	Width byte 1	3	–
GR22	Height byte 0	8	Yes
GR23	Height byte 1	2	Yes
GR24	Destination Pitch byte 0	8	No
GR25	Destination Pitch byte 1	4	No
GR26	Source Pitch byte 0	8	No
GR27	Source Pitch byte 1	4	No
GR28	Destination Start byte 0	8	Yes
GR29	Destination Start byte 1	8	Yes
GR2A	Destination Start byte 2	5	Yes
GR2B	Reserved		
GR2C	Source Start byte 0	8	Yes
GR2D	Source Start byte 1	8	Yes
GR2E	Source Start byte 2	5	Yes
GR2F	Destination Write Mask	3	No
GR30	BLT mode	8	No
GR31	Start/Status	4	–
GR32	Raster Operation	8	No
GR34	Transparent Color – Low Byte	8	No
GR35	Transparent Color – High Byte	8	No
GR38	Transparent Color Mask – Low Byte	8	No
GR39	Transparent Color Mask – High Byte	8	No
SR2	Plane Mask	8	No

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A1.12 BLT Registers modified While BLT is Occuring

Some registers associated with a BLT are modified while the BLT is occurring. Therefore, they must be re-written prior to the next BLT, even when the initial values are to be the same.

A1.13 Text Expansion Example

Using color expansion, a text string is copied from system memory, resulting in faster test-write operations. The monochrome image of the string is arranged in system memory by scanline. For example, assume that the destination area is 150 pixels x 25 scanlines, 8 bits per pixel. The destination pitch is 1024 pixels. The registers must be loaded as indicated in Table A1-6. When the background pixels are not to be written, GR30[3] must be set to 1.

Table A1–6. Typical Register Settings for Color-Text Expansion

Register(s)	Register Contents (Decimal)	Register Description	How Calculated?
GR0 / GR10	Don't Care	Background Color	-
GR1 / GR11	Don't Care	Foreground Color	-
GR20 / GR21	149 (decimal)	Width	150 - 1
GR22 / GR23	24 (decimal)	Height	25 - 1
GR24 / GR25	1024 (decimal)	Destination Pitch	-
GR26 / GR27	n/a	Source Pitch	(System memory)
GR28 / GR29 / GR2A	Don't Care	Destination Start	-
GR2C / GR2D / GR2E	n/a	Source Start	(System memory)
GR30	84 (hex)	BLT Mode	Color Expansion, Source = System Memory
GR31	02 (hex)	Start / Status	Set bit 1
GR32	0D (hex)	Raster Operation	SRC COPY

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After the registers are loaded, the source bitmap must be transferred.

- The first DWORD write transfers the image for pixels 0 to 31.
- The second write transfers the image for pixels 32 to 63.
- The third transfers the image for pixels 64 to 95.
- The fourth transfers the image for pixels 96 to 127.
- The data sent in the fifth DWORD transfer is shown in Figure A1-4.

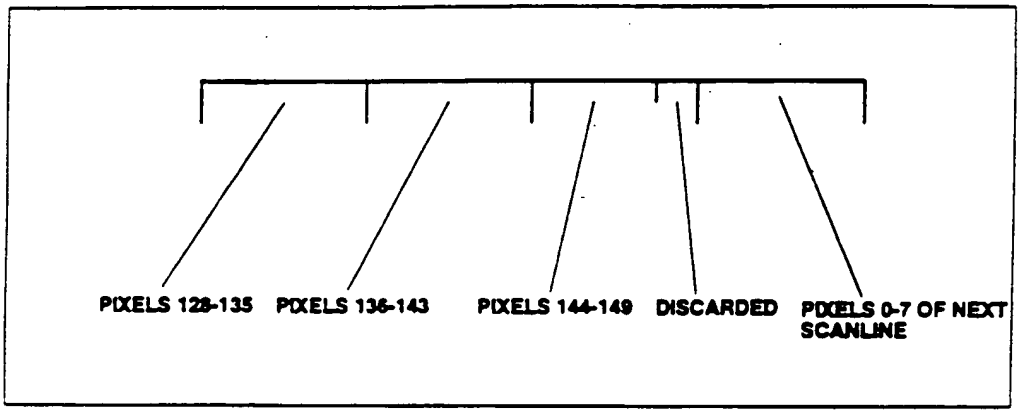


Figure A1–4. Color Expand Transfer

A total of 119 DWORD transfers are required. The last one byte of the last transfer is discarded.

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Appendix A2

Hardware Cursor

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A2. Hardware Cursor

A2.1 Introduction

The CL-GD7542 is capable of supporting a 32 x 32 or 64 x 64 hardware cursor (mouse pointer) in 16-color planar, 256-, 32K-, and 64K-color packed-pixel graphics modes.

Multiple hardware cursor patterns can be loaded into the upper display memory area, allowing application programs to select one of the patterns as an active-cursor pattern.

The hardware cursor (mouse pointer) replaces a software mouse pointer commonly used by Graphics User Interface (GUI) applications. The hardware cursor eliminates the need for application software to save and restore the screen data as the mouse pointer position changes.

After initializing the hardware cursor, the application software needs only to update the cursor position (x,y) to move the cursor on the screen. Compared to a software cursor, the hardware cursor offers a smooth-moving mouse pointer with improved performance.

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A2.2 Hardware Cursor Operation

Each pixel in the hardware cursor consists of two bits: bit 1 and bit 0. The following table shows how the two bits determine the displayed data of each cursor pixel.

Table A2–1. Hardware Cursor Bits

Bit 0	Bit 1	Displayed Data of Hardware Cursor Pixel
0	0	Transparent
0	1	Inverted VGA Display Data
1	0	Cursor color 0
1	1	Cursor color 1

The cursor colors 0 and 1 are supplied by the internal palette DAC's two extra Lookup Table (LUT) locations which are mapped into the existing LUT indexes 00h and 0Fh, respectively. As a result, the hardware cursor colors are independent of the existing LUT indexes 00h through FFh.

The CL-GD7542 extension register SR12, the Video Datapath Control Register, can be programmed:

- to enable or disable the cursor
- to select the cursor size
- to enable access to the Palette DAC cursor colors
- to enable cursor movement

The hardware cursor data is located in the top 8 Kbytes of the display memory. The number of cursor patterns that can be loaded in the display memory at one time is either 32 (for 32 x 32 bit cursors) or 8 (for 64 x 64 bit cursors). One of the cursor patterns loaded in display memory is selected as the active-cursor pattern using the Graphics Cursor Pattern Address Offset Register (SR13).

The hardware cursor position is controlled by programming the hardware cursor horizontal (X) position and hardware cursor vertical (Y) position. The 11-bit cursor X-location and Y-location values are programmed by initiating two 16-bit I/O writes to:

1. SRX (3C4h) and SR10 (3C5h): Horizontal position
2. SRX (3C4h) and SR11 (3C5h): Vertical position

where the SRX[7:5] bits of the Index Register are the least-significant bits of the 11-bit value, and the SRX[4:0] bits are the index into the horizontal and vertical position registers. Moving the cursor always requires writing to both the horizontal and vertical position registers.

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The horizontal position is written first but does not take effect until the vertical position is updated.

NOTE: The horizontal fine-position control requires one more bit for those expanded-graphics modes that use 10-dot character clocks. For these special cases (for example, 640 x 480 graphics expanded for 800 x 600 LCDs), the most-significant bit for the fine-position adjustment is in SR2E[0], which is appended to the index bits SRX[7:5]. For standard non-expanded graphics modes, SR2E[0] is always 0 and can be ignored when moving the cursor.

The following table shows the CL-GD7542 Extension Registers bits that are needed for programming the hardware cursor:

Table A2–2. Extension Registers Bits For Programming Hardware Cursor

To:	Program:			
	Index or Extension Register	I/O Port Address	Register Bits	Value
Enable hardware cursor	SR12	3C5h	[0]	1
Access graphics palette DAC colors	SR12	3C5h	[1]	1
Set hardware cursor size (32 x 32)	SR12	3C5h	[2]	0
Set hardware cursor size (64 x 64)	SR12	3C5h	[2]	1
Enable hardware cursor movement	SR12	3C5h	[3]	0
Select hardware cursor pattern (32 x 32)	SR13	3C5h	[4:0]	31..0
Select hardware cursor pattern (64 x 64)	SR13	3C5h	[4:2]	7.0
Set hardware cursor horizontal position	SRX/SR10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	[7:5]/[7:0]	2047..0
Set hardware cursor horizontal position fine-position extension (msb) for expanded graphics	SR2E	3C5h	[0]	0:Non-Exp. 1:Expanded
Set hardware cursor vertical position	SRX/SR11, 31, 51, 71, 91, B1, D1, F1	3C4h/3C5h	[7:5]/[7:0]	2047..0
Enable 64 x 64 hardware cursor memory mapping	SR21	3C4h/3C5h	[4]	1

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A2.3 The 32 X 32 Hardware Cursor

Each 32 x 32 cursor pattern requires 256 bytes (128 bytes per cursor pixel bit x 2 cursor pixel bits), which allows for 32 cursor patterns to be loaded into 8 Kbytes of the hardware cursor data area in the display memory. The active cursor pattern is selected by programming the Graphics Cursor Pattern Address Register bits (SR13[4:0]).

The hardware cursor data and the hardware icon data are loaded into the top 16 Kbytes of the display memory as follows:

- The hardware icon data is loaded into the top 8 Kbytes of the display memory.
- The hardware cursor data is loaded into the next 8 Kbytes of the display memory.

For more information about the hardware icon, refer to Appendix 3.

The 32 x 32 hardware cursor pattern data from cursor pixel bit 0 and cursor pixel bit 1 is loaded into the display memory as shown in the following figure:

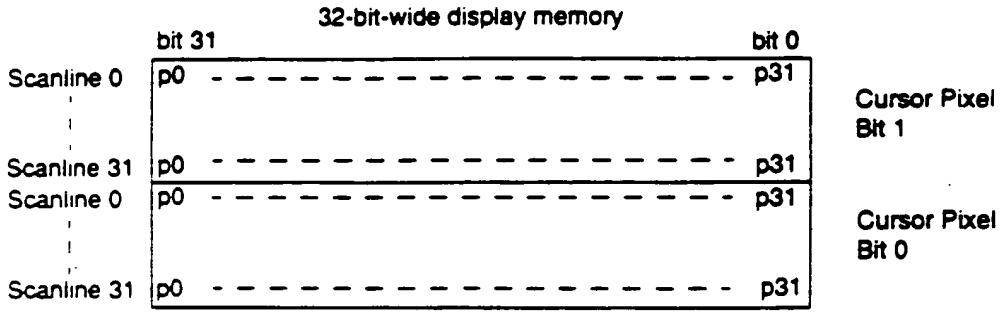


Figure A2—1. Mapping of 32 x 32 Hardware Cursor

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A2.4 The 64 x 64 Hardware Cursor

Each 64 x 64 cursor pattern requires 1024 bytes (512 bytes per cursor pixel bit x 2 cursor pixel bits), which allows for 8 cursor patterns to be loaded into 8K of the hardware cursor data area. The active hardware cursor pattern is selected by programming the Graphics Cursor Pattern Address Register bits (SR13[4:2]).

The 64 x 64 hardware cursor pattern data from cursor pixel bit 0 and cursor pixel bit 1 is loaded into display memory one cursor scanline at a time. The same action takes place until all 64 scanlines from cursor pixel bit 0 and cursor pixel bit 1 are loaded into the system memory as shown in the following figure:

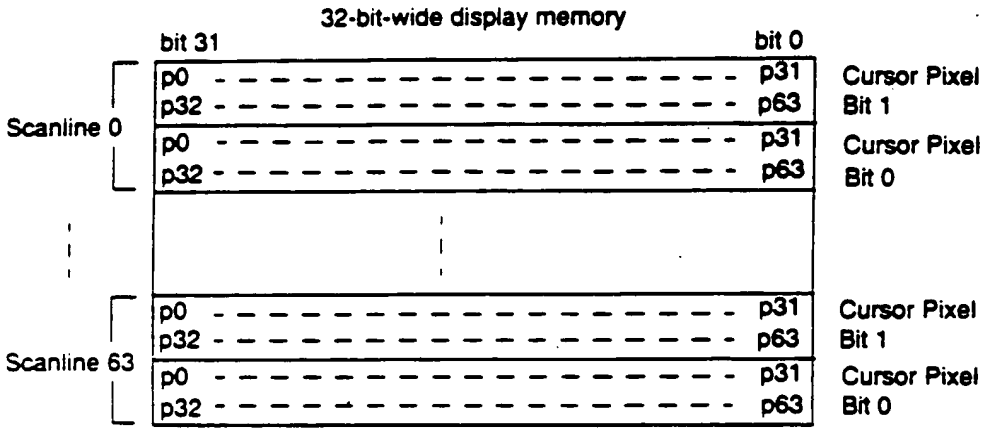


Figure A2-2. Mapping of 64 x 64 Hardware Cursor

To get proper 64 x 64 hardware cursor mapping, Extension Register SR21[4] bit must be set to 1.

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The following table shows the location of the hardware cusrsor memory map within the display memory.

Table A2–3. Hardware Icon Memory Map in 1-Mbyte Display Memory

Address	32 x 32 Hardware Cursor	64 x 64 Hardware Cursor
3FF00-3FFFF	Cursor Map #28 - Cursor Map #31	Cursor Map #7
3FE00-3FEFF	Cursor Map #24 - Cursor Map #27	Cursor Map #6
3FD00-3FDFF	Cursor Map #20 - Cursor Map #23	Cursor Map #5
3FC00-3FCFF	Cursor Map #16 - Cursor Map #19	Cursor Map #4
3FB00-3FBFF	Cursor Map #12 - Cursor Map #15	Cursor Map #3
3FA00-3FAFF	Cursor Map #8 - Cursor Map #11	Cusor Map # 2
3F900-3F9FF	Cursor Map #4 - Cursor Map #7	Cursor Map #1
3F800-3F8FF	Cursor Map #0 - Cursor Map #3	Cursor Map #0

NOTE: For the 32 x 32 hardware cursor, four hardware-cursor data patterns occupy 3Fx00 through 3FxFF. Their respective addresses (x = 8 - F) are:
3Fx00 - 3Fx3F
3Fx40 - 3Fx7F
3Fx80 - 3FxBF
3FxC0 -3FxFF

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Appendix A3

Hardware Icon

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A3. Hardware Icon

A3.1 Introduction

A hardware icon (a hardware-driven icon window), as compared to a software icon, eliminates the need for application software to save and restore the screen data as the icon position changes.

In various operational modes, the CL-GD7542 Super VGA LCD Controller is capable of supporting four hardware icons with the following features:

- One to four icons displayed simultaneously on the screen.
- Icon size is 64 x 64 pixels.
- Icon size can be doubled vertically and/or horizontally to 64 x 128- 128 x 64-, and 128 x 128- pixels.
- Up to eight icon maps may be defined in display memory for use and are associated with the displayed hardware icons in two ways:
  - Two maps for each hardware icon
  - All eight maps used with the first hardware icon.
- A single location known as a hot spot is used to define the screen position of all of the icons. This hot spot defines the upper left-hand corner of the first icon. All subsequent icons are left aligned vertically down from the first icon.
- The hot spot is positioned at a resolution of one pixel.
- Each icon independently controls the following:
  - Display Enable
  - Display Mode: 4 colors, or 3 colors + transparency
  - Blink Enable: at either blink rate, or at one-half the icon blink rate
  - Horizontal Pixel Doubling
  - Vertical Pixel Doubling
  - Memory Map Selection
- The hardware icons have the second most display priority in the video sub-system. Only the hardware cursor will appear on top of the icon.

The hardware icon memory model and programming model are very similar in usage to that of the hardware cursor. The memory used to define the icon maps is at the top of the available display memory space and is fixed by the GD7542.

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A3.2 Hardware Icon Operation

The CL-GD7542 Video Datapath Control Register (SR12), and Hardware Icon Control Registers (SR2A / SR2B / SR2C / SR2D) can be programmed for the following:

- to enable/disable the icon
- to select the icon size
- to enable access to the Palette DAC icon colors
- to enable icon movement.

The hardware icon data is located in the bottom 8 Kbytes of the of the top 16 Kbytes of available display memory. The number of icon patterns that can be loaded in the display memory at one time is eight 64x 64bit- icons (of which four can be simultaneously displayed). These patterns can be defined as either two patterns per icon, or all eight patterns can be displayed on the first icon allowing all of the patterns to be displayed at the same location without having to update the icon hot spot.

A3.2.1 Icon Color

Each hardware icon pixel consists of two bits: The icon pixel bit 0 and the icon pixel bit 1. The following table shows how the two bits determine the displayed state of each icon pixel.

Table A3–1. Hardware Icon Pixel Bits

Icon Pixel Bit 0	Icon Pixel Bit 1	Displayed Data of Hardware Icon Pixel
0	0	Transparent / Icon Color 0
0	1	Icon Color 1
1	0	Icon Color 2
1	1	Icon Color 3

The icon colors 0 and 3 are supplied by the internal palette DAC's four extra Lookup Table (LUT) locations which are mapped into the existing LUT indexes 03h, 04h, 05h, and 06h, respectively. As a result, the hardware cursor colors are independent of the existing LUT indexes 00h through FFh.

- When enabled by setting SR12 [1] to 1, these four additional palette locations are accessible the same way as their standard VGA counterparts.
- Clearing SR12 [1] to 0 restores standard VGA operation to the palette.

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A3.2.2 Icon Position

The hardware icon position is controlled by programming the Graphics Icon Horizontal (X) position and Graphics Icon Vertical (Y) position. The hardware icon position is programmed the same way as the hardware cursor using the same I/O addresses. The GD7542 distinguishes the difference between the two operations by the state of register bit SR12 [3].

- When SR12 [3] = 0, writing X and Y position data will control the position of the hardware cursor.
- When SR12 [3] = 1, writing X and Y position data will control the position of the hot spot of the hardware icons.

The 11-bit icon X-location and Y-location values are programmed by initiating two 16-bit I/O writes to:

- SRX (3C4h) and SR10 (3C5h): Horizontal position
- SRX (3C4h) and SR11 (3C5h): Vertical position

where SRX[7:5] of the Index Register are the least-significant bits of the 11-bit value, and SRX[4:0] is the index into the horizontal and vertical position registers. Moving the icon always requires writing to both the horizontal and vertical position registers. The horizontal position is written first, but it does not take effect until the vertical position is updated.

NOTE: The horizontal fine-position control requires one more bit for those expanded-graphics modes that use 10-dot character clocks. For these special cases (for example, 640 x 480 graphics expanded for 800 x 600 panels), the most-significant bit for the fine-position adjustment is in SR2A[6], which is appended to the index bits SRX[7:5]. For standard non-expanded graphics modes, SR2A[6] is always 0, and can be ignored when moving the icon.

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The following figure shows the hot spot and vertical alignment of the icons as they appear on the display.

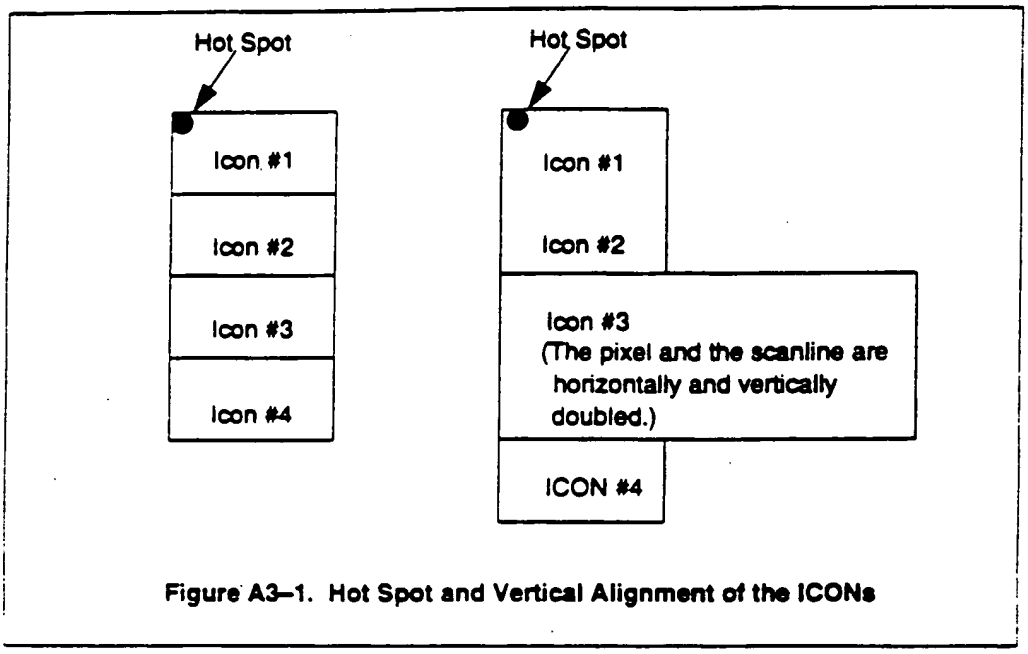


Figure A3–1. Hot Spot and Vertical Alignment of the ICONs

The following table shows the CL-GD7542 Extension Registers bits needed for programming the hardware icon.

Table A3-2. Extension Registers Bits for Programming Hardware Icon

To:	Program:			
	Extension Register	I/O Port Address	Register Bits	Value
Enable hardware icon	SR2x[1]	3C5h	[0]	1
Display 3 colors + transparency	SR2x[1]	3C5h	[1]	1
Display 4 colors	SR2x[1]	3C5h	[1]	0
Enable blink	SR2x[1]	3C5h	[2]	1
Double horizontal pixel	SR2x[1]	3C5h	[3]	1
Double vertical scanline	SR2x[1]	3C5h	[4]	1
Select memory map	SR2x[1]	3C5h	[5]	0 or 1
Select icon #0 eight memory maps option	SR2E	3C5h	[2:1]	11, 10, 01, 00
Set hardware icon horizontal position[2]	SRX / SR10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	[7:5]/[7:0]	2047...0
Set icon horizontal position fine-position extension (msb) for expanded graphics	SR2A	3C5h	[6]	0: Non-Exp. 1: Expanded
Set hardware icon vertical position[2]	SRX / SR11, 31, 51, 71, 91, B1, D1, F1	3C4h/3C5h	[7:5]/[7:0]	2047...0

1. The x represents the four available icon programming registers; 2Ah, 2Bh, 2Ch, and 2Dh, which correspond to the GD7542's four hardware icons.
2. The icon position is programmed the same way as the hardware cursor using the same I/O addresses. The state of SR12[3] determines either the icon position or the cursor position are being updated.

A3.2.3 Memory Map Option

The eight CL-GD7542icon maps can be configured in two ways:

- Two maps per icon
- All eight maps available to icon #0

Register SR2E [2.1] controls this option.

- When this field is zero, the corresponding map pair that is displayed is icon #0.
- When this field is non-zero, only Icon #0 can be used, and it has accesses to all eight memory maps. The non-zero number points to the corresponding map pair that is displayed as Icon #0.

The member of the map pair that is actually displayed is selected by the state of SR2A [5]. For example, if SR2E [2:1] = 11 and SR2A[5]=0 then map #6 will be displayed as icon #0. For memory map details, refer to Table A3-3 .

When SR2E[2:1] field is non-zero, icons #1, #2, and #3 should be disabled.

A3.3 Hardware Icon Memory Map And Data Format

The following table shows the location of the hardware icon memory maps within the display memory.

Table A3–3. Hardware Icon Memory Map in 1-Mbyte Display Memory

Address	Hardware Icon Memory Map
3F700-3F7FF	Icon #3 Map #1 or Icon #0 Map #7
3F600-3F6FF	Icon #3 Map #0 or Icon #0 Map #6
3F500-3F5FF	Icon #2 Map #1 or Icon #0 Map #5
3F400-3F4FF	Icon #2 Map #0 or Icon #0 Map #4
3F300-3F3FF	Icon #1 Map #1 or Icon #0 Map #3
3F200-3F2FF	Icon #1 Map # 0 or Icon #0 Map #2
3F100-3F1FF	Icon #0 Map #1
3F000-3F0FF	Icon #0 Map #0

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The actual data that is stored in display memory to define the icon is written with two bits of data per pixel, as defined in Section A.3.2.1, "Icon Color". The following figure shows how the 64 pixels x 64 pixels icon is stored in 32-bit-wide display memory.

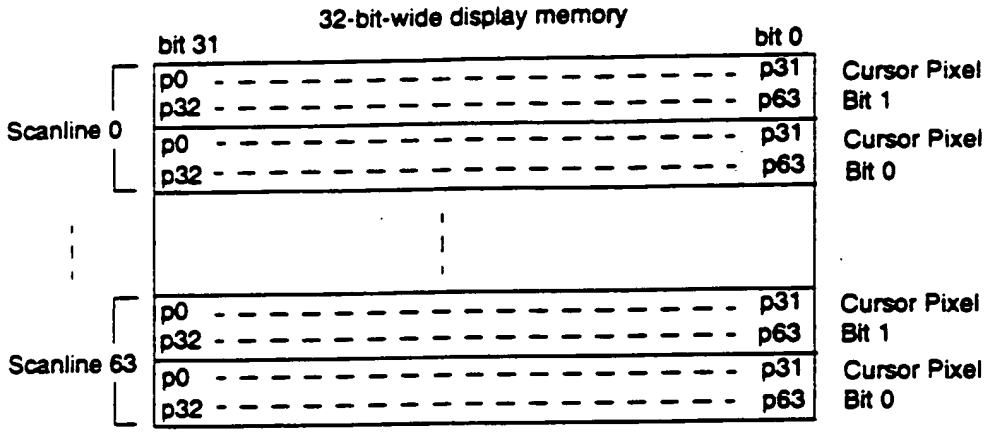


Figure A3-2. Icon (64 Pixels x 64 pixels) Stored in the Display Memory

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Appendix A4

Color Expansion and

Extended Write Modes

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A4. Color Expansion And Extended-write Modes

A4.1. Introduction

The CL-GD7542 supports color expansion, using extended-write modes for faster CPU write performance. In graphics modes, these extended write modes can be used for the following operations: faster text write, pattern fill, and block move operations. In 8- or 16-bit-per-pixel graphics modes with packed-pixel addressing, these write modes operate on 8 pixels at a time.

A4.2. Color Expansion

Color expansion is the automatic conversion of a monochrome bit map, typically defining a character, icon, or pattern into foreground and background color values that are written into display memory. The foreground and background color values are held in the CL-GD7542, and only the monochrome bit maps need be transmitted across the bus. Each bit of the monochrome map is converted into an 8-bit or 16-bit pixel value: The bus traffic is reduced accordingly.

A4.3. Registers Involved In Color Expansion

The following register bits are involved in color expansion.

Table A4–1. Color Expansion Registers

Register Bit	Function
SR2[7:0]	Enable Writing Pixels
GRB[2]	1 enables Extended Write Modes
GRB[4]	1 enhances Extended Write Modes to 16-bit pixels
GR5[2:0]	100 chooses Extended Write Mode 4 101 chooses Extended Write Modes 5
GR0[7:0]	Extended Write Mode 5 Background Color Low Byte
GR1[7:0]	Extended Write Mode 4/5 Foreground Color Low Byte
GR10[7:0]	Extended Write Mode 5 Background Color High Byte
GR11[7:0]	Extended Write Mode 4/5 Foreground Color High Byte

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A4.4. Extended Write Modes

The CL-GD7542 supports two extended write modes: Extended Write Modes 4 and 5. These extended write modes can selectively update up to eight pixels of 8 or 16 bits each. For more information, refer to sections A4.8. and A4.9.

The extension register GRB, Graphics Controller Mode Extensions Register, bits [4:1] are used in combination to enable the CL-GD7542 Extended Write Modes.

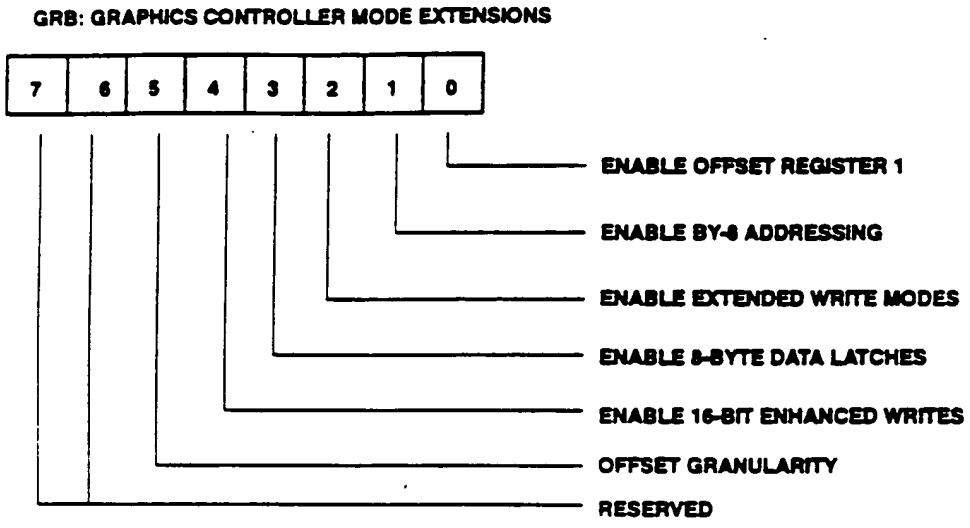


Figure A4–1. Extension Register GRB

When Extended Write Modes are enabled by setting GRB[2] to 1:

- Up to eight bytes can be transferred to display memory for every CPU byte transfer.
- GR5[2], the Mode Register bit, is enabled to select Extended Write Modes 4 and 5.
- GR0[7:0], the Set/Reset Register, extends read/write values for Extended Write Mode 5 Background Color.
- GR1[7.0], the. Enable Set/Reset Register, extends read/write values for Write Mode 4/5 Foreground Color.
- SR2[3:0], the Map Mask Register bits, extends to SR2[7:0] for Write Modes 4 and 5.
- GRB[4], the Graphics Controller Mode Extensions Register bit, is enabled so that it can select enhanced writes for Write Modes 4 and 5.

A4.5. By-8 Addressing

GRB[1], when set to 1, selects By-8 addressing for 8-bit-per-pixel (256-color) video modes. The system address is shifted left by three bits relative to packed-pixel addressing so that each system byte address points to a different 8 pixel (8 bytes) block in display memory.

This GRB[1] bit, in combination with GRB[2], is used for selecting extended write modes. This bit is a don't care when GRB[4] is 1.

A4.6. By-16 Addressing

GRB[4], in combination with GRB[2], is used to select Write Mode 4 and 5 for 16-bits-per-pixel graphics modes (RGB 555 or 565). The system address is shifted left by four bits relative to packed-pixel addressing so that each system byte address points to a different 8 pixels (16 bytes) block in display memoyr.

GRB[4] and GRB[2], when set to 1, select the following write mode operation:

- Enables By-16 addressing.
- Enables up to 16 bytes (eight pixels) to be transferred for each CPU byte cycle.
- Enables GR10 and GR11 as high-byte data for foreground and background color extensions. (GR0 and GR1 contain the low-byte data.)
- Enables each bit of SR2 to be used as pixel write mask for two bytes.

A4.7. Data Latches

When GRB[3] is set to 1, the memory read latches are eight bytes wide, instead of the normal four. Eight-byte wide memory read latches can be used in Write Mode 1 to write eight latched bytes back into display memory. This action allows either eight pixels in 256-color modes or four pixels in 16-bit/pixel modes to be updated in a single CPU byte cycle.

A4.8. Extended Write Mode 4

The CL-GD7542 supports Extended Write Mode 4, which is used in combination with BY-8 or BY-16 addressing modes to operate on eight pixels of data at a time (8 or 16 bytes, depending on 8-bit or 16-bit-per-pixel mode).

- In 8 bits per pixel mode, the Foreground Color Bits GR1[7:0] are used to update each pixel byte in display memory.
  - The 8-bit value is written as the foreground color when the corresponding CPU data is a 1, and the corresponding Map Mask Register bit in SR2 is also set to a 1.
  - When the CPU Data bit is a 0, the corresponding pixel in display memory is not changed by the write.
- In 16 bits per pixel mode, the Foreground Color Register bits GR11[7:0] (foreground-color high byte) and GR1[7:0] (foreground-color low byte) are used to update each pixel word in display memory.
  - When the corresponding CPU data is 1 and the corresponding Map Mask Register bit in SR2 is also 1, the 16-bit value is written as the Foreground Color.
  - When the CPU data bit is 0, the corresponding pixel in display memory is not changed by the write.

This mode, for example, can be used to write text to display memory with the foreground color while preserving the background color. This action allows eight pixels of display data to be updated with a single CPU byte cycle.

A4.9. Extended Write Mode 5

The CL-GD7542 supports Write Mode 5, which is used in combination with x8 or x16 addressing mode to operate on eight pixels of data at a time (8 or 16 bytes based on 8-bit or 16-bit-per-pixel mode). This mode can be used to write text to display memory with a selected Foreground Color and a Background Color. This action allows eight pixels of display data to be updated with a single CPU byte cycle.

- In 8-bit/pixel mode, the Foreground Color bits GR1[7:0] or the Background Color Register bits GR0[7:0] are used to update each pixel byte in display memory.
  - When the corresponding CPU data is 1, the 8-bit value is written as the foreground color.
  - When the CPU data bit is 0, the corresponding pixel in display memory is written with the background color.
  - The corresponding Map-Mask Register, SR2[7:0], also inhibits writes to selected pixel in display memory.
- In 16-bit/pixel mode, the Foreground-Color bits GR11[7:0] (foreground-color high byte) and GR1[7:0] (foreground-color low byte), or the Background Color GR10[7:0] (background-color high byte) and GR0[7:0] (background-color low byte), are used to update each pixel word in display memory.
  - When the corresponding CPU data is 1, the 16-bit value is written with the foreground color.
  - When that CPU data bit is 0, the corresponding pixel in display memory is written with the background color.
  - The corresponding Map-Mask Register, SR2[7:0], also inhibits the corresponding pixel value (two bytes) to be written to display memory.

Appendix A5

True-Color Modes

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A5. True-color Modes

A5.1 Introduction

The CL-GD7542 has a built-in true-color multi-mode palette DAC that supports the following modes:

- 8 bits per pixel (VGA-standard 256-color Palette Mode)
- 15 bits per pixel (32K color, the 5-5-5 Sierra Mode™)
- 16 bits per pixel (64K color, the 5-6-5 XGA™ Mode)
- 24 bits per pixel (16.8-million color, the 8-8-8 True-Color Mode)
- Mix Mode: Either 15 bits per pixel (5-5-5 Mode) or 8 bits per pixel(standard VGA Mode)

In the 256-color Palette Mode, the Palette DAC is VGA compatible and provides 256 simultaneous colors out of a palette of 256K on the display screen.

A5.2 Programming for a True-color Multi-mode Palette DAC

Extended Color Modes are enabled by the Hidden DAC Register (HDR at I/O Port 3C6h). At reset, this register is loaded with 00h, which programs the Palette DAC in a VGA-compatible mode. In this mode, the Palette DAC is functionally equivalent to the industry-standard Brooktree® BT476 RAMDAC™. By writing code to the Hidden DAC Register, the Palette DAC can be programmed in one of the modes mentioned above.

The following method is used to write to the Hidden DAC Register:

Step 1: Read from the Pixel-Mask Register (3C6h) four times in succession. No other reads/writes should be directed to that address.

Step 2: After the fourth read, the Pixel-Mask Register points to the Hidden DAC Register. At this time, the Hidden DAC Register can be programmed by writing to it at Port 3C6h. Any read from or write to any address, other than the Pixel-Mask Register, will reset an internal counter which 'hides' the Hidden DAC Register again. To continue, repeat Step 1.

Table A5–1. Extended Color Mode Selected with the Hidden DAC Register

HDR								Function
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0	X	X	X	X	X	X	X	Standard VGA Compatible 256-color Mode
1	1	1/0	0	0	0	0	0	5-5-5 Mode (32K colors,Sierra™)
1	1	1/0	1	0	0	0	0	5-5-5 and 256-color Mix Mode
1	1	X	0	0	0	0	1	5-6-5 Mode (64K colors, XGA™)
1	1	X	0	0	1	0	1	8-8-8 Mode (16.8-million colors, True Color Mode)

NOTE. In 5-5-5 Mode (Sierra™):
- Programming HDR[5] to 0 chooses Clocking Mode 1.
- Programming HDR[5] to 1 chooses Clocking Mode 2.

When using a video overlay feature of the CL-GD7542, choose Clocking Mode 1.

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A5.2.1 5-5-5 Mode with 32K Colors

This mode supports the industry-standard 5-5-5 RGB mode with 32,768 colors. Each pixel is represented by 15 bits containing five bits of Red, Green, and Blue color information. The input sequence for each pixel is the low byte first, followed by the high byte.

The first low byte will be taken on the first rising edge of clock occuring after BLANK# has gone inactive (high).

- In Clocking Mode 2 (HDR[5] = 1), all subsequent bytes are clocked in on the rising edge of the clock.
- In Clocking Mode 1 (HDR[5] = 0), the low bytes are clocked in on the rising edige of the clock and the high bytes are clocked in on the falling edge of the clock .

This mode ignores the palette DAC's Lookup Table.

Table A5–2. Pixel Data Format in 5-5-5 Mode

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
X	RED					GREEN					BLUE				

A5.2.2 5-6-5 Mode with 64K Colors (XGA™)

This mode supports the XGA™ 5-6-5 RGB Mode with 65,536 colors. Each pixel is represented by 16 bits containing five bits of Red, six bits of Green, and five bits of Blue color information. The input sequence for each pixel is the low byte first, followed by the high byte., by using the Clocking Mode 1 or 2. The first low byte will be taken on the first rising edge of clock occurring after BLANK# has gone inactive (high).

- In Clocking Mode 2 (HDR[5] = 1), all subsequent bytes are clocked in on the rising edge of clock.
- In Clocking Mode 1 (HDR[5] = 0), the low bytes are clocked in on the rising edge of the clock, and the high bytes are clocked in on the falling edge of the clock.

This mode ignores the palette DAC's Lookup Table..

Table A5–3. Pixel Data Format in 5-6-5 Mode with 64K Colors

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4	3	2	1	0	5	4	3	2	1	0	4	3	2	1	0
RED					GREEN						BLUE				

A5.2.3 8-8-8 Mode with 16.8 Million Colors (True Color Mode)

This mode supports the industry-standard 8-8-8 RGB Mode with 16,777,216 colors. Each pixel is represented by 24 bits containing one byte each of Red, Green, and Blue color information. The input sequence for each pixel is the low byte (Blue) first, followed by the middle byte (Green), followed by the high byte (Red).

This mode uses Clocking Mode 2 (HDR[5] = 1). The first low-byte is taken on the first rising edge of clock occurring, after BLANK# has gone inactive (high). All subsequent bytes are clocked in on the rising edge of clock. This mode ignores the palette DAC's Lookup Table. .

Table A5–4. Pixel Data Format in 8-8-8 Mode with 16.8 Million Colors

MSB HIGH BYTE								MIDDLE BYTE								LOW BYTE LSB							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

A5.2.4 Mix Mode

When HDR[4] is set to 1, the pixel data bit [15] will be used to select between 5-5-5 RGB Mode and the standard VGA compatible, 256-color mode.

Table A5–5. Pixel Data Format in 5-5-5 Mode of the Mix Mode

MSB HIGH BYTE								LOW BYTE LSB							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
5-5-5 Mode	RED					GREEN					BLUE				

Table A5–6. Pixel Data Format in 256-Color Mode of the Mix Mode

MSB HIGH BYTE								LOW BYTE LSB							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	7	6	5	4	3	2	1	0
256-Color Mode	Ignored							Palette DAC's Lookup-Table Input							

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Appendix A6

Memory Configurations

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A6. Memory Configurations

A6.1 Introduction

The CL-GD7542 supports scalable 32-bit-wide display-memory configurations, from 1 Mbyte to 2 Mbytes, using the following types of DRAMs.

- 512K x 8
- 256K x 16 – dual-CAS#
- 256K x 16 – dual-WE#

A6.2 Possible Memory Configurations

Table A6-1 shows the possible memory configurations that the CL-GD7542 supports.

For 256K x 16 DRAM configurations, the total display memory can be expanded from 1 M byte to 2 Mbytes. The 512K x 8 DRAM configuration must be 2 Mbytes. Some signals of the CL-GD7542 change functions according to the DRAM organization that is used.

For optimum performance, choose multiple-CAS# configurations over multiple WE# configurations.

Table A6–1. CL-GD7542 Memory Configurations

Total Display Memory Size	Memory Bus Width	DRAMs	
		Number	Type
1 Mbyte	32 bits	2	256K x 16
2 Mbytes[a]	32 bits	4	512K x 8
2 Mbytes[b]	32 bits	4	256K x 16

NOTES: [a] The DRAM Control Register bit SRF[7] = 0
[b] The DRAM Control Register bit SRF[7] = 1

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A6.3 Control Signals for Various Memory Configurations

The following five tables indicate how the CL-GD7542 and the DRAMs must be connected.

Table A6–2. 2-Mbytes Display Memory: Four 512K x 8 DRAMs

DRAM Pins Connected to the CL-GD7542	The CL-GD7542 Pins Connected to the DRAMs			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
OE#	OE#	OE#	OE#	OE#
WE#	WE#	WE#	WE#	WE#
CAS#	CAS0#	CAS1#	CAS2#	CAS3#
RAS#	RAS0#	RAS0#	RAS0#	RAS0#
ADDR[9:0]	MA[9:0]	MA[9:0]	MA[9:0]	MA[9:0]
DATA	MD[7:0]	MD[15:8]	MD[23:16]	MD[31:24]
Bit Plane Stored in Each DRAM	3	2	1	0

NOTE: This configuration is Multiple-CAS#, Common-WE# (SRF[0] = 1).

Table A6–3. 1-Mbyte Display Memory: Two 256K x 16 DRAMs: — Dual-CAS# Type

DRAM Pins Connected to the CL-GD7542	The CL-GD7542 Pins Connected to the DRAMs	
	To DRAM #1	To DRAM #2
LCAS#	CAS2#	CAS0#
UCAS#	CAS3#	CAS1#
OE#	OE#	OE#
RAS#	RAS0#	RAS0#
WE#	WE#	WE#
ADDR[8:0]	MA[8:0]	MA[8:0]
ADDR[9]	not valid	not valid
DATA	MD[31:16]	MD[15:0]
Bit Planes Stored in Each DRAM	0,1	2,3

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Table A6–4. 1-Mbyte Display Memory:Two 256K x 16 DRAMs — Dual-WE# Type

DRAM Pins Connected to the CL-GD7542	The CL-GD7542Pins Connected to the DRAMs	
	To DRAM #1	To DRAM #2
LWE#	WE2#	WE0#
UWE#	WE3#	WE1#
OE#	OE#	OE#
RAS#	RAS0#	RAS0#
CAS#	CAS#	CAS#
ADDR[8:0]	MA[8:0]	MA[8:0]
ADDR[9]	not valid	not valid
DATA	MD[31:16]	MD[15:0]
Bit Plane Stored in Each DRAM	0,1	2,3

Table A6–5. 2-Mbytes Display Memory: Four 256K x 16 DRAMs — Dual-CAS# Type

DRAM Pins Connected to the CL-GD7542	The CL-GD7542 Pins Connected to the DRAMs			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
LCAS#	CAS2#	CAS0#	CAS2#	CAS0#
UCAS#	CAS3#	CAS1#	CAS3#	CAS1#
OE#	OE#	OE#	OE#	OE#
RAS#	RAS0#	RAS0#	RAS1#	RAS1#
WE#	WE#	WE#	WE#	WE#
ADDR[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[31:16]	MD[15:0]	MD[31:16]	MD[15:0]
Bit Planes Stored in Each DRAM	0,1	2,3	0,1	2,3

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Table A6–6. 2-Mbytes Display Memory: Four 256K x 16 DRAMs — Dual-WE# Type

DRAM Pins	The CL-GD7542Pins			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
LWE#	WE2#	WE0#	WE2#	WE0#
UWE#	WE3#	WE1#	WE3#	WE1#
OE#	OE#	OE#	OE#	OE#
RAS#	RAS0#	RAS0#	RAS1	RAS1
CAS#	CAS#	CAS#	CAS#	CAS#
ADDR[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[31:16]	MD[15:0]	MD[31:16]	MD[15:0]
Bit Planes Stored in Each DRAM	0,1	2,3	0,1	2,3

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Appendix A7

Clock Options

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A7. Clock Options

A7.1 Introduction

The dual-frequency synthesizer in the CL-GD7542 generates all the clocks needed for the memory timing (RAS#, CAS#, etc.), as well as the video clock timing. To derive these internal clock signals, an external reference clock must be provided to the OSC input of the CL-GD7542. For all calculations in this document, the external reference clock used is 14.31818 MHz ± 0.01% with a duty cycle of 50 ± 10%.

A7.2 Memory Clock

Memory Clock (MCLK) is used to generate all of the memory timing signals (RAS#, CAS#, etc.).

A7.2.1 Default Memory Clock (MCLK)

The CL-GD7542 default memory clock frequency is 44.744 MHz. For the equation in the next section, this frequency is equivalent to 19h (25 decimal). For information regarding the CL-GD7542's configuration, refer to Appendix A14.

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A7.2.2 MCLK Programming

The CL-GD7542 has a programmable memory clock for higher performance. The desired MCLK frequency is programmed directly into SR1F[5:0], by using the equation below. The MCLK selected at system reset(19h) is valid until SR1F is written.

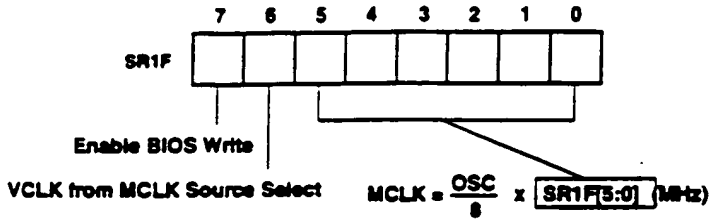


Figure A7.–1. Programmable Memory Clock

Examples of valid MCLK frequencies are shown in following table:

Table A7–1. Examples of Valid MCLK Frequencies

SR1F[5:0] (Decimal))	SR1F[5:0] (hex)	MCLK Frequency (MHz)
21	15h	37.585
23	17h	41.165
25	19h	44.744
28	1Ch	50.114

A7.3 Video Clock

The video clock (VCLK) is the fundamental video timing clock in the system. The CRT monitor timing signals (HSYNC and VSYNC) as well as the LCD clocks are derived from VCLK.

A7.3.1 Default Video Clock Source

The VCLK source is determined by a number of factors, as indicated in Table A7-2. MCLK or MCLK/2 (one half the frequency of MCLK) as well as four VCLKs can be used as a default VCLK.:

Table A7-2. VCLK Sources and Frequencies

SR1F[6]	SR1E[0]	MISC Register 3C2[3:2]	Video Clock (Defaults)	
			Source	Frequency (MHz)
0	x	00	VCLK0	25.180
0	x	01	VCLK1	28.325
0	x	10	VCLK2	41.165
0	x	11	VCLK3	36.082
1	0	xx	MCLK	42.955
1	1	xx	MCLK/2	21.477

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A7.3.2 VCLK Programming

The four internal VCLK sources can be programmed with two registers each, as indicated in the following table.

Table A7–3. Internal VCLK Sources

Video Clock Source	Default Frequency (MHz)	Numerator			Denominator			Post-Scalar
		Register	Dec.	Hex	Register	Dec.	Hex	
VCLK0	25.180	SRB[6:0]	102	66h	SR1B[5:1]	29	3Bh	1
VCLK1	28.325	SRC[6:0]	91	5Bh	SR1C[5:1]	23	2Fh	1
VCLK2	41.165	SRD[6:0]	69	45h	SR1D[5:1]	24	30h	0
VCLK3	36.082	SRE[6:0]	126	7Eh	SR1E[5:1]	25	19h	1

For each VCLK, a 7-bit numerator (N), 5-bit denominator (D), and 1-bit post scalar (P) determines its frequency according to the equation shown in the following figure:

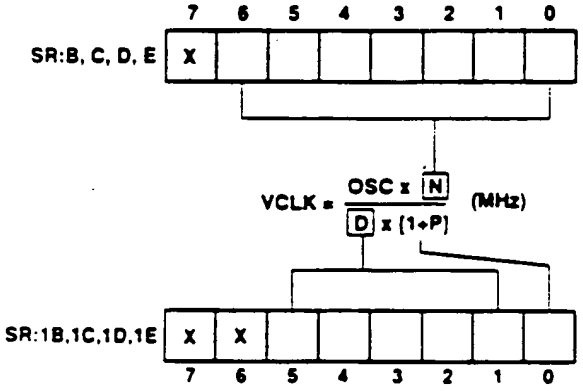


Figure A7–2. Programmable Video Clock

Typically a large number of numerator/denominator values will program a common frequency. The choice among these combinations is made empirically. Generally, better results will be obtained if the post-scalar is programmed to 1

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A7.4 Using MCLK as VCLK

When MCLK and VCLK are programmed to frequencies very close to each other (within about 1%), or to frequencies that are nearly multiples of each other, they may interfere with each other. This interference can show up as 'jitter' on the screen. The solution is to shut down the VCLK Oscillator and use MCLK (or MCLK/2) as VCLK. The following table shows examples of frequencies for which this solution should be used.

Table A7–4. Memory Clock Used as Video Clock

MCLK	Video Mode	VCLK		Selection Criteria		
		Frequency	Source	SR1F[5:0]	SR1F[6]	SR1E[0]
50.1	64, 66 at 60 Hz	25 MHz	MCLK/2	1Ch	'1'	'1'
50.1	58, 5C at 72 Hz	50 MHz	MCLK	1Ch	'1'	'0'

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Appendix A8

Dynamic Video Overlay

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A8. Dynamic Video Overlay

A8.1 Introduction

The CL-GD7542 supports the dynamic video overlay modes, in which the video data from the feature connector pixel data bus (Pixel Bus) is overlaid on a pixel-by-pixel basis. The dynamic video overlay modes are intended to be used when the CL-GD7542 is in Video Mode 5F (640 x 480 x 256 colors). Other 256-color modes may be used as limited by dot clock.

A8.2 Dynamic Video Overlay Features

The CL-GD7542's dynamic video overlay has the following functions:

- VESA pass-through when the FCEVIDEO# pin is driven low
- On-chip Window timing generator
- Dynamic video overlay with Color Key and OVWR#

The CL-GD7542 supports the standard VESA pass-through function, during which the FCEVIDEO# pin is statically driven low and the video is driven into the Pixel Bus. The entire frame is overlaid, and the contents of display memory are ignored. While this function is on, the CL-GD7542 supports only 8-bit-per-pixel data.

In the dynamic video overlay configurations, the video from display memory can be overlaid on a pixel-by-pixel basis. This feature makes it possible to overlay a portion of the frame and mix the VGA video with externally generated video. The term 'dynamic' applies because both the video source and the choice of pixels to be overlaid can be changed dynamically.

In large part, the dynamic video overlay is made possible by driving the Pixel Bus input pins to the valid CMOS levels, and taking video from them to the DAC only when desired. This action eliminates the bus exchange time. The CL-GD7542 supports the dynamic video overlay, but it has some restrictions regarding the Color Key feature.

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A8.3 Overview Of Dynamic Video Overlay

The Dynamic Video Overlay Modes are intended to be used when the CL-GD7542 is in video mode 5F (640 x 480 x 256 colors). Other 256-color Modes may be used as limited by dot clock. The Dynamic Overlay Modes are chosen by programming the CR1A[3:2] field according to the following table:

Table A8-1. Dynamic Video Overlay Modes

CR1A		Mode
[3]	[2]	
0	0	VGA-compatible Operation
0	1	Dynamic Video Overlay with FCEVIDEO#
1	0	Dynamic Video with OVWR# and Color Key
1	1	Dynamic Video Overlay with Color Key

The video data that is introduced into the Pixel Bus is assumed to be 5-5-5 Sierra™ or 5-6-5 XGA™ format according to the value of the Hidden DAC Register. These formats are the only ones allowed. Refer toTable A8-2. Clocking Mode 1 must be used.

NOTES: Clocking Mode 1 can be chosen by setting HDR[5] to a 0. In Clocking Mode 1, 16-bit/pixel modes will use both edges of FCDCLK to latch data: The rising edge will latch the least significant byte. The falling edge will latch the most significant byte.

Table A8-2. External Video Format

External Video Format	Hidden DAC Register Value
5-5-5	100XXXX 110X0000
5-6-5	110X0001

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A8.4 Dynamic Video Overlay With FCEVIDEO#

When the CR1A[3:2] field is programmed to 01, the Dynamic Video Overlay with FCEVIDEO# is chosen. The Pixel Bus is switched to inputs: An external video generator must always drive the bus to guarantee valid CMOS levels, even when the inputs are being ignored. Each pixel for which FCEVIDEO# is low will be taken from the Pixel Bus. There is no requirement that the pixels to be overlaid be contiguous (adjacent), either horizontally or vertically.

The following timing diagram shows the FCEVIDEO# setup and hold times that must be met with respect to FCDCLK. FCEVIDEO# has a setup and hold time requirement to guarantee both that the desired pixel will be overlaid and the adjacent pixels will not be overlaid. In addition, there is a data setup and hold requirement for both edges of FCDCLK (the DAC is in Clocking Mode 1). The rising edge of FCDCLK will clock the least-significant byte of the pixel. The falling edge of FCDCLK will clock the most-significant byte.

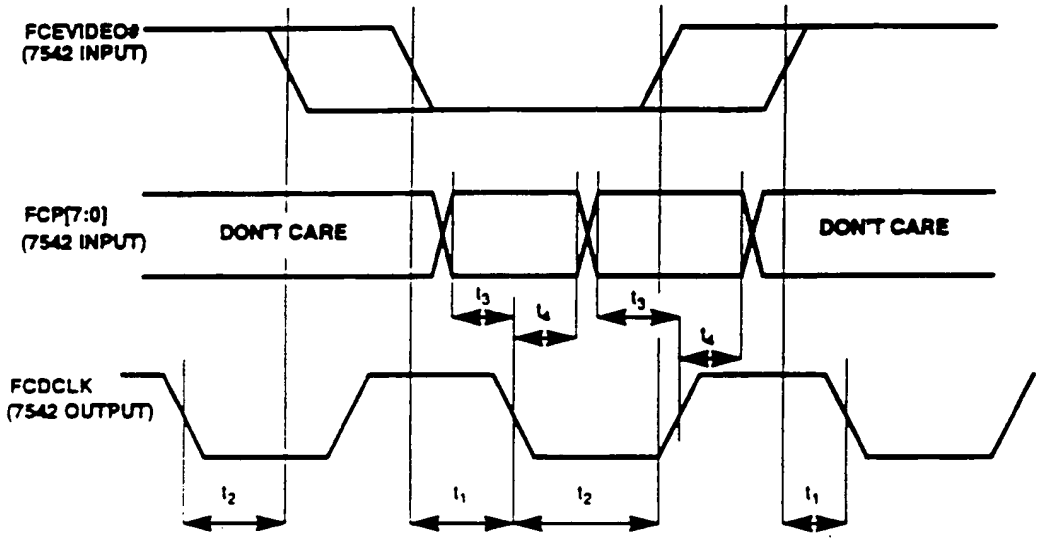


Figure A8–1. FCEVIDEO# Setup and Hold Times

NOTES:
t_1: Command Setup to Clock
t_2: Command Hold from Clock
t_3: Data Setup to Clock
t_4: Data Hold from Clock

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The following pseudo-code fragment shows the registers that must be programmed:

```
Call WriteDACMode(0xC1)     'Choose 5-6-5 Mode Video (for example)
Call SetReg(CR1A,0x04)      'Overlay with FCEVIDEO#
```

Once these two registers have been programmed, each pixel either will or will not be overlaid according to the state of FCEVIDEO#

A8.5 On-chip Window Timing Generator

The CL-GD7542 contains logic to generate a single rectangular window. If this mode is enabled, the window timing comes out on OVWR#, which may be fed back into FCEVIDEO#: The chip specifies its own window.

This mode is chosen by programming CR1B[5] to a 1. When this bit is set, the blanking term to the palette DAC comes from the internal display enable signal, and there is no border. In turn, this action frees the Blank Generator Logic, which is used as a window generator.

The following timing diagram shows how the Blanking Start and Blanking End Registers are used to specify either the horizontal or vertical component of the window. The Horizontal Blanking End field is extended to eight bits and the Vertical Blanking End is extended to 10 bits.

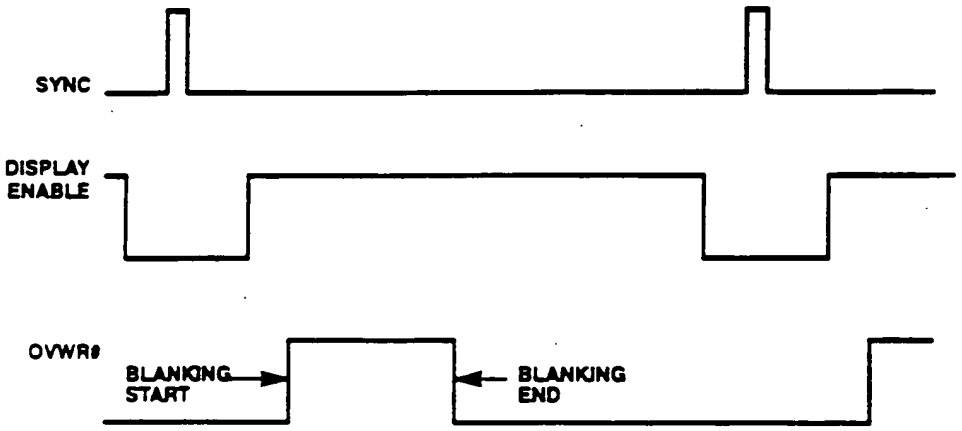


Figure A8–2. Usage of Blanking Start and Blanking End Registers

When the vertical timing and the horizontal timing thus generated coincide, OVWR# will be driven low indicating the window. OVWR# may be connected directly to FCEVIDEO# if CR1A[3,2] = 11 (dynamic video overlay mode with color key only) is never going to be chosen. If CR1A[3,2] = 10 (dynamic video overlay mode with color key and OVWR#), OVWR# must be driven into FCEVIDEO# with an external three-state buffer to avoid a potential bus collision.

This method of generating timing has four restrictions that require consideration.

- There can be no border, because the blank timing generation logic is used for window generation. This restriction is inconsequential since the VESA timing specifications do not include a border.
- The resolution of the horizontal component of the window is 8 pixels, since the Horizontal Counters operate on an 8-pixel character clock. This restriction can be overcome at least in part by using FCEVIDEO# and color key overlay, as discussed later.
- There can be only a single window and it must be rectangular.

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- The first or third scanline or group of pixels can be chosen as a window boundary, but not the second scanline.

For dynamic programming of the blank registers, eight registers must be programmed to set up all four blank parameters, five of which contain bits related to other functions. The following table shows the registers that are involved:

Table A8–4. Dynamic Programming of Blank Registers

Register	Bits	Parameter
CR2	[7:0]	Horizontal Blanking Start [7:0]
CR3	[4:0]	Horizontal Blanking End [4:0]
CR5	[7]	Horizontal Blanking End [5]
CR7	[3]	Vertical Blanking Start [8]
CR9	[5]	Vertical Blanking Start [9]
CR15	[7:0]	Vertical Blanking Start [7:0]
CR16	[7:0]	Vertical Blanking End [7:0]
CR1A	[7:6]	Vertical Blanking End [9:8]
CR1A	[5:4]	Horizontal Blanking End [7:6]

All the following general scheme is used to dynamically move and resize the window.

- Obtain copies of the registers containing bits used for other functions (CR3, CR5, CR7, CR9, CR1A), and force the blank control bits to zeroes. These values are saved and used as templates in the first of two activities. This activity accepts the window co-ordinates and returns the value for each register. This routine must isolate and align each field as indicated in the table above, and then merge it with the template that was previously saved.
- Accept the values for all eight registers and load them into the hardware. This activity should be synchronized with vertical retrace.

A8.6 Dynamic Video Overlay With Color Key

Dynamic video overlay with color key is chosen when the CR1A[3:2] field is programmed to 11. In this mode, the window timing is controlled strictly by the contents of display memory. If a pixel matches the contents of the Color Key Register, it will be replaced with the video from the Pixel Bus. FCEVIDEO# is a normally a low output in this mode, that goes high for one FCVCLK period before a pixel is replaced. If multiple contiguous pixels are to be replaced, FCEVIDEO# will remain high appropriately.

GRC, the Color Key Compare Register, contains the color key which is compared with the pixel from display memory.

The following pseudo-code fragment shows the registers that must be programmed to configure the CL-GD7542 for Dynamic Video Overlay with Color Key:

```
Call WriteDACMode(0xC1)     'Choose 5-6-5 Mode Video(for example)
Call SetReg(CR1A,0x0C)      'Overlay with FCEVIDEO#
Call SetReg(GRC,ColorKey)   'Set up the Key
Call SetReg(GRD,KeyMask)    'and the mask
```

Once the CL-GD7542 has been programmed into this mode, the Pixel Bus bits are the inputs and must be driven by an external video generator to guarantee valid CMOS levels, even during those periods for which the Input Video will not be used. The Pixel Bus does not have internal pull-ups.

FCEVIDEO# may be used by an external video generator to determine when the first pixel of the window is about to occur. This would be useful if the external video is to be positioned with respect to a rectangular window, rather with respect to the frame. The following diagram shows the timing of FCEVIDEO# and the required timing for the video.

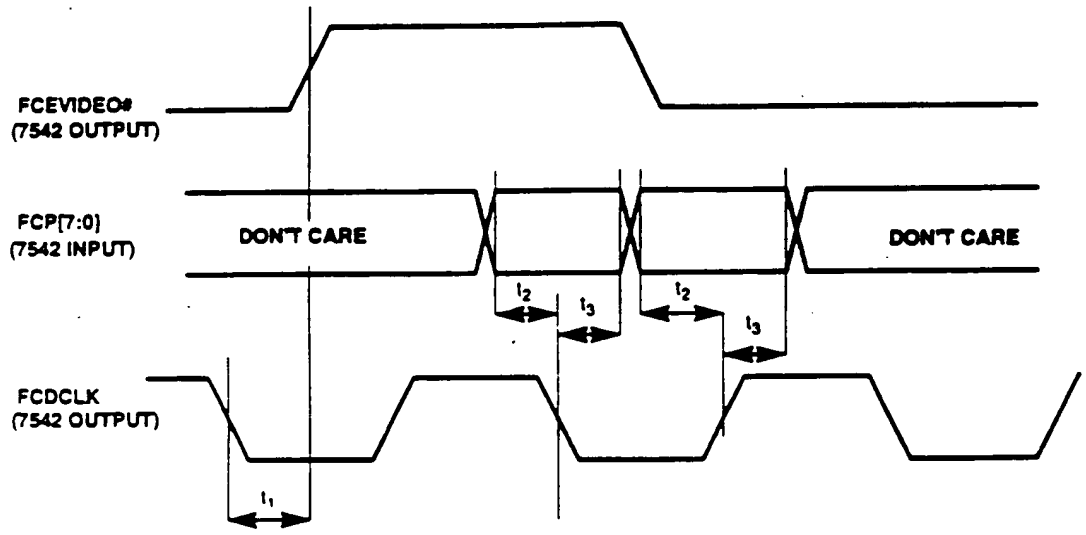


Figure A8–3. External Video Timing

NOTES:

t_1 FCDCLK to FCEVIDEO# Propagation Delay

t_2 Data Setup to FCDCLK

t_3 Data Hold from FCDCLK

A8.7 Dynamic Video Overlay with Color Key And OVWR#

Dynamic Video Overlay with Color Key and OVWR# is chosen when the CR1A[3:2] field is programmed to 10. The window time is the result of the logical AND of the Color Key Comparison and OVWR# being active. In this mode, FCEVIDEO# is an input and will be active for pixels that will be overlaid. This mode is intended to restrict the Color Key effect to a specified area.

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SPECIFICATION

Revision 1.4

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1 DOCUMENTATION / CHIP REVISION

Revision Date	Description
Rev 1.0 11/20/92	Initial Released
Rev 1.1 2/26/93	Second Released. Too many changes to document.
Rev 1.2 7/9/93	New features: ➢ Power Management feature compliant to DPMS ➢ VAFC compliant ➢ VMC compliant for future revision or version
Rev 1.3 8/26/93	Changes: ➢ Section 4.4, change to 'data is connected to BD[7:0]' ➢ Section 4.8, added and expanded description of the input/output ports for Multimedia; added more details of the implementation ➢ Section 6 - refer to rev history for Section 6.
Rev 1.4 10/18/93	Changes: ➢ Section 2.0, changed features ➢ Added section 4.9 or I^2C & Auxiliary I/O support ➢ Section 5.x, changed pin out from 208 to 240 ➢ Section 6 - refer to rev history for Section 6

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2 FEATURES

- 32-bit direct PCI & VL interface & 16-bit direct ISA interface
- Bus master mode on PCI
  - Supports direct burst read from system memory for faster memory to screen transfer
  - Supports direct write to system memory for faster screen to memory transfer
- Drawing engine
  - True 64-bit datapath
  - BitBlt engine with color expansion/conversion and clipping
  - Supports four independent bitmaps - destination, source, pattern and mask
  - Supports WINDOWS NT/4.0 *quaternary ROP's* and WINDOWS 3.x *ternary ROP's*
  - Line drawing
  - Area fills
  - CPU assisted drawing mode
  - 1,8, 16, & 32 bpp
- Hardware Cursor (64x64, 2bpp, 16M color) using off-screen.
- 8,16, 24-bit pixel data bus
  - Multiple pixels packing allowing higher resolution /color depth modes to run at slower VCLK
- Write cache/queue
  - Write cache for VGA path
  - Write queue for co-processor path
- Linea address mapping above 1MB up to 4G on VL and PCI, up to 16M on ISA
- Memory mapped I/O for Co-processor
- Maximum 110Mhz dot clock rate, 66MHz memory clock rate
- Maximum resolution 1280 x 1024 256 colors (non-interlace)
- 32K/64K colors at 640x480, 800x600, and 1024x768
- 16M colors at 640x480, 800x600, 1024x768
- Video buffer size up to 8MB
- Flexible memory support
  - Support for 256KxXX, 64Kx16, 512Kx8 & 1024Kx4 DRAM's, in 32 or 64 bit bus configuration
  - Programmable memory timing
- EEPROM support for switchless implementation
- Integrated Feature Connector support compliant to VESA VAFC Proposal 1.0p
- Multimedia Support
  - 16-bit input port for live video (will be compatible with VESA Media Bus in revision B)
  - Input scaling (output scaling can will be supported in revision B)
  - Mask map for input video to allow color keying with simple DAC.
  - Control video windowing
  - Allow Video DAC to share memory bus for video port
- Power saving modes compliant to VESA DPMS Proposal 1.0p
- I²C & address decode/data routing for other auxiliary parts in subsystem
- 240 pin PQFP

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3 PIT-FALLS

- IBM VGA text modes, i.e. DOS applications, will be slower than S3's 805, ET4000/W32 because of single memory address bus
- Support DRAM only will project "Low Performance Image" and cannot compete with VRAM performance
- Registers not compatible with OTI-087, OTI-077, OTI-067 or OTI-037
- Master mode will require different set of drivers and may not work
- Inconsistencies across platforms (VL, PCI, ISA)
  - 24-bit pixel data interface not supported on VL bus
  - Master mode not supported on ISA and VL
  - 16-bit BIOS is not supported on VL & PCI
  - Auxiliary I/O space supported on VL bus requires more external logic
  - Does not support vertical zooming of the Bt885 on VL bus
- Not backward compatible with EGA, CGA & Hercules
- No plug & play for ISA, VL
- Can not write to BIOS EEPROM (could be a desirable feature for OEM)
- 4bpp is dropped from the co-processor.
- 32bpp co-processor can only be used at lower resolution due to bandwidth limitation
- Not so glueless interface for basic VGA add-on board
  - ISA - needs 1 inverter for RESET
  - VL - needs a LS10 & a LS245 to support DAC & BIOS ROM, needs a LS244 to support auto-configuration from VL's ID bits.
- Co-processor features that may not work:
  - Mask Map - arbitrary masking
  - 16bpp, 32bpp
  - Line drawing - short stroke vectors
  - BitBlt - reverse bliting
  - CPU assisted BitBlit - more than 2 maps operation
- 66 MHz MCLK may not work over production range.

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4 INTERFACE DESCRIPTION

The OTI-107 has the following major interfaces to the outside world

1. System bus interface
2. DAC interface
3. Clock interface
4. ROM BIOS interface
5. Feature connector interface
6. EEPROM/Dipswitch interface
7. Display memory interface
8. Multimedia interface
9. I^2C & other components in subsystem
10. Monitor interface and DPMS.

4.1 System Bus Interface

The OTI-107 can be configured to interface directly to three standard system buses: VL, PCI and ISA. The chip configures itself to interface to a particular bus during hardware reset through Hardware Configuration Register 1 The VL interface is compliant to the VESA VL-Bus Specification Version 2.0p, Revision 0.93p, dated 9/23/1993. The PCI interface is compliant to the PCI Local Bus Specification Revision 2.0, dated 4/30/1993. The ISA interface is compatible to the IEEE P996 standard for 8-bit and 16-bit ISA bus.

4.1.1 VL Bus

OTI-107 supports both I/O and memory cycles on VL bus up to 50MHz. I/O cycles are minimally 1 wait states and programmable up to 5 wait states. Memory write cycles are designed to run at 0-2 wait states on cache hit cycles, depending the speed of the bus. Strictly following VL bus specification of 4ns setup time for address and data would force the controller to run at a minimum of 1 wait. Memory mapped I/O write cycles are minimally 1 wait state and programmable up to 5 wait states, while memory mapped I/O read cycles are minimally 2 wait states and programmable up to 6 wait states. General rule of thumb, the memory write cycles are zero wait at 25MHz bus speed, and 1 wait at 33-50MHz.

32-bit I/O is supported for Extended System Interface registers (2xxx). Standard VGA and Oak Extended registers at 3DE/3DF can only be supported with word or byte cycles. DAC and Auxiliary registers can only be supported with byte cycle. BIOS and drivers must take care of this.

OTI-107 does not support Bus Mastering or burst mode.

See VESA VL-Bus Specification for more operational information on VL bus.

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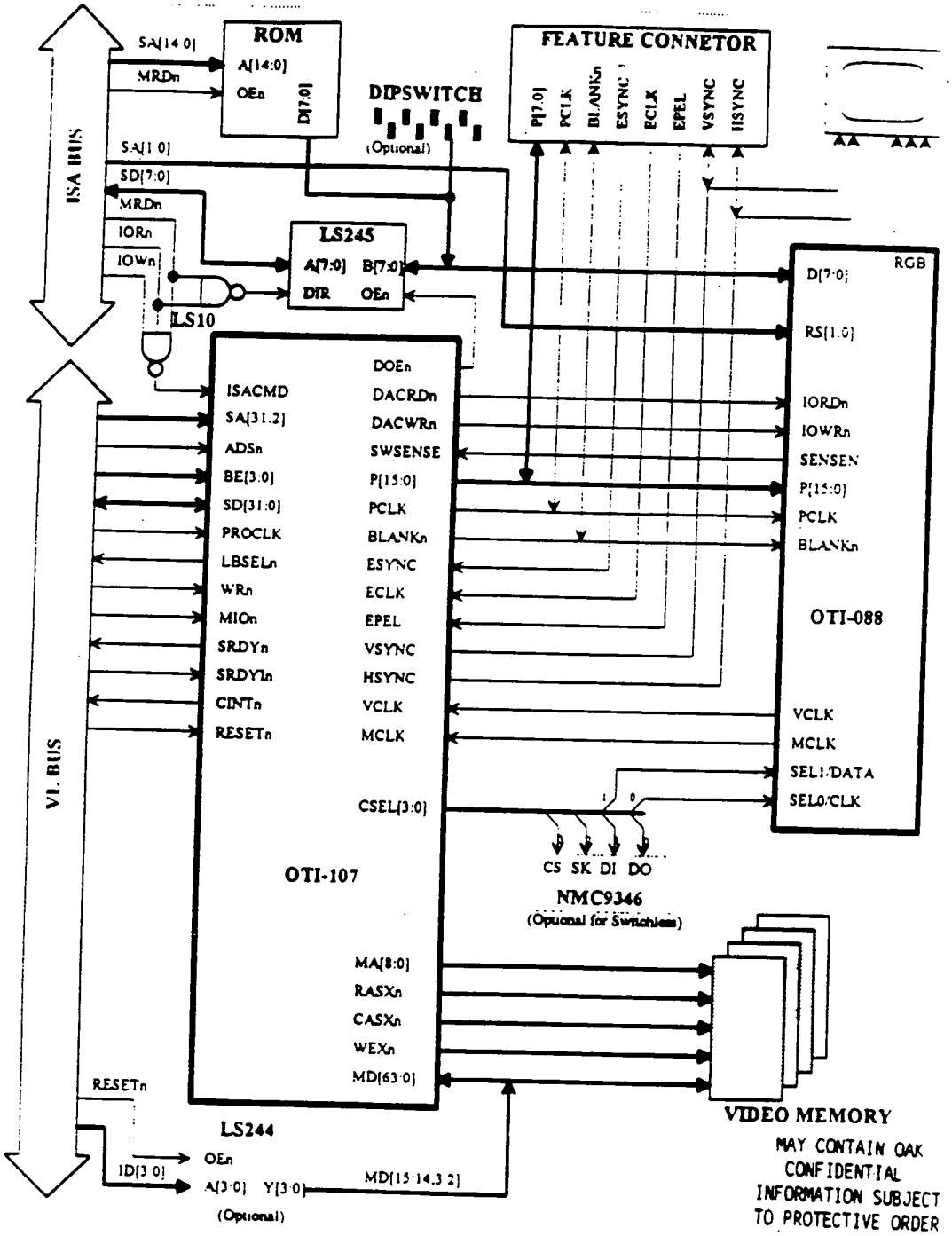


Figure 4.1 - VL Bus Block Diagram

4.1.2 PCI Bus

Only 32-bit PCI bus is supported. 64-bit extension is not supported. PCI bus can be supported up to 33MHz. I/O and Configuration cycles are minimally 1 wait states and programmable up to 5 wait states. Memory cycles, both read and write, are minimally 1 wait state and maximally three wait states. Memory mapped I/O write cycles are minimally 1 wait state and programmable up to 5 wait states, while memory mapped I/O read cycles are minimally 2 wait states and programmable up to 6 wait states.

32-bit I/O is supported for Extended System Interface registers (2xxx). Standard VGA and Oak Extended registers at 3DE-3DF can only be supported with word or byte cycles. DAC and Auxiliary registers can only be supported with byte cycle. BIOS and drivers must take care of this.

Bus mastering and burst mode are supported for PCI bus. However, physical memory must be used in order to use master mode. Parity generation is supported but there is no parity checking.

See PCI Local Bus Specification (Rev 2.0) for more details.

4.1.3 ISA Bus

The OTI-107 provides 0 wait state memory operations and 1 wait I/O on ISA bus up to 12.5MHz. Faster bus systems should disable 0 wait state feature. DAC and Auxiliary registers can only be supported with byte cycle. IO16n will not be generated for these cycles.

Bus Mastering is not supported.

4.2 DAC Interface

DAC I/O is assumed to be 8-bit transfer only. For ISA or PCI bus implementation, DAC system data is routed through BD bus to the system bus. For VL bus implementation, DAC system data is routed to the ISA bus through external buffers. OTI-107 will always decode address and status/command to generate DACRDn and DACWRn for the DAC I/O commands. DAC address space is default to 3C6-3C9. Extended DAC I/O space can be supported from 2x80-2x9F. The 'x' is programmable and default to 1. See system block diagrams for more information.

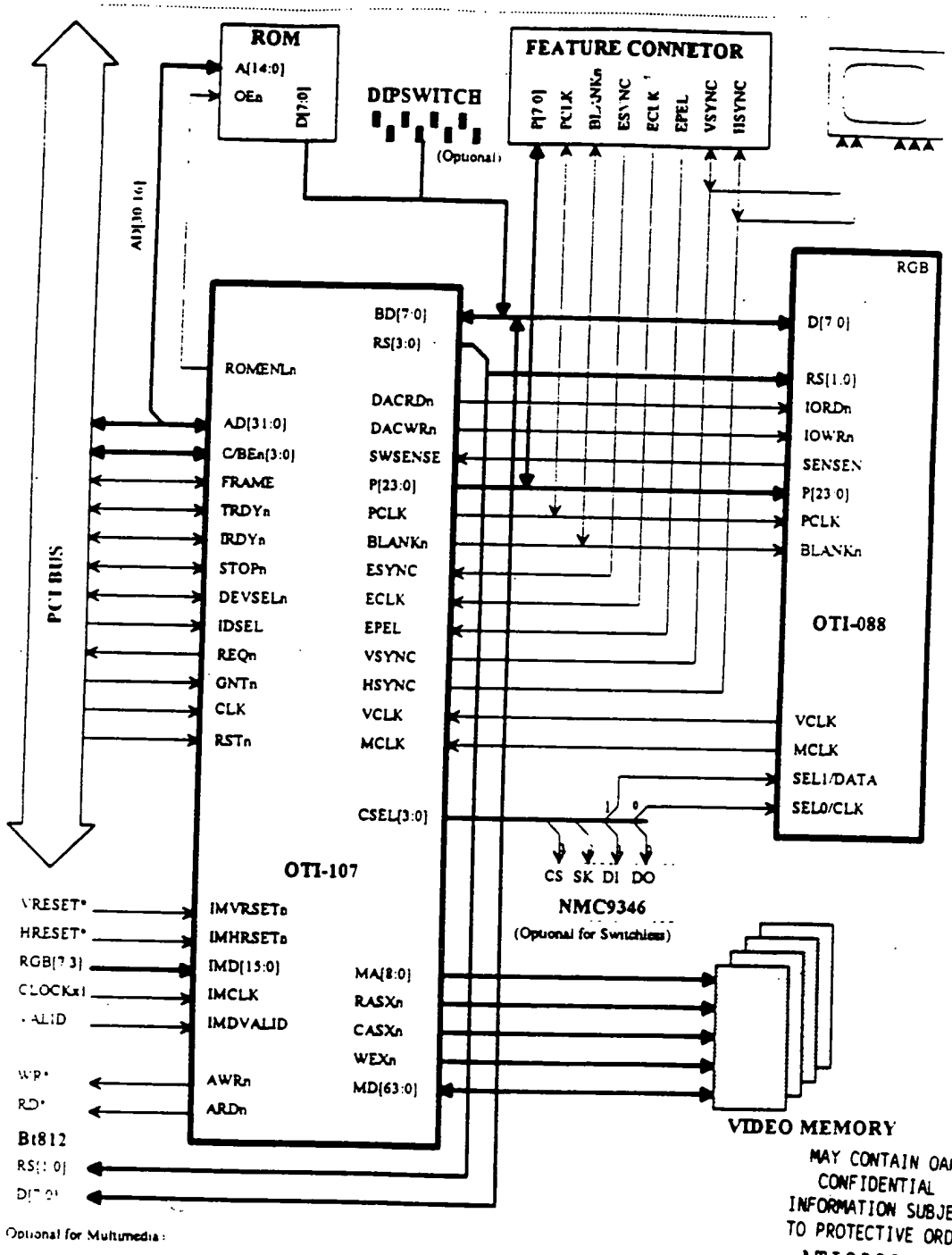
OTI-107 can be configured to be either 8, 16 or 24-bit pixel bus support. Hi-color and true-color support in 8-bit configuration is the same as 87X (double or triple frequency). Hi-color support in 16-bit pixel bus will allow the controller to run at regular frequency instead of doubling. True-color support in 16-bit pixel bus will require doubling frequency (with one byte wasted or with packed format), but not tripling the frequency. For high resolution (1280x1024) 256 color modes, there is an option to send the 16-bit pixel data out at a time and the pixel clock can be half the regular frequency.

24-bit pixel bus is supported for true color modes only. Due to pin limitation on VL bus, pins P[23:16] are available only when the OTI-107 is on either ISA or PCI bus. 24-bit pixel bus support allows the OTI-107 to support true color at higher resolution without having to double or triple the pixel clock frequency.

See Pixel Interface register for more information on various modes supported at different pixel bus width.

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Figure 4.2 - PCI Bus Block Diagram w/ Live Video Option

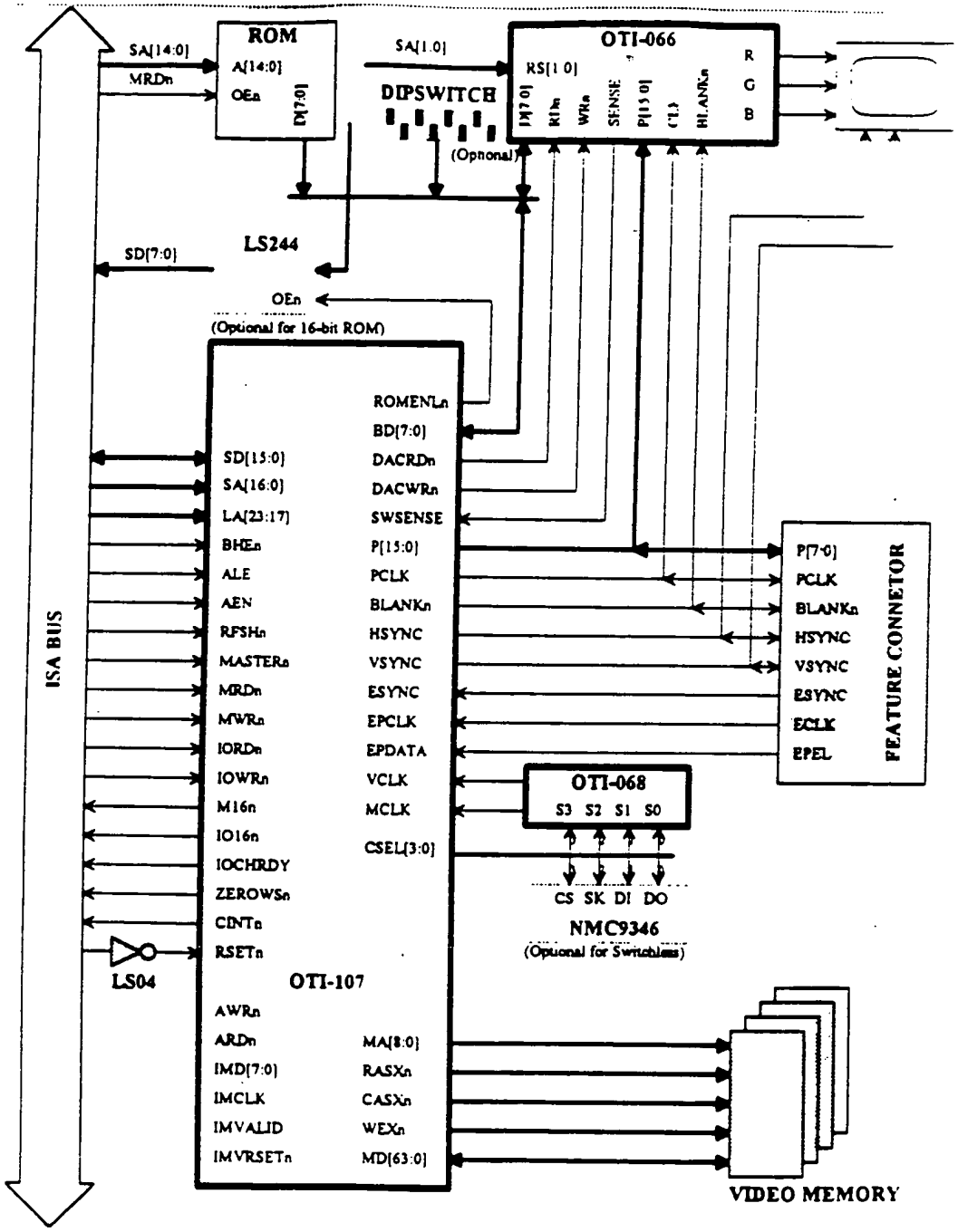


Figure 4.3 - ISA Bus Block Diagram

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4.3 Clock Interface

Up to 16 external video clock frequencies can be selected by four programmable clock select pins. Video clock frequencies can be supported up to 110MHz. These programmable pins can also be used as clock and data pins for serially programmable clock sources, allowing the OTI-107 to support both VESA and conventional video frequencies without any hardware switches.

Memory clock is selectable through either software if the clock chip is programmable, or by hardware through jumpers if the clock chip has fix frequencies. Memory clock can be supported up to 66MHz.

4.4 ROM BIOS Interface

For ISA bus configuration, the OTI-107 can support either single (8-bit BIOS) or double ROM (16-bit BIOS). The ROM data is routed back to the ISA bus through BD bus and external buffer if two ROM's are used.

For VL bus configuration, only single ROM (8-bit BIOS) and the ROM can only be on the ISA bus. ROM data is routed back to the ISA bus through external buffer.

For PCI bus configuration, only single ROM (8-bit BIOS) can be supported. The ROM address is connected to AD[30:16], while the data is connected to BD[7:0]. During ROM read cycle, the OTI-107 latches the lower system address AD[14:0] to generate internal RA[14:0] and drive them out through AD[30:16], generates ROMENLn as a ROM output enable signal, and toggled the RA[1:0] appropriately depending on whether the current cycle is byte, word or doubleword. If it is word or double word, the OTI-107 toggles the RA[1:0] and latches in the ROM data through AD[7:0] bus, aligns the data, and sends them back out to AD[31:0]. Wait states are automatically asserted for the ROM access, assuming MCLK is 66MHz and the slowest ROM speed is 120ns.

ROM BIOS address space is assumed to be at 'hC0000. ROM BIOS support as described above can be enable or disable through the Hardware Configuration Register 2.

4.5 Feature Connector Interface

The OTI-107 supports feature connector in all configurations. The OTI-107 feature connector support is compliant to the VESA Standard VGA Pass-Through Connector (VSVPC), and it can be compliant to the VESA Advanced Feature Connector (VAFC) with an appropriate DAC/Synthesizer. For VAFC, base line compliant is readily achieved with OTI-107 and any 16-bit pixel port DAC, with clock doubling modes, and 5:6:5 RGB format, such as the OTI-088. To be VAFC compliant in extended modes, a more advanced DAC such as the Bt885 is needed.

Pins EPDATA, EPCLK, and ESYNC are inputs to the chip to enable/disable P[23:0], PCLK, and BLANKn/HSYNC/VSYNC respecuvely. Pins HSYNC & VSYNC now have AC timing requirements with respect to PCLK to meet the VAFC specification.

Although PCLK can operate up to 110MHz, it is not meant to drive the feature connector at this speed. Feature connector operation should be limited to 40MHz or less.

Pin GRDY is currently not generated from the OTI-107, but with an appropriate timing, BLANKn can be used to generate GRDY for the connector.

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4.6 EEPROM/Dipswitch Interface

A small EEPROM (1024x1) can be supported to enable the add-on card or the graphic subsystem to be switchless Because the control pins for the EEPROM interface is muxed with clock select pins, EEPROM should be programmed or read during POST only. See EEPROM Control Register description for more details.

For cost saving purposes, an 8-bit dipswitch can be supported in place of the EEPROM The dipswitch support does not need external buffers. Dipswitch can be read at anytime through extended register 3DF index D

4.7 Display Memory Interface

The OTI-107 supports 64Kx16 DRAM, 256KxXX DRAM, 512Kx8 and 1Mx4 DRAM. The OTI-107 provides all the necessary control signals, address and data lines to access the video memory in fast page mode. The maximum video buffer size is 8M bytes when used with 1Mx4 DRAM's, 4M bytes when used with 512Kx8 or symmetric 256Kx16 DRAM's, 2M when used with 64Kx16, 256Kx4 or asymmetric 256Kx16 DRAM's. Minimum configuration is 256K bytes when used with 64Kx16 DRAM, 1M bytes when used with 256KxXX or 512Kx8 DRAM, and 2M bytes when used with 1Mx4 DRAM.

Support for 256Kx16 includes 10-bit row address, 8-bit column address type as well as 9-bit row, 9-bit column address type. There is an option to convert WExn signals to CASxn signals, and vice versa.

Memory cycles can be programmed to match with different types of DRAM. The RAS precharge and pulse, CAS precharge and pulse width, and RAS-to-CAS delay are all programmable. Matching memory cycles with a programmable memory clock would virtually guaranteed the most efficient memory interface for a given memory type. Memory clock can be supported up to 66MHz.

The video buffer can be addressed through either a programmable linear address range above 1M up to 4G on VL and PCI bus, up to 1.5M on ISA bus, or through the conventional video address (A0000 to BFFFF) with the segment registers. Depending on the type of memory used, and the amount of memory installed, the chip can be configured to have either 32-bit or 64-bit memory data bus. See memory configuration block diagrams for more details

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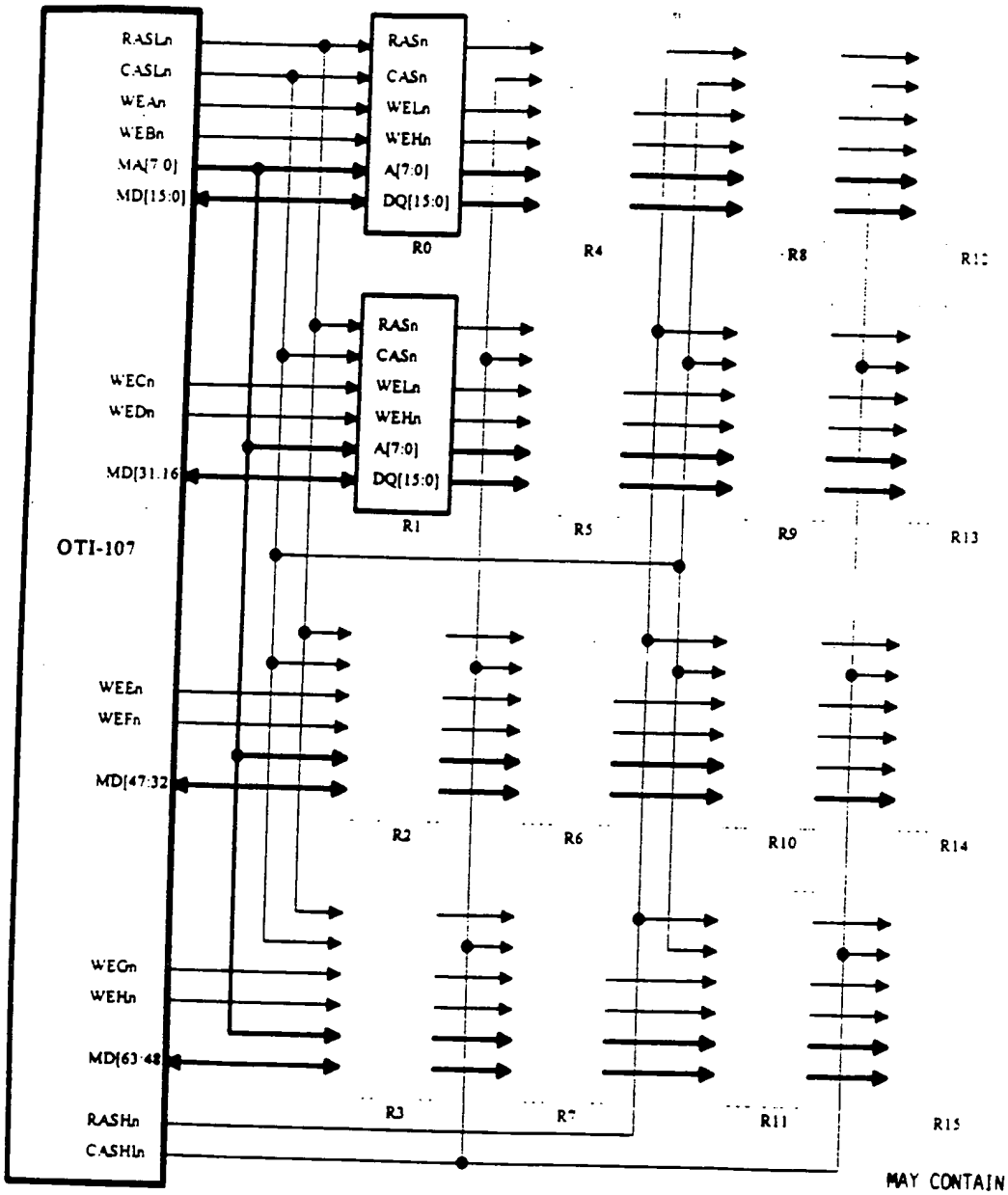
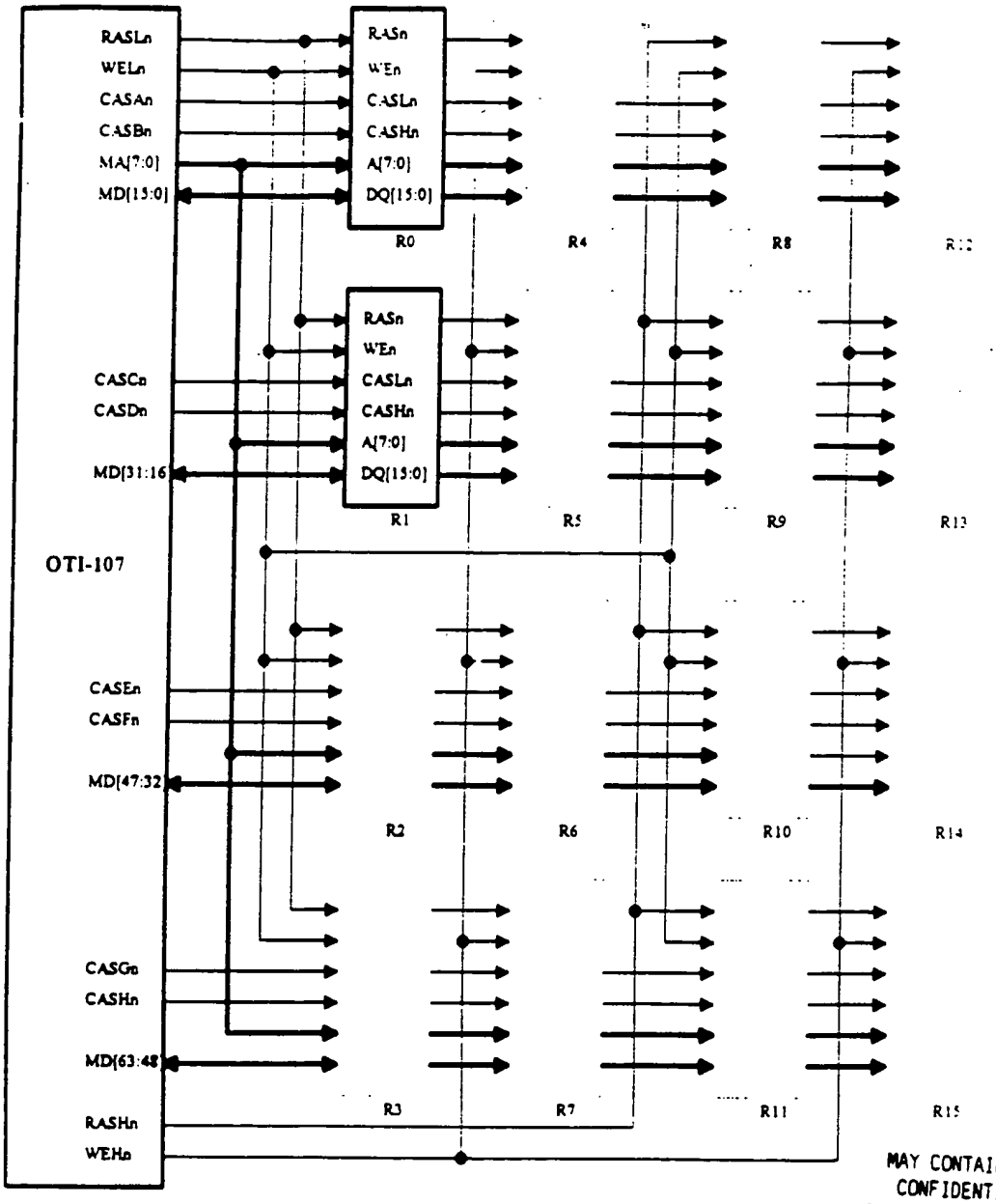


Figure 4.4 - 64Kx16 DRAM's (1 CASn, 2 WEn), MD32 & 64, 256K - 2M bytes

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Figure 4.5 - 64Kx16 DRAM's (2 CASn, 1 WEn), MD32 & 64, 256K - 2M bytes

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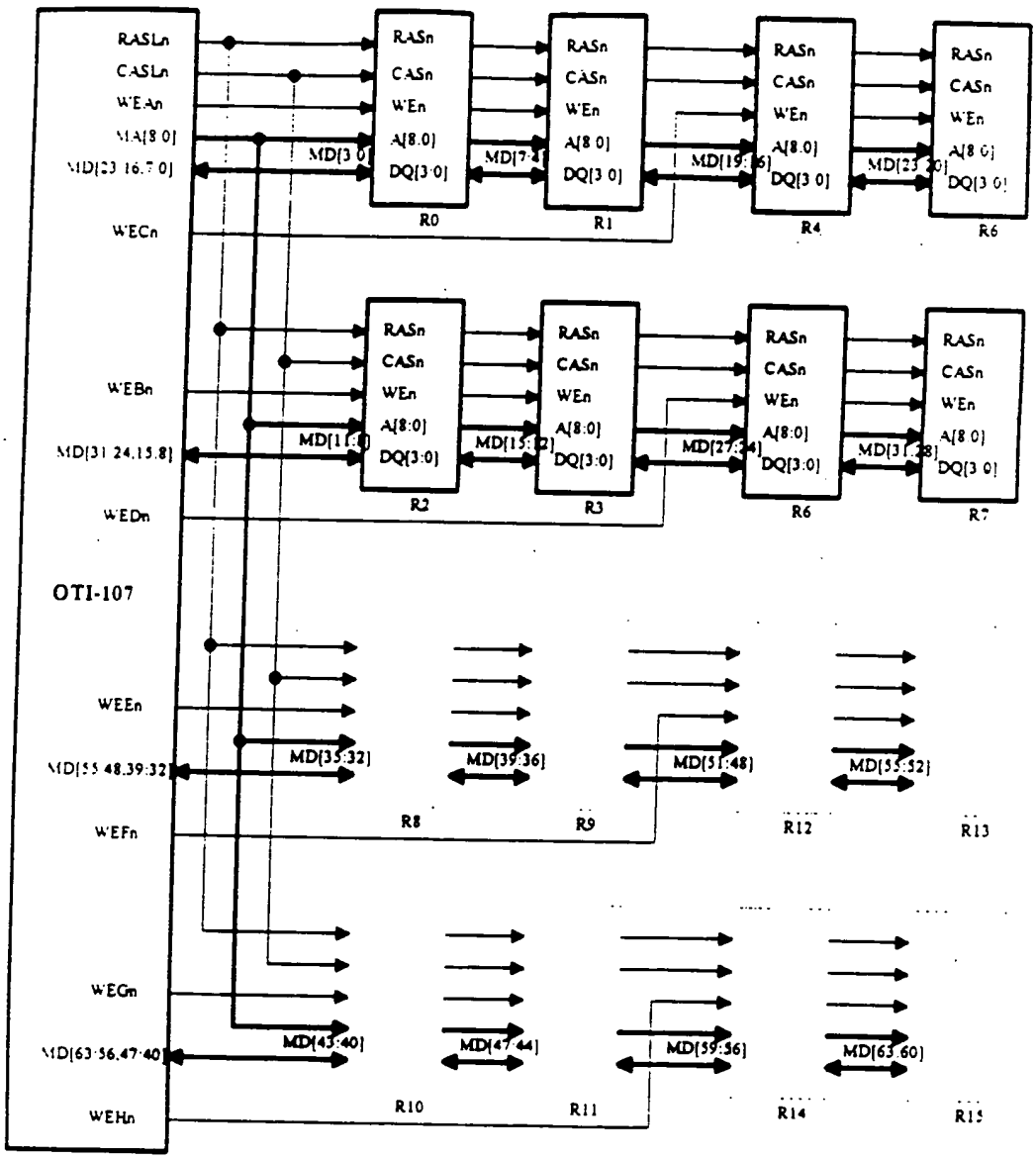
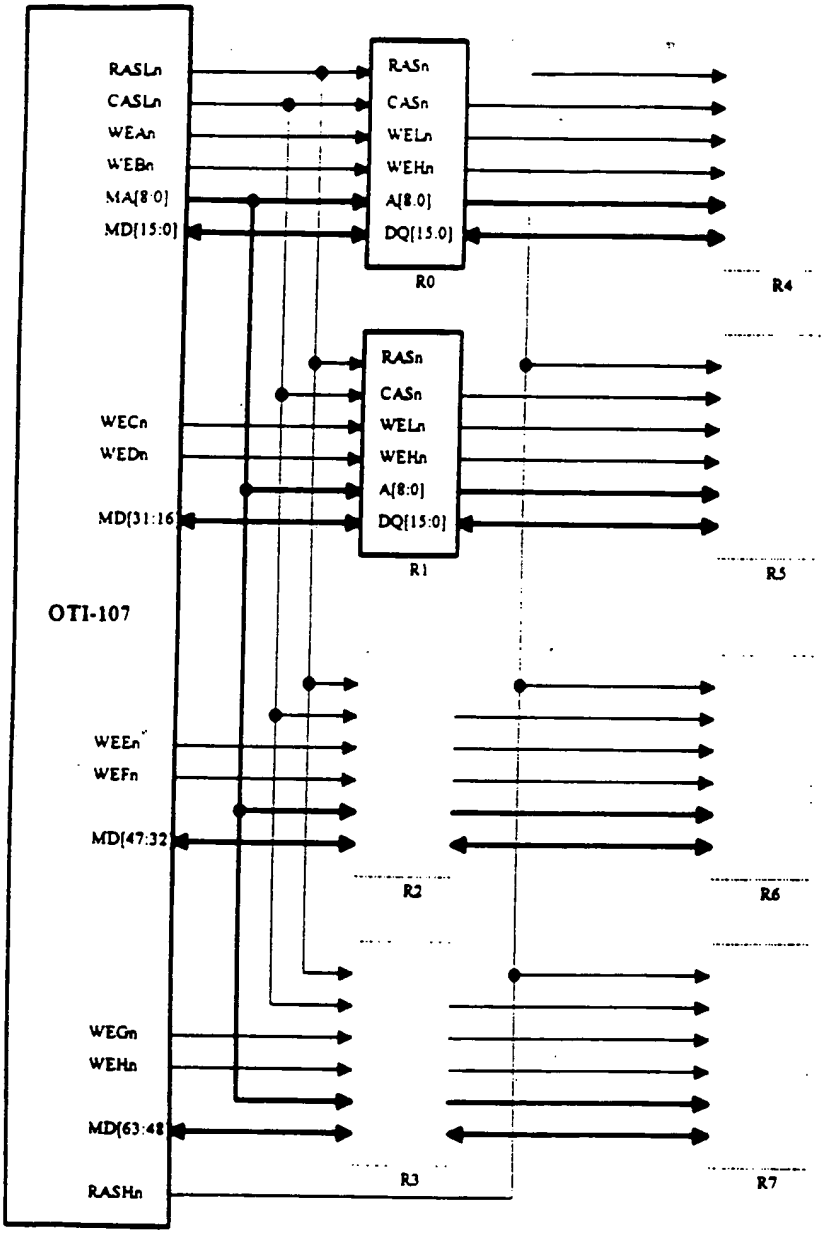


Figure 4.6 - 256Kx4 DRAM's, MD16, 32 & 64, 512K - 2M bytes

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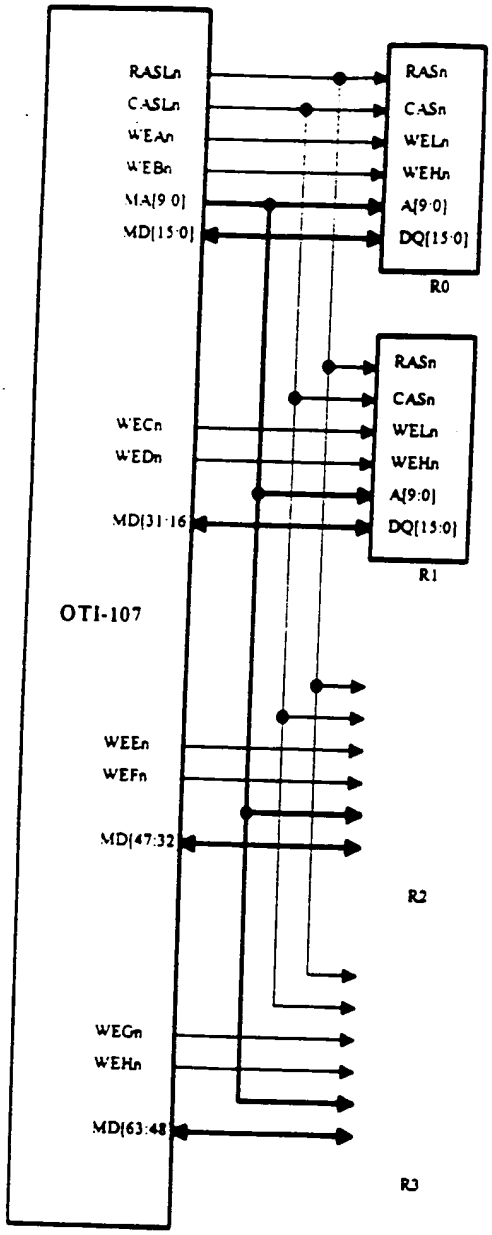
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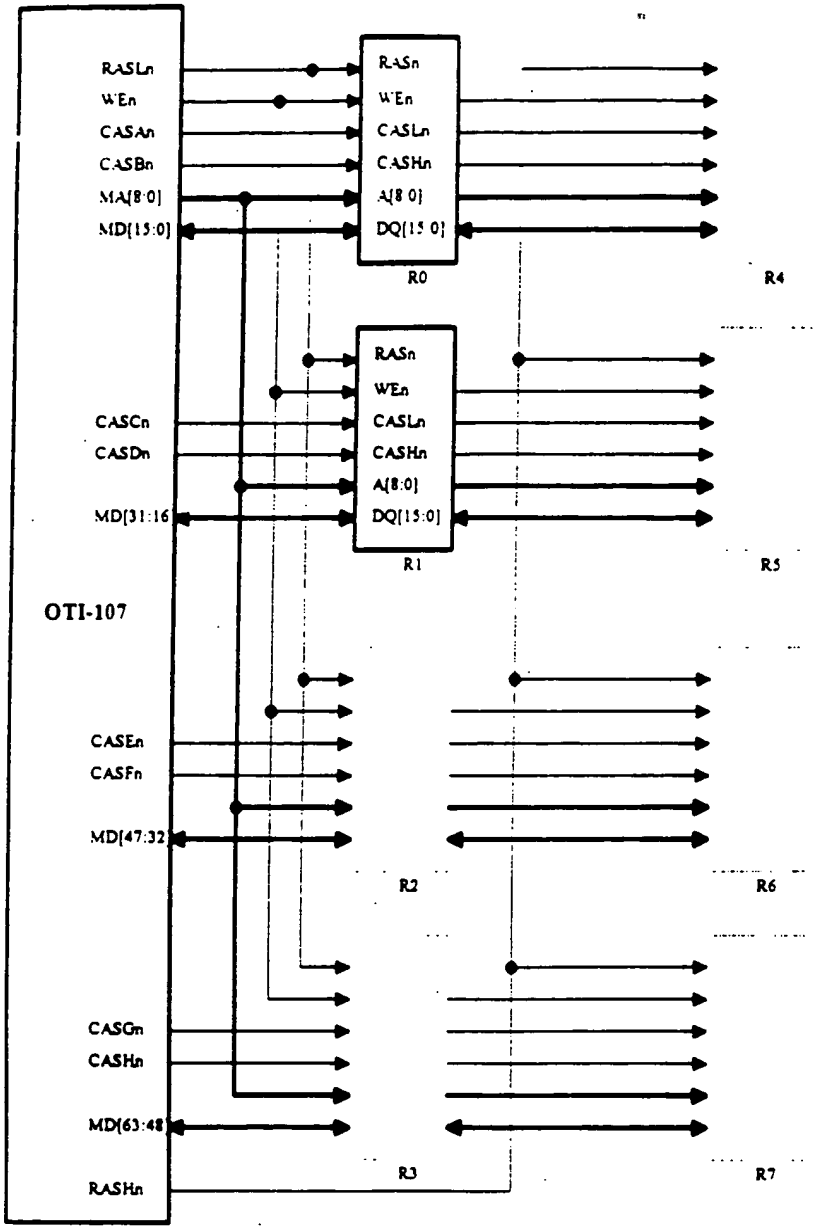
Figure 4.7 - 256Kx16 DRAM's (9x9, 1 CASn, 2 WEn), MD16, 32 & 64, 512K - 4M bytes

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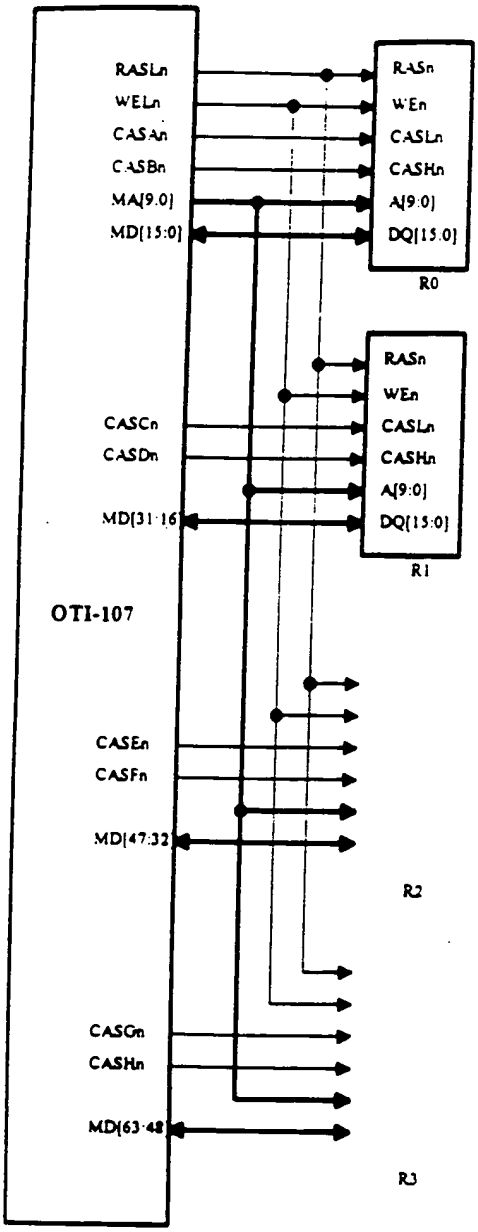
Figure 4.8 - 256Kx16 DRAM's (10x8, 1 CASn, 2 WEn), MD16, 32 & 64, 512K - 2M bytes



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Figure 4.9 - 256Kx16 DRAM's (9x9, 2 CASn, 1 WEn), MD16, 32 & 64, 512K - 4M bytes

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Figure 4.10 - 256Kx16 DRAM's (10x8, 2 CASn, 1 WEn), MD16, 32 & 64, 512K - 4M bytes

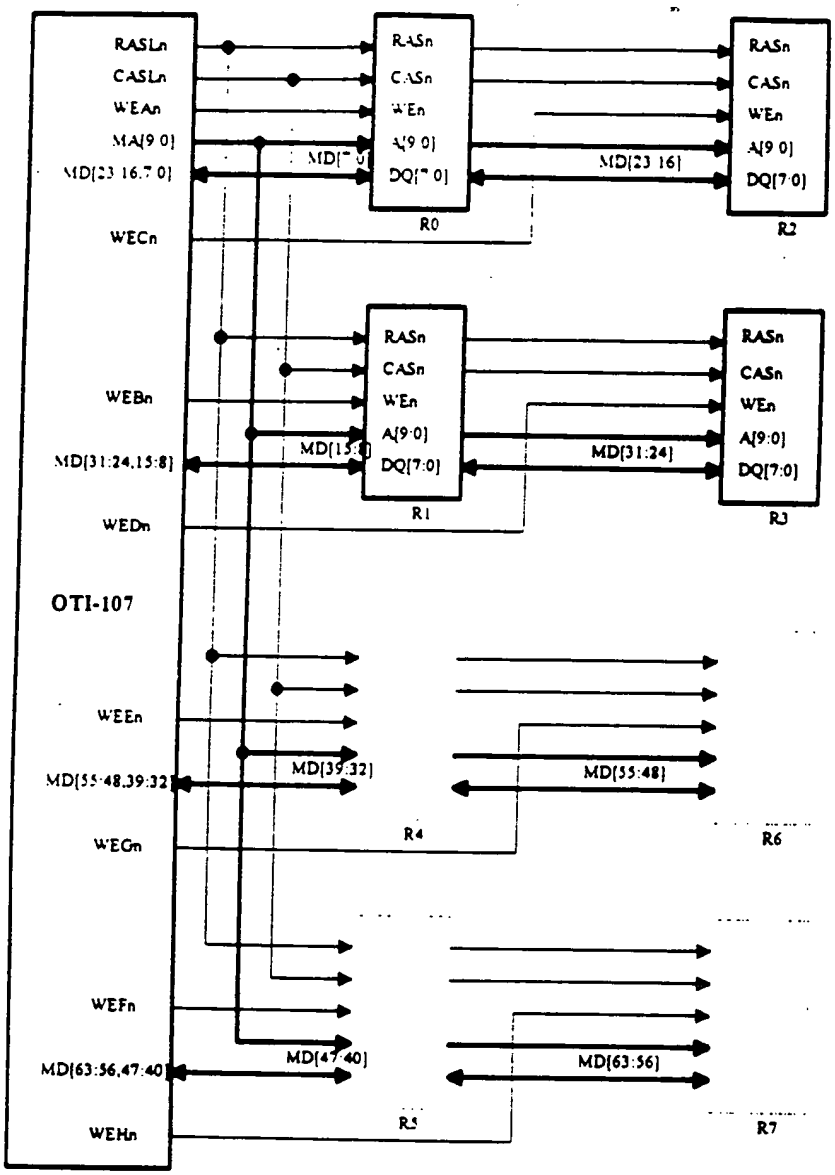


Figure 4.11 - 512Kx8 DRAM's, MD16, 32 & 64, 1M - 4M bytes

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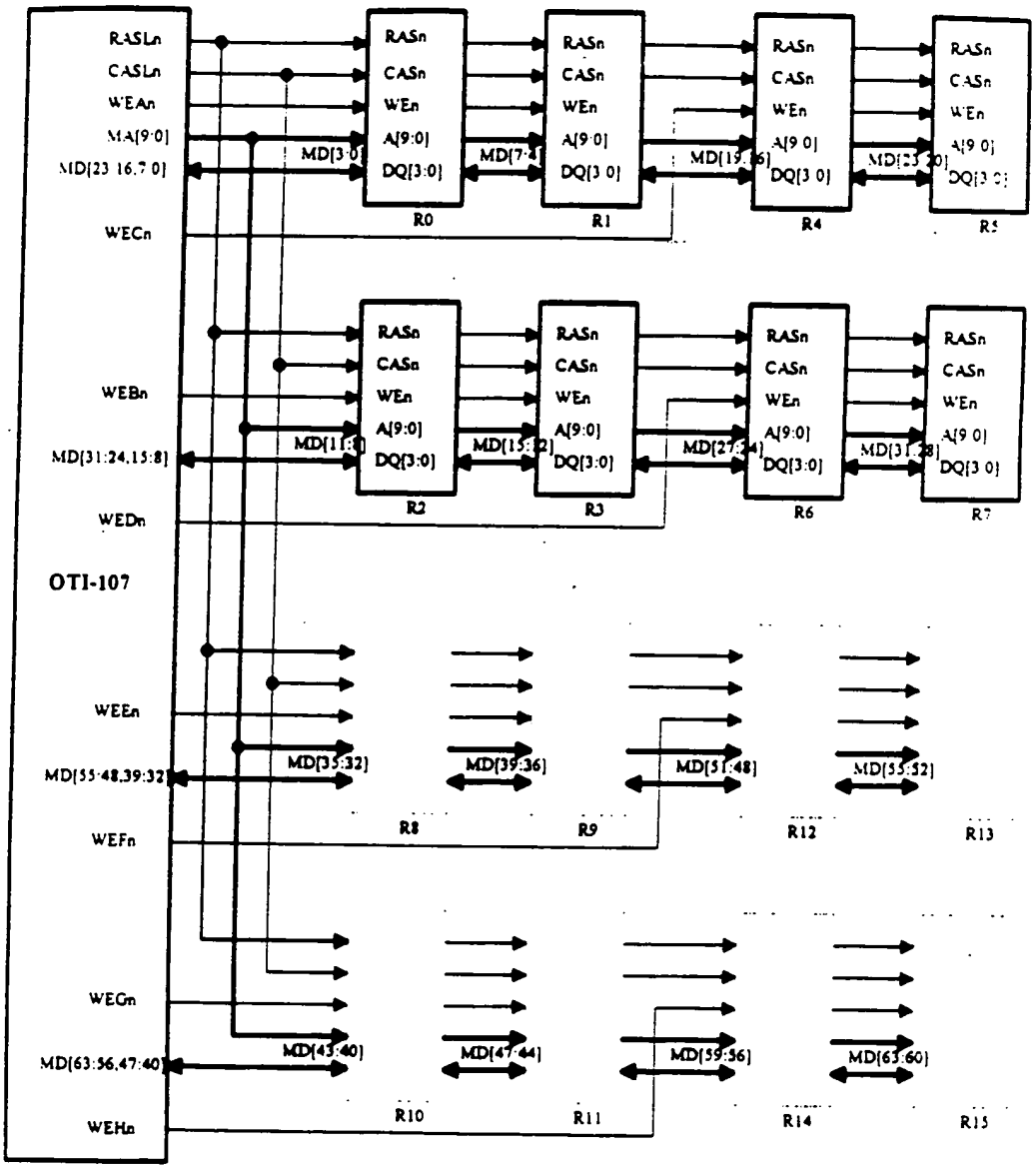


Figure 4.12 - 1024Kx4, MD16,32 & 64, 2M & 8M bytes

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4.8 Multimedia Interface

Typically, multimedia support in a VGA subsystem consists of an input port and an output port pair connecting directly to the graphics frame buffer memory (also referred to as the video memory). The input port accepts live video data (i.e continuous input data stream from any source) and stores it into the graphics frame buffer, eliminating the need of a system bus data path and a dual-frame-buffer memory scheme. The video data coming into the input port can be in either an RGB or a YUV data format. Once the video data is stored into the graphics frame buffer it can be displayed on the screen via the output port.

The output port consists of a hardware window logic section that displays the stored video data (as opposed to graphics data) on the screen. The hardware window fetches the video data directly from the graphics frame buffer and sends the video data to the DAC. There are two methods of displaying video data.

The first method involves storing the video data into a non-displayed area of the graphics frame buffer. In this case, a 'key' code is placed in the display area of the graphics frame buffer at the point at which the video data is to be displayed on the screen. As the data from the graphics frame buffer is sent to the DAC, the DAC scans the incoming data for the key code. When this key code is encountered the DAC will fetch the data from the non-displayed area of the graphics frame buffer; because the displayed data is stored in two different areas of the graphics frame buffer, the DAC must multiplex the data between the display area and the non-display area each time the key code is encountered. This technique is called 'chroma-keying' and uses a predefined byte for the key and a set of multiplexing logic to facilitate the switch between data types. The 'window' size for the video data that is displayed on the screen is controlled in the following manner. For each scan line chroma-keys are placed in the graphics frame buffer to indicate the points at which the data multiplexing between the video and graphics data is to occur. A key is placed in the display area to indicate the beginning of the video image. Another key is placed in the video data itself to indicate the end of the video image; the window size of the video image is defined in this manner. The advantage of chroma-keying is that the color depth of the video data (i.e. 4, 8, 16 or 24 bits per pixel) and format (RGB vs. YUV) can be different from that of the graphics data. While this scheme provides color depth flexibility it requires the use of an intelligent DAC such as Bt885 and support logic to multiplex between graphics and video data. Because the Bt885 DAC performs the switch between displaying graphics data and video data, both data types must be transferred out of the graphics frame buffer. This requires a very high transfer bandwidth out of the graphics frame buffer memory; data must be fetched from two different places in the frame buffer, one from the graphics data area (the display area) and the other from the video data area (the non-display area). This is accomplished by sending the graphics data out during the display time and sending the video data out during the non-display time. Note that this scheme effectively limits the size of the video window.

A second method is implemented in the 107 to eliminate these critical problems. It involves storing live video data into the graphics frame buffer at the location at which it will be displayed on the screen. This requires that the color depth of the video data be at the same color depth as that of the graphics data; also the input format must be in RGB format. This may limit the kind of video data that can be displayed, however, any ordinary DAC can be used which can result in a significant cost saving. In addition, this scheme does not require additional graphics frame buffer memory bandwidth.

In this case, no special keying codes are required. The contents of the graphics frame buffer are sent to the DAC without regard of data type. In order to support overlapping windows an Imaging Mask Map (not to be confused with the co-processor mask map) is utilized to mask the video data it is stored into the graphics frame buffer. The Imaging Mask Map is a 1bpp map used to prevent the incoming video data from updating current graphics data on the screen, thus preserving the content of any graphic data overlapping the video data. Each bit in the mask corresponds to one pixel in the displayed area of the screen. Only incoming pixels of the video data corresponding to set bits in the mask will be stored into the graphics frame buffer. Because the video data occupies a portion of the displayed area, the video data is sent to the DAC in the same manner as graphics data. The driver must determine the size and shape requirements of the video window and setup the Imaging Mask Map to simulate window overlapping.

The Imaging Mask Map is read and written as bytes in the graphics frame buffer memory address space; only whole bytes can be manipulated for each read or write to the mask. Since each bit in the mask corresponds to one

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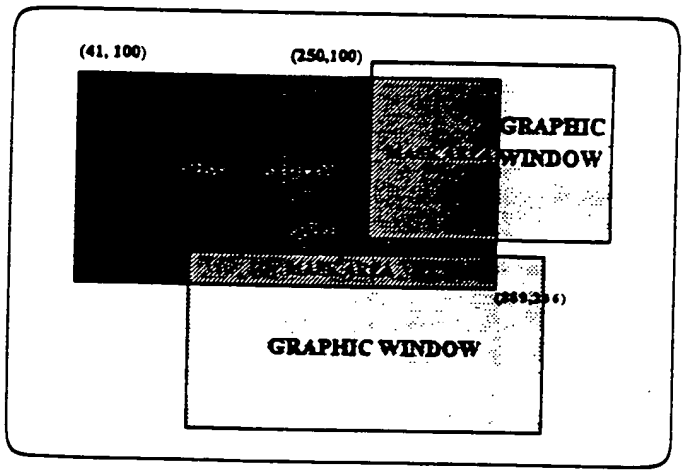
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pixel, and since the number of pixels that the mask operates on could be odd, the software driver must account for partial-byte read or writes to the mask. A '1' would allow video data to update the screen, a '0' would prohibit updating. This map can be located anywhere in the non-display area and is programmable through the Imaging Mask Map Start Address register. This map is assumed to be continuous and has no offset. There is no alignment hardware for this map. Unused bits should be filled with 0's.

There are two sets of registers that affect this scheme. The first set of registers control the video data window: HW Start Address Registers offset[9C-9E], HW Address Offset Register offset[9F] (these registers are in the memory mapped I/O space). The Start Address Registers define the address within the graphics frame buffer at which the input video data will be stored. The Address Offset Register defines the starting address of the next scan line of the video data. (The value in the Offset is the scan line length of the displayed area of the screen which may not be the same as the total scan line length.). Once these registers are setup, the video data is automatically written into the graphics frame buffer for each cycle on the input port. Or, in the case of the output port, the video data is fetched from the frame buffer for each cycle on the output port.

A second set of registers control the Imaging Mask Map: HW Mask Map Start Address Registers 3DF[98-9A], HW Control Register 3DF[96]. The Mask Map Start Address Registers define the address within the frame buffer at which the Imaging Mask Map begins. The Control Register enables the use of the mask. In the case in which the video data is stored directly into the display area of the frame buffer, the Imaging Mask Map, when enabled via the Control Register, prevents live video data from updating the existing contents of the frame buffer where ever a 0 is encountered in the mask. The area defined by the video data window control registers must be greater than or equal to the area masked by the Imaging Mask Map.

The figure below illustrates a conceptual display using the masking scheme in the 107.



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Figure 4.13 - Video Windows & Image Masking

In the example, the display resolution is 1024x768 and the color depth is 8-bits/pixel. The the absolute diagonal coordinates of the video windows are x=41 pixels/y=100 pixels and x=359 pixels/y=246 pixels. The Imaging Mask Map is typically placed in the upper, non-displayed area of the graphics frame buffer. For this resolution 98,304 bytes are required to store the mask data.

The Imaging Mask Map will contain 1's for the following areas: 41,100 to 250,200; 41,201 to 359,219; and 41,220 to 120,246. The mask will contain 0's in all other pixel positions.

The video window registers are setup to define the overall size of the video window. The HW Start Address is 'd12677, the HW Line Length is 'd10 (318 pixels is 2 pixels less than 10 double words)., the HW Address Offset is 'd64 (1024 pixels is the scan line length for this resolution). Since the line length of the incoming video data is greater than the amount displayed on the screen, the mask is setup to prevent last 2 pixels from being written to the frame buffer. Also, since the starting address of the video data actually specifies a location before x=41, the appropriate mask bits must be cleared.

The values in the Imaging Mask Map are set up in the following manner. Bytes 0 to 12677 in the mask contain 0's Byte 12678 contains 'h7F (because x=41 is the second pixel). Bytes 12679 to 12703 contain 'hFF. Byte 12704 contains 'hC0 (x=250 is at a partial byte boundary). This scheme is repeated until the entire mask is initialized to define the video data window. The software must account for partial byte values in the mask.

4.8.1 Input Port

The input port is an 16-bit synchronous data port that can receive data up to 33 MHz. For revision A of the chip, this input port is designed to interface to the Phillips SAA7191B or the Brooktree Bt812 directly with no external logic. Support for the SAA7191B/Bt812 includes a chip select, system I/O command and system data control logic, and I^2C bus. For future revision or version, the OTI-107 can be modified to interface directly to the VESA Media Channel, 16-bit mode and maintain pin-to-pin compatible with the current version.

The input port takes video data into the 107 and stores it into the graphics frame buffer. The input data can also be scaled vertically and/or horizontally. Vertical scaling by displaying every 2, 4, or 8 lines is supported with an option to start skipping on odd or even scan lines. Horizontal scaling by displaying every 2, 4 or 8 pixels is supported in a similar manner. Scaling is particularly important to save memory space and bandwidth.

The registers that control the input port are: HW Start Address Registers at offset[9C-9E], HW Address Offset Register at offset[9F] (these registers are in the memory mapped I/O space). The Start Address Registers define the address within the graphics frame buffer at which the input video data will be stored. The Address Offset Register defines the starting address of the next scan line of the video data. (The value in the Offset is the scan line length of the displayed area of the screen which may not be the same as the total scan line length.). Once these registers are setup, the video data is automatically written into the graphics frame buffer for each cycle on the input port. Or, in the case of the output port, the video data is fetched from the frame buffer for each cycle on the output port.

4.8.2 Output Port

The output port is supported as a hardware window (very similar to that of the hardware cursor) and is designed to interface with the Brooktree Bt885 with minimal additional logic (8 F374 when use with MD64, none with MD32). The data path for the video data is connected to the Bt885 via MD[63:0]. A video window can be defined through the Vertical Position Start, Width and Height registers. In this case the first display method is selected. The output port as described above is used when video data is stored in the non-display area and a smart DAC like the Bt885 is used. The hardware cursor is supported through the logic in the Bt885. A repeat line input signal is also available to assist the Bt885 to do vertical zooming. When this line is active, the memory controller would fetch the same video line again.

When an ordinary DAC is used, the hardware cursor logic is enabled in the 107 instead of the hardware window. In this case the second scheme must be used to display the video data window and the Imaging Mask Map is used to control the size of the video data window.

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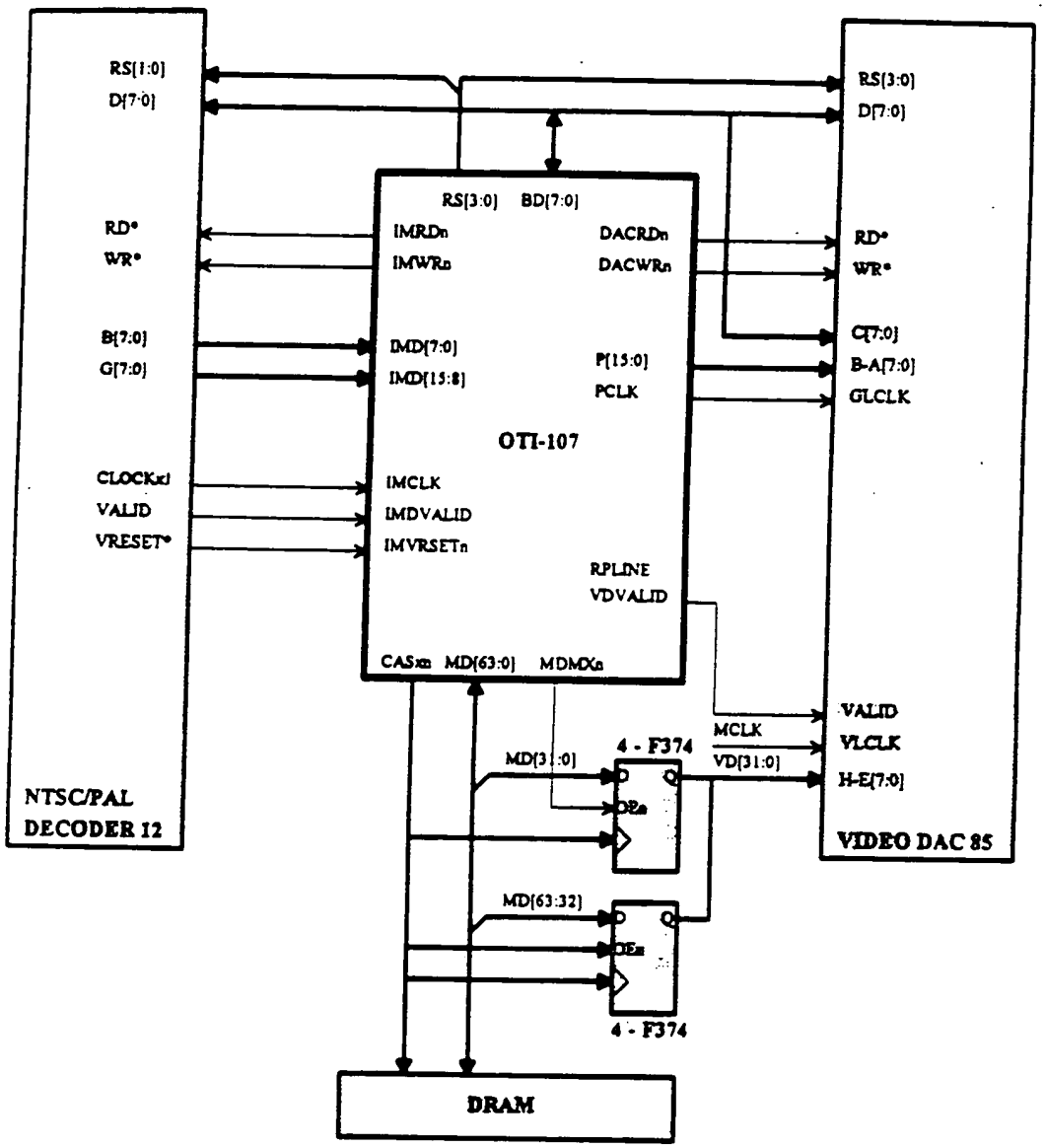


Figure 4.14 - Multi-Media Interface w/ Video DAC Block Diagram

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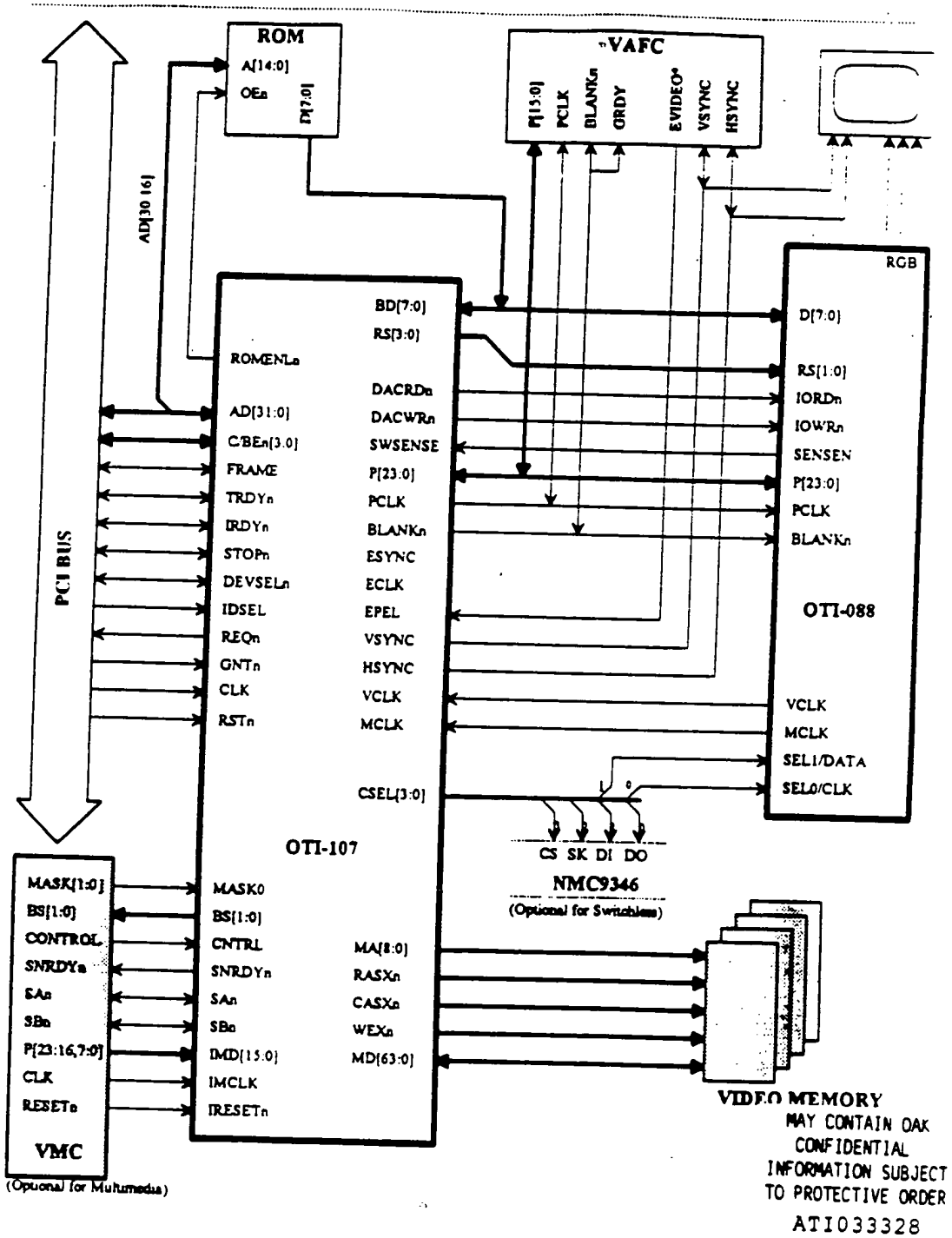


Figure 4.15 - Multi-Media Interface w/ VMC & VAFC (rev B only)

4.9 I²C/Auxiliary I/O Support

To save glue logic when external components are needed for the graphic subsystem (such as video decoder, image scaler), the OTI-107 provides additional address decoding, address latching and data routing for these external components. For components that have I²C interface instead of standard host interface, the OTI-107 can also interface with them through combination of hardware and software.

4.9.1 I²C Support

When the OTI-107 does not support VMC bus, there are two programmable pins available, SRCK and SRD, to support the I²C bus. These two pins are controlled and can be read from register ERC. Writing 0's will drive the pins low, and writing 1's will tristate the pins. Software can control and read these pins in accordance with the I²C bus protocol to program the external component's registers. See I²C Bus Specification for more information

4.9.2 Auxiliary I/O Support

On VL bus, auxiliary I/O can be supported by configuring the OTI-107 to generate DACCSn and ACSn instead of DACRDn & DACWRn. These chip select signals, can be ORed (LS32) with IOWRn and IORDn from the ISA bus to generate DACRDn, DACWRn, ARDn, and AWRn. The register select address can be connected directly to SA bus of the ISA connector. Data routing is done through the same LS245 that is used for DAC & BIOS ROM routing.

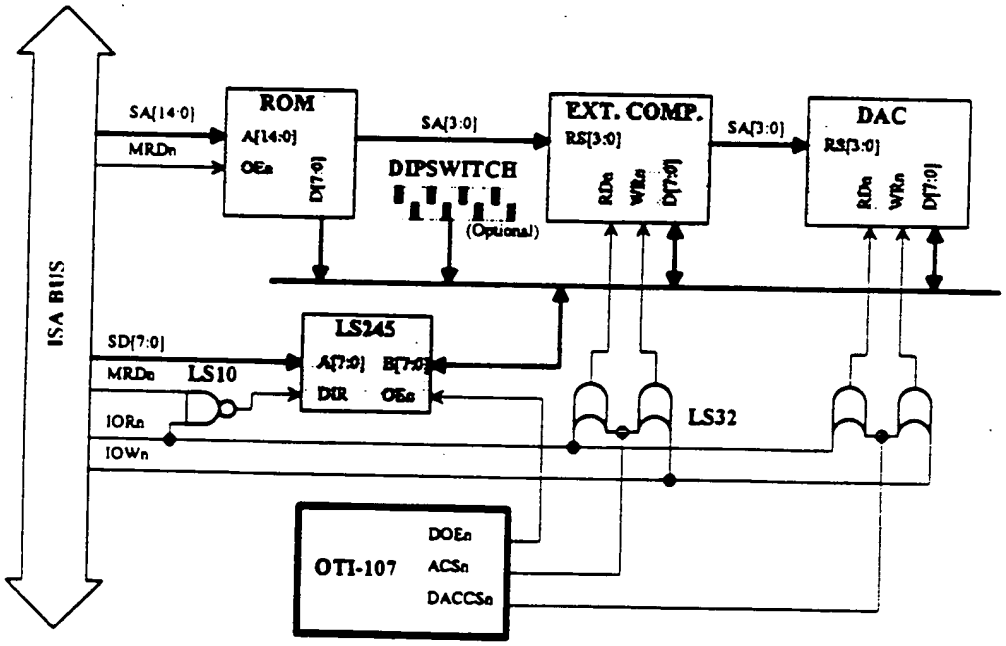


Figure 4.16 - Auxiliary I/O on VL Bus (via ISA Bus)

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On PCI bus, ARDn and AWRn are generated from OTI-107. ARS[3:0] are latched from system address and sent out to external components. Data is routed through the BD[7:0] bus. See figure 4.2 for more information.

On ISA bus, ARDn and AWRn are also generated, BD[7:0] is also used to route data, but ARS[3:0] are not generated and the register select lines should be connected directly to the system bus just like on VL bus.

4.10 Power Management Support

The OTI-107 has power saving modes that are compliant to the VESA DPMS Proposal version 1.0p. The four modes of power management are as follow:

State	HSYNC	VSYNC	BLANKn	P[23:0]	DPMS Requirement	Power Savings
On	Pulses	Pulses	Active	Active	Mandatory	None
Stand-by	No Pulses	Pulses	Blanked	Blanked	Optional	Minimal
Suspend	Pulses	No Pulses	Blanked	Blanked	Mandatory	Substantial
Off	No Pulses	No Pulses	Blanked	Blanked	Mandatory	Maximum

Active - means normal operation, signal is switching between active and inactive

No Pulses - signals remain at inactive state (HSYNC, VSYNC = 0)

Pulses - normal operation for HSYNC & VSYNC

Blanked - BLANKn is asserted (0), P[23:0] = 0

Power management is controlled by ER0F.

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5 PIN DESCRIPTION

5.1 ISA Bus Interface

Pin Name	Pin Number	Type	Description
MASTERn	60	I	MASTERn. This pin indicates the current cycle is a master cycle when the controller is in add-on configuration. It enables the LA address to pass through during master cycle.
MWRn	62	I	MEMORY WRITE. Active low memory write strobe.
MRDn	63	I	MEMORY READ. Active low memory read strobe.
CINTn	66	O_{od}	CRT INTERRUPT REQUEST. Interrupt is asserted when vertical retrace occurs if it is enabled by bit 5 of the Vertical Retrace End register. It is an active low open drain output.
RESETn	67	I	RESET. Active low system reset signal. This input signal will reset the VGA controller and initialize the configuration register based on the logic level on MD[15:0] pins at power-up reset time. This signal is inverted from the bus reset.
LA[23:17]	75-72,70, 65-64	I	UNLATCHED SYSTEM ADDRESS BITS 23:17. These bits are decoded to generate M16n. Bits 19:17 are latched by ALE to generate SA[19:17].
M16n	68	O_{od}	16-BIT MEMORY. Active low, open drain output signal used to indicate to the system that the present cycle is a 16-bit data transfer to video memory. This signal is derived from the decoding of LA23:LA17
ZEROWSn	69	O_{od}	ZERO WAIT STATE This pin is used to indicate the current cycle is a 0 wait state cycle.
IO16n	71	O_{od}	16-BIT I/O. This active low, open drain output signal is used to indicate to the system that the present data transfer is a 16-bit I/O cycle. It is derived from decode of address SA19-SA0.
BHEn	76	I	BYTE HIGH ENABLE. This active low input indicates that there is valid data on SD[15:8] bus. This signal and SA[0] together indicate to the OTI-097 whether an 8 bit or 16 bit cycle is being executed by the system.
ALE	78	I	ADDRESS LATCH ENABLE. This input is used to latch a valid address from the CPU in add-on configuration.
RFSHn	79	I	REFRESH. This input is used to qualify the video memory and I/O access from CPU. An active low indicates a system memory refresh cycle.
IORn	80	I	I/O READ. This is an active low I/O read strobe.
IOWn	81	I	I/O WRITE. This is an active low I/O write strobe.
IOCHRDY	82	O_{od}	IO CHANNEL READY. An open drain active high output to signal processor that it ready for memory access. This signal is used to add wait states to bus cycle during video memory access.
SA[16:0]	101-92,90-85,83	I	LATCHED SYSTEM ADDRESS BITS 16:0

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SD[15:0]	102-108,110, 112-115,117-120	I/O	SYSTEM DATA BUS BITS 15:0
AEN	111	I	ADDRESS ENABLE. This input is used to qualify the video I/O access from CPU. When it is active high, the DMA controller has control of the address bus, data bus, and command lines

Total 55 pins

5.2 VL Bus Interface

Pin Name	Pin Number	Type	Description
SA[31:2]	3-10,72-69, 65-62,60-47	I	SYSTEM ADDRESS BUS bits 31:2. This bus should be connected to the ADR[31:2] bus of the VL connector.
CINTn	66	O_{od}	CRT INTERRUPT REQUEST. Interrupt is asserted when vertical retrace occurs if it is enabled by bit 5 of the Vertical Retrace End register. It is an active low open drain output.
RESETn	67	I	MASTER RESET. This reset signal is used to reset all internal state machines and some default registers. During Reset active, all bidirectional buses are tri-stated. This signal is also used to latch-in the configuration register values. This reset is active low and should be connected the VL bus RESETn signal instead of the ISA bus active high RESET.
PROCLK	68	I	PROCESSOR CLOCK. Processor clock input used to sample CPU status and address. This clock is 1X for VL bus but can be configured to be 2X. This signal should be connected to the LCLK pin of the VL connector.
SD[31:0]	73-76,78-81, 85-90,92-93, 102-108,110, 112-115,117-120	I/O	SYSTEM DATA BUS bits 31:0. This bus should be connected to the DAT[31:0] bus of the VL connector.
BEn[3:0]	82,94,101,111	I	BYTE ENABLES. Used to indicate which byte lanes of the 32-bit data bus are involved with the current transfer cycle. These signals should be connected to the BE[3:0] pins of the VL connector.
LBSELn	83	O_{od}	LOCAL BUS SELECT. Active low simulated open drain output signal used to indicate to system controller chipset that the current cycle is a video local bus cycle and the chipset should not response to the CPU. This signal should be connected to the LDEVn pin of the VL connector.
ADSn	95	I	ADDRESS STATUS. Active low input used to indicate a valid address is on the bus. This signal should be connected to the ADSn pin of the VL connector.
SRDYIn	96	I	SYSTEM READY INPUT. Input from chipset to indicate termination of a cycle. This signal should be connected to the RDYRTNn pin of the VL connector. For system without RDYRTNn signal, SRDYn should be routed back to SRDYIn.

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SRDYn	97	O_{od}	SYSTEM READY. Tristateable active low output used to indicate the termination of a bus cycle. This signal should be driven high for one Proclk before being released. This signal should be driven during the first T2 state only when in Fast Write configuration. For regular write configuration and all read cycles, this signal should only be driven from the second T2 state onward. This signal should be connected to the LRDYn pin of the VL connector.
ISACMD	98	I	ISA COMMAND. This is a NAND of IORn, IOWn, MRDn. This signal is used to generate DACRDn, DACWRn, and DOEn.
WRn	99	I	WRITE/READ. Signal used to distinguish between a write (WRn high) or a read (WRn low) transfer. This signal should be connected to the W/Rn pin of the VL connector.
MIOn	100	I	MEMORY or I/O STATUS. Input from the bus to indicate the current cycle is a memory (MIOn high) transfer or an IO (MIOn low) transfer This signal should be connected to the M/IOn pin of the VL connector

Total 76 pins.

5.3 PCI Bus Interface

Pin Name	Pin Number	Type	Description
CINTn	66	O_{od}	CRT INTERRUPT REQUEST. Interrupt is asserted when vertical retrace occurs if it is enabled by bit 5 of the Vertical Retrace End register. It is an active low open drain output.
RESETn	67	I	RESET. This reset signal is used to reset all internal state machines and some default registers. During RST active, all bidirectional buses are tri-stated. This signal is also used to latch-in the configuration register values. This reset is active low.
CLK	68	I	CLOCK. Used to provide timing for all trasactions on PCI. ALL other PCI signals are sampled on the rising edge of CLK, and all other timing parameters are defined with respect to this edge.
PAR	70	I/O	PARITY. Active high even parity across AD[31:0] and C/BEn[3:0]
GNTn	71	I	GRANT. Input from the bus arbiter to indicate that the bus has been granted.
REQn	72	O	REQUEST. Output to the bus arbiter to request for the bus.
AD[31:0]	73-76,78-81, 85-90,92-93, 102-108,110, 112-115,117-120	I/O	ADDRESS/DATA BITS 31:0. Address and Data are multiplexed. During the first clock of transaction AD[31:00] contain a physical byte address (32bits). During subsequent clocks, AD[31:0] contain data.
C/BEn[3:0]	82,94,101,111	I/O	BUS COMMAND/BYTE ENABLES. Bus Command and Byte Enables are multiplexed. During the address phase of transaction, C/BEn define the bus command. During the data phase C/BEn are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. This bus is input during slave mode and output during master mode.
IDSEL	83	I	INITIALIZATION DEVICE SELECT. Active high chip select in lieu of the upper 24 address lines during configuration read and write transactions

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FRAMEn	95	I/O	CYCLE FRAME. Used to indicate the beginning and duration of an access. This signal is input during slave mode and output during master mode.
IRDYn	96	I/O_{ssd}	INITIATOR READY. IRDYn used to indicate the initiating agent's ability to complete the current data phase of the transacuon. It is used in conjunction with TRDYn. This singnal is input during slave mode and output during master mode.
TRDYn	97	I/O_{ssd}	TARGET READY. Used to indicate the target agent's ability to complete the current data phase of the transaction. TRDYn is used in conjunction with IRDYn. A data phase is completed on any clock both TRDYn and IRDYn are sampled asserted. During a read TRDYn indicates that valid data is present on AD[31:0]. During a write it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDYn and TRDY are asserted together. This signal is output during slave mode and input during master mode.
DEVSELn	98	I/O_{ssd}	DEVICE SELECT. When acitvely driven, indicates the driving device has decoded its address as the target of the current access. As an input it indicates whether any device on the bus has been selected. This signal is an output during slave mode and input during master mode.
STOPn	99	I/O_{ssd}	STOP. Active low signal used by the current slave to request the current Master to stop the current transaction. This signal is an output during slave mode and input during master mode.
LOCKn	100	I/O_{ssd}	LOCK. Active low singal used indicates an atomic operation that may require multiple transactions to complete.

Total 49 pins

5.4 BIOS ROM Interface

Pin Name	Pin Number	Type	Description
DOEn/ ROMENLn	45	O	DATA OUTPUT ENABLE. VL bus configuration, this is an active low signal to enable the low byte of BIOS data, DACK data, and DIP SWITCH data to ISA data bus. Depend on the cycle, the selected device will drive out the data or will receive the data. ROM ENABLE. PCI bus configuration, this is an active low signal to enable the ROM read. ISA bus 16-bit ROM configuration, this signal is used to enable the external buffer which routes the upper byte out to the system bus

Total 1 pin

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5.5 Clock Interface

Pin Name	Pin Number	Type	Description
VCLK	2	I	VIDEO CLOCK. This is the master input pixel clock.
CSEL[3]	11	O	CLOCK SELECT LINE 3. Clock select lines are used to select appropriate video clock frequency. This pin can be programmed through register 3DF index 6.
CSEL[2]	12	O	CLOCK SELECT LINE 2. Clock select lines are used to select appropriate video clock frequency. This pin can be programmed through register 3DF index 6.
CSEL[1]	13	O	CLOCK SELECT LINE 1. Clock select lines are used to select appropriate video clock frequency. This pin can be programmed through register 3DF index 6 or register 3C2.
CSEL[0]	14	O	CLOCK SELECT LINE 0. Clock select lines are used to select appropriate video clock frequency. This pin can be programmed through register 3DF index 6 or register 3C2.
MCLK	196	I	MEMORY CLOCK. This is the input clock used for memory timing.

Total 6 pins.

5.6 Feature Connector Interface

Pin Name	Pin Number	Type	Description
ESYNC	216	I	ENABLE SYNC. This active high input is used to enable BLANKn, HSYNC and VSYNC.
EPCLK	220	I	ENABLE PCLK. This active high input is used to enable PCLK output.
EPDATA	222	I	ENABLE PDATA. This active high input is used to enable P[23:16]

Total 3 pins

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5.7 DAC Interface

Pin Name	Pin Number	Type	Description
P[23:16]	3-10	O	PIXEL DATA. Upper 8-bit of pixel data. This bus exists on PCI & ISA bus only
P[15:0]	224-229,231-240	O	PIXEL DATA. Output data bus interfaces to an external palette chip for color mapping during CRT display.
PCLK	221	O	PIXEL CLOCK. Pixel clock output to DAC to latch the pixel data P7-P0. It is derived from the current dot clock rate of operating mode
BLANKn	217	O	BLANK. Active low output signal to RAMDAC to blank the pixel data for the display monitor.
DACWRn	214	O	RAMDAC WRITE. An active low I/O write signal generated for writing external color palette registers. For VL bus configuration, this signal is also used to control data flow from ISA bus to and from the DAC, ROM, and DIP SWITCH. When DACWRn is high, data is outputing to the ISA bus, when DACRDn is low, data is receiving from the ISA bus
DACRDn	215	O	RAMDAC READ. An active low I/O read signal generated for reading external color palette registers.
SWSENSE	15	I	SWITCH SENSE. An input signal used to auto detect color or mono monitor.

Total of 29 pins for PCI & ISA buses, and 21 pins for VL bus.

5.8 Monitor Interface

Pin Name	Pin Number	Type	Description
VSYNC	218	O	VERTICAL SYNC. Vertical synchronization pulse to display monitor. The polarity of the pulse is determined by bit 7 of the Miscellaneous Output Register.
HSYNC	219	O	HORIZONTAL SYNC. Horizontal synchronization pulse to display monitor. The polarity of the pulse is determined by bit 6 of the Miscellaneous Output Register.

Total 2 pins

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5.9 Auxiliary Bus Interface

Pin Name	Pin Number	Type	Description
ARDn	49	O	AUXILIARY READ. This pin is decoded from system address and ORed with I/O read command internally to generate register read for some other device in the graphic subsystem. This pin is valid for PCI & ISA buses only.
AWRn	50	O	AUXILIARY WRITE. This pin is decoded from system address and ORed with I/O write command internally to generate register write for some other device in the graphic subsystem. This pin is valid for PCI & ISA buses only.
BD[7:0]	51-58	I/O	AUXILIARY DATA BUS 7:0. Data bit 7-0 of BIOS high byte data in 16-bit BIOS ISA bus configuration. Data bit 7-0 in 8-bit BIOS ISA or PCI bus configuration. Can also be used for buffering DAC data and dipswitch data or other devices in the subsystem. The OTI-107 routes data from/to BD bus out to/from SD/AD bus during read/write cycles BD bus is available in ISA bus and PCI bus interface only
ARS[3:0]	59-60,62-63	O	AUXILIARY REGISTER SELECT 3:0. These pins are available for PCI bus only. System address bits 3:0 is latched from the PCI bus and send out for devices in the graphic subsystem. The primary intention for these pins are for the color palette, but they can be used for other devices as well. These pins are valid on PCI bus only

Total 14 pins for PCI bus, 10 pins for ISA bus and 0 pin for VL bus

5.10 I^2C Interface

Pin Name	Pin Number	Type	Description
SRCK	16	I/O	SERIAL CLOCK.
SRD	44	I/O	SERIAL DATA.

Total of 2 pins. These pins do not exist when VMC bus is supported.

5.11 Bt885 Support

Pin Name	Pin Number	Type	Description
VDVALID	46	O	VIDEO DATA VALID. Output used indicate to the Video DAC that data is valid and ready to be clocked in.
MDMXn	47	O	MEMORY DATA MUX. Active low signal to mux MD[63:32] with MD[31:0] for the Video DAC. This pin exists for PCI and ISA bus only. For VL bus, CASxn can be inverted to generate MDMXn.
RPLINE	48	I	REPEAT LINE. Active high signal used to indicate to the OTI-107 to repeat the previous line for video window. This is used for vertical zooming. This pin exists for PCI and ISA bus only.

Total of 3 pins for PCI & ISA buses, and 1 pin for VL bus.

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5.12 Video Memory Interface

Pin Name	Pin Number	Type	Description
MA[7:0]	170-163	O	MEMORY ADDRESS. Memory address bits 7:0 for all DRAM configurations.
RASLn	161	O	ROW ADDRESS STROBE LOW. Active low output signal used for all DRAM configurations.
RASHn/ MA[9]	172	O	ROW ADDRESS STROBE HIGH. Active low output signal used in 64-bit memory bus, 64Kx16 and 256KxXX DRAM's configuration. MEMORY ADDRESS 9. For 512Kx8 and 1Mx4 DRAM's, this pin is memory address bit 9, and should be connected to all maps and all banks of DRAM's.
CASLn/ WELn	162	O	COLUMN ADDRESS STROBE LOW. For x4, x8 and x16 DRAM's with 1 CASn and 2 WEn, this pin is configured to be CASLn. WRITE ENABLE LOW. For x16 DRAM's with 2 CASn and 1 WEn, this pin is configured to be WELn.
CASHIn/ WEHIn/ MA[8]/	171	O	COLUMN ADDRESS STROBE HIGH. Used for 64-bit memory bus, 64Kx16 DRAM, 1 CASn, 2 WEn only. WRITE ENABLE HIGH. Used for 64-bit memory bus, 64Kx16 DRAM with 2 CASn & 1 WEn only. MEMORY ADDRESS 8. For 256KxXX, 512Kx8, and 1Mx4 DRAM's, this pin is memory address bit 8, and should be connected to all maps and all banks of DRAM's.
WEAn/ CASAn	122	O	WRITE ENABLE A. Active low write enable to memory map 0 and 1 in 16-bit MD configurations (4 256Kx4, 2 512Kx8, 1 256Kx16 w/ 1 CASn 2 WEn), write enable for map 0 in 32-bit MD configuration and 64-bit MD configuration when MA=XXx000. COLUMN ADDRESS STROBE A. For x16 DRAM's with 2 CASn, 1 WEn, this pin is CASAn controlling the same maps as WEAn.
WEBn/ CASBn	131	O	WRITE ENABLE B. Active low write enable pulse to memory map 2 and 3 in 16-bit MD configurations (4 256Kx4, 2 512Kx8, 1 256Kx16 w/ 1 CASn 2 WEn), write enable for map 2 in 32-bit MD configuration and 64-bit MD configuration when MA=XXx001. COLUMN ADDRESS STROBE B. For x16 DRAM's with 2 CASn, 1 WEn, this pin is CASBn controlling the same maps as WEBn.
WECn/ CASCn	141	O	WRITE ENABLE C. Active low write enable pulse to memory map 1 in 32-bit MD configuration and 64-bit MD configuration when MA=XXx010. COLUMN ADDRESS STROBE C. For x16 DRAM's with 2 CASn, 1 WEn, this pin is CASCn controlling the same maps as WECn.
WEDn/ CASDn	150	O	WRITE ENABLE D. Active low write enable pulse to memory map 3 in 32-bit MD configuration and 64-bit MD configuration when MA=XXx011. COLUMN ADDRESS STROBE D. For x16 DRAM's with 2 CASn, 1 WEn, this pin is CASDn controlling the same maps as WEDn.
WEEn/ CASEn	173	O	WRITE ENABLE E. Active low write enable to memory map 0 in 64-bit MD configuration when MA=XXx100. COLUMN ADDRESS STROBE E. For x16 DRAM's with 2 CASn, 1 WEn, this pin is CASEn controlling the same maps as WEEn.

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WEFn/ CASFn	183	O	WRITE ENABLE F. Active low write enable to memory map 1 in 64-bit MD configuration when MA=XXx101. COLUMN ADDRESS STROBE F. For x16 DRAM's with 2 CASn, 1 WEn, this pin is CASFn controlling the same maps as WEFn
WEGn/ CASGn	193	O	WRITE ENABLE G. Active low write enable to memory map 2 in 64-bit MD configuration when MA=XXx110. COLUMN ADDRESS STROBE G. For x16 DRAM's with 2 CASn, 1 WEn, this pin is CASGn controlling the same maps as WEGn.
WEHn/ CASHn	204	O	WRITE ENABLE H.COLUMN ADDRESS STROBE H. Active low write enable to memory map 3 in 64-bit MD configuration when MA=XXx111. COLUMN ADDRESS STROBE H. For x16 DRAM's with 2 CASn, 1 WEn, this pin is CASHn controlling the same maps as WEHn. Note that this is WE H or CAS H as opposed to WE HIGH or CAS HIGH
MD[63:0]	213-207,205, 203-200,198-197 195-194,191-184 182,180-174, 159-154,152-151 149-142,139-132 130-123	I/O	MEMORY DATA. Memory data bits 63-0. MD[15:0] are also used for configuration register during hardware reset. MD[7:0] correspond to bits 7:0 of Configuration Register 1, MD[15:8] correspond to bits 7:0 of Configuration Register 2, MD[23:16] correspond to bits 7:0 of Configuration Register 3.

Total 84 Pins

5.13 EEPROM Interface

Pin Name	Pin Number	Type	Description
EEPRD	195	I	EEPROM READ DATA. Data can be read from the EEPROM through the data read bit in the register 3DF index 18.
EEPWD	196	O	EEPROM WRITE DATA. Data can be written to the EEPROM through the data bit in the register 3DF index 18.
EEPSK	197	O	EEPROM SHIFT CLOCK. This clock can be toggled through register 3DF index 18.
EEPCS	198	O	EEPROM CHIP SELECT. This signal is used to enable the serial EEPROM for read and write operations.

Total 0 pin (pins EEPCS, EEPRD, EEPWD & EEPSK are muxed with CSEL[3:0])

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5.14 Imaging Interface Option 1 (all revisions)

Pin Name	Pin Number	Type	Description
IMVRSETn	17	I	IMAGING VERTICAL RESET. Acuve low input used to indicate beginning of new frame.
IMHRSETn	18	I	IMAGING HORIZONTAL RESET. Acuve low input used to indicate beginning of new line.
IMDVALID	21	I	IMAGING DATA VALID. Acuve high input used to indicate that data is ready to be latched in.
IMCLK	23	I	IMAGING DATA CLOCK. Input clock used to clock-in IMD[7:0]
IMD[15:0]	43-42,40-27	I	IMAGING PORT DATA. Multimedia port input data bits 15.0 This data is latched in at the rising edge of IMCLK.

Total 20 pins

5.15 Media Bus - Imaging Interface Option 2 (future revision only)

Pin Name	Pin Number	Type	Description
SAn	16	I/O	SERIAL LINE A - Serial I/O line used to link devices together in a chain. It is configured during the device ID writing phase, and is used to ensure that each device receiveds a unique ID.
BSn[1:0]	18-17	I/O	IMAGING BUS SIZE. These two signals are used to downsize the bus from 32 to 16-bits.
SNRDYn	20	O_{od}	SLAVE NOT READY - Active low open drain output used to indicate that the OTI-107 is not ready to receive data.
CNTRL	21	I	IMAGING CONTROL. Used to indicate that a Control Cycle rather than a data transfer is taking place on the next transfer.
IRESETn	22	I	IMAGING PORT RESET - Active low reset signal generated from the VESA Media Bus.
IMCLK	23	I	IMAGING DATA CLOCK. Input clock used to clock-in IMD[7:0]
MASK[1:0]	25-24	I	IMAGING MASK BIT 0 - Input used to indicate whether the accompanying pixel should be displayed. This signal is combined with the internal Imaging Mask Map to form the final mask. This signal is also used with SA & SB during the configuration process to assign ID's.
IMD[15:0]	43-42,40-27	I	IMAGING PORT DATA. Multimedia port input data bits 15:0. This data is latched in at the rising edge of IMCLK.
SBn	44	I/O	SERIAL LINE B - Serial I/O line used to link devices together in a chain. It is configured during the device ID writing phase, and is used to ensure that each device receiveds a unique ID.

Total 26 pins

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5.16 Power & Ground

Pin Name	Pin Number	Type	Description
VSSO0	1	GNDO	EXTERNAL GROUND
VSSO1	19	GNDO	EXTERNAL GROUND
VSSO2	41	GNDO	EXTERNAL GROUND
VSSO3	61	GNDO	EXTERNAL GROUND
VSSO4	91	GNDO	EXTERNAL GROUND
VSSO5	109	GNDO	EXTERNAL GROUND
VSSO6	121	GNDO	EXTERNAL GROUND
VSSO7	140	GNDO	EXTERNAL GROUND
VSSO8	160	GNDO	EXTERNAL GROUND
VSSO9	181	GNDO	EXTERNAL GROUND
VSSO10	206	GNDO	EXTERNAL GROUND
VSSO11	230	GNDO	EXTERNAL GROUND
VSSI0	77	GNDI	INTERNAL GROUND
VSSI1	192	GNDI	INTERNAL GROUND
VDD0	21	VDDB	EXTERNAL & INTERNAL POWER
VDD1	75	VDDB	EXTERNAL & INTERNAL POWER
VDD2	124	VDDB	EXTERNAL & INTERNAL POWER
VDD3	179	VDDB	EXTERNAL & INTERNAL POWER
VDD4	199	VDDB	EXTERNAL & INTERNAL POWER
VDD5	223	VDDB	EXTERNAL & INTERNAL POWER

Total 20 pins.

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Pin Count for VL bus:

System Interface	76
Memory Interface	84
DAC & Monitor	23
Feature Connector	3
ROM Interface	1
EEPROM Interface	0
Clock Interface	6
Auxiliary bus	0
Multimedia	27
Power & Ground	20
Total	**240**

Pin Count for PCI bus:

System Interface	49
Memory Interface	84
DAC & Monitor	31
Feature Connector	3
ROM Interface	1
EEPROM Interface	0
Clock Interface	6
Auxiliary bus	14
Multimedia	29
Power & Ground	20
Total	**237**

Pin Count for ISA bus:

System Interface	55
Memory Interface	84
DAC & Monitor	31
Feature Connector	3
ROM Interface	1
EEPROM Interface	0
Clock Interface	6
Auxiliary bus	10
Multimedia	29
Power & Ground	20
Total	**239**

Pin Type:

I	Input
I_{pu}	Input with internal pull-up
O	Output
I/O	Input/Output
O_{od}	Open drain output
O_{sod}	Simulated open drain output - output should be driven high for one system clock before released.

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5.17 Pin Cross Reference Table

Pin Number	Type	Drive (DC)	Pad Name	ISA	PCI	VL	Next Rev * (VMC Option)
1	GNDO		PV0A	VSSO0	VSSO0	VSSO0	
2	I		PT5D01	VCLK	VCLK	VCLK	
3-10	I/O	4mA	PT5B02	P[23:16]	P[23:16]	SA[31:24]	
11	O	2mA	PT5O01	CSEL[3]/ EEPCS	CSEL[3]/ EEPCS	CSEL[3]/ EEPCS	
12	O	2mA	PT5O01	CSEL[2]/ EEPSK	CSEL[2]/ EEPRD	CSEL[2]/ EEPSK	
13	O	2mA	PT5O01	CSEL[1]/ EEPWD	CSEL[1]/ EEPWD	CSEL[1]/ EEPWD	
14	I/O	2mA	PT5B01	CSEL[0]/ EEPRD	CSEL[0]/ EEPRD	CSEL[0]/ EEPRD	
15	I		PT5D01	SWSENSE	SWSENSE	SWSENSE	
16	I/O	4mA	PT5B02	SRCK	SRCK	SRCK	SAn
17	I		PT5D01	IMVRSETn	IMVRSETn	IMVRSETn	BSn[0]
18	I		PT5D01	IMHRSETn	IMHRSETn	IMHRSETn	BSn[1]
19	GNDO		PV0A	VSSO1	VSSO1	VSSO1	
20	O_{od}	4mA	PT5T02	NC	NC	NC	SNRDYn
21	I		PT5D01	IMDVALID	IMDVALID	IMDVALID	CNTRL
22	I		PT5D01	NC	NC	NC	IRESETn
23	I		PT5D01	IMCLK	IMCLK	IMCLK	
24-25	I		PT5D01	NC	NC	NC	MASK[0:1]
26	VDDB		PVDF	VDD0	VDD0	VDD0	
27-40	I		PT5D01	IMD[0:13]	IMD[0:13]	IMD[0:13]	
41	GNDO		PV0A	VSSO2	VSSO2	VSSO2	
42-43	I		PT5D01	IMD[15:14]	IMD[15:14]	IMD[15:14]	
44	I/O	4mA	PT5B02	SRD	SRD	SRD	SBn
45	O	2mA	PT5O01	ROMENLn	ROMENLn	DOEn	
46	O	2mA	PT5O01	VDVALID	VDVALID	VDVALID	
47	O	2mA	PT5O01	MDMXn	MDMXn	SA[2]	
48	I		PT5D01	RPLINE	RPLINE	SA[3]	
49	I/O	2mA	PT5B01	ARDn	ARDn	SA[4]	
50	I/O	2mA	PT5B01	AWRn	AWRn	SA[5]	
51-58	I/O	2mA	PT5B01	BD[7:0]	BD[7:0]	SA[6:13]	
59	I/O	2mA	PT5B01	NC	ARS[3]	SA[14]	
60	I/O	2mA	PT5B01	MASTERn	ARS[2]	SA[15]	
61	GNDO		PV0A	VSSO3	VSSO3	VSSO3	
62	I/O	2mA	PT5B01	MWRn	ARS[1]	SA[16]	
63	I/O	2mA	PT5B01	MRDn	ARS[0]	SA[17]	
64	I	2mA	PT5D01	LA[17]	NC	SA[18]	
65	I	2mA	PT5D01	LA[18]	NC	SA[19]	
66	O	24mA	PT5T04	CINTn	CINTn	CINTn	
67	I		PT5D01	RESETn	RESETn	RESETn	
68	I/O	24mA	PT5B04	M16n	CLK	PROCLK	
69	I/O	24mA	PT5B04	ZEROWSn	NC	SA[20]	

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70	I/O	8mA	PT5B03	LA[19]	PAR	SA[21]	
71	I/O	24mA	PT5B04	IOi6n	GNTn	SA[22]	
72	I/O	8mA	PT5B03	LA[20]	REQn	SA[23]	
73	I/O	8mA	PT5B03	LA[21]	AD[31]	SD[31]	
74	I/O	8mA	PT5B03	LA[22]	AD[30]	SD[30]	
75	I/O	8mA	PT5B03	LA[23]	AD[29]	SD[29]	
76	I/O	8mA	PT5B03	BHEn	AD[28]	SD[28]	
77	GNDI		PV0B	VSSI0	VSSI0	VSSI0	
78	I/O	8mA	PT5B03	ALE	AD[27]	SD[27]	
79	I/O	8mA	PT5B03	RFSHn	AD[26]	SD[26]	
80	I/O	8mA	PT5B03	IORn	AD[25]	SD[25]	
81	I/O	8mA	PT5B03	IOWn	AD[24]	SD[24]	
82	I/O	24mA	PT5B04	IOCHRDY	C/BEn[3]	BEn[3]	
83	I/O	8mA	PT5B03	SA[0]	IDSELn	LBSELn	
84	VDDB		PVDF	VDD1	VDD2	VDD3	
85	I/O	8mA	PT5B03	SA[1]	AD[23]	SD[23]	
86	I/O	8mA	PT5B03	SA[2]	AD[22]	SD[22]	
87	I/O	8mA	PT5B03	SA[3]	AD[21]	SD[21]	
88	I/O	8mA	PT5B03	SA[4]	AD[20]	SD[20]	
89	I/O	8mA	PT5B03	SA[5]	AD[19]	SD[19]	
90	I/O	8mA	PT5B03	SA[6]	AD[18]	SD[18]	
91	GNDO		PV0A	VSSO4	VSSO4	VSSO4	
92	I/O	8mA	PT5B03	SA[7]	AD[17]	SD[17]	
93	I/O	8mA	PT5B03	SA[8]	AD[16]	SD[16]	
94	I/O	8mA	PT5B03	SA[9]	C/BEn[2]	BEn[2]	
95	I/O	8mA	PT5B03	SA[10]	FRAMEn	ADSn	
96	I/O	8mA	PT5B03	SA[11]	IRDYn	SRDYIn	
97	I/O	8mA	PT5B03	SA[12]	TRDYn	SRDYn	
98	I/O	8mA	PT5B03	SA[13]	DEVSELn	ISACMD	
99	I/O	8mA	PT5B03	SA[14]	STOPn	WRn	
100	I/O	8mA	PT5B03	SA[15]	LOCKn	MIOn	
101	I/O	8mA	PT5B03	SA[16]	C/BEn[1]	BEn[1]	
102-108	I/O	24mA	PT5B04	SD[15:9]	AD[15:9]	SD[15:9]	
109	GNDO		PV0A	VSSO5	VSSO5	VSSO5	
110	I/O	8mA	PT5B04	SD[8]	SD[8]	SD[8]	
111	I/O	8mA	PT5B03	AEN	C/BEn[0]	BEn[0]	
112-115	I/O	24mA	PT5B04	SD[7:4]	AD[7:4]	SD[7:4]	
116	VDDB		PVDF	VDD2	VDD2	VDD2	
117-120	I/O	24mA	PT5B04	SD[3:0]	AD[3:0]	SD[3:0]	
121	GNDO		PV0A	VSSO6	VSSO6	VSSO6	
122	O	4mA	PT5O02	WEAn/CASAn	WEAn/CASAn	WEAn/CASAn	
123-130	I/O	2mA	PT5B01	MD[0:7]	MD[0:7]	MD[0:7]	
131	O	4mA	PT5O02	WEBn/CASBn	WEBn/CASBn	WEBn/CASBn	
132-139	I/O	2mA	PT5B01	MD[8:15]	MD[8:15]	MD[8:15]	
140	GNDO		PV0A	VSSO7	VSSO7	VSSO7	
141	O	4mA	PT5O02	WECn/CASCn	WECn/CASCn	WECn/CASCn	
142-149	I/O	2mA	PT5B01	MD[16:23]	MD[16:23]	MD[16:23]	

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150	O	4mA	PT5O02	WEDn/CASDn	WEDn/CASDn	WEDn/CASDn	
151-152	I/O	2mA	PT5B01	MD[24:25]	MD[24:25]	MD[24:25]	
153	VDDB		PVDF	VDD3	VDD3	VDD3	
154-159	I/O	2mA	PT5B01	MD[26:31]	MD[26:31]	MD[26:31]	
160	GNDO		PV0A	VSSO8	VSSO8	VSSO8	
161	O	8mA	PT5O03	RASLn	RASLn	PASLn	
162	O	8mA	PT5O03	CASLn/WELn	CASLn/WELn	CASLn/WELn	
163-170	O	8mA	PT5O03	MA[0:7]	MA[0:7]	MA[0:7]	
171	O	8mA	PT5O03	CASHn/ WEHn/MA[8]	CASHn/ WEHn/MA[8]	CASHn/ WEHn/MA[8]	
172	O	8mA	PT5O03	RASHn/MA[9]	RASHn/MA[9]	RASHn/MA[9]	
173	O	4mA	PT5O02	WEEn/CASEn	WEEn/CASEn	WEEn/CASEn	
174-180	I/O	2mA	PT5O01	MD[32:38]	MD[32:38]	MD[32:38]	
181	GNDO		PV0A	VSSO9	VSSO9	VSSO9	
182	I/O	2mA	PT5B01	MD[39]	MD[39]	MD[39]	
183	O	4mA	PT5O02	WEFn/CASFn	WEFn/CASFn	WEFn/CASFn	
184-191	I/O	2mA	PT5B01	MD[40:47]	MD[40:47]	MD[40:47]	
192	GNDI		PV0B	VSSI1	VSSI1	VSSI1	
193	O	4mA	PT5O02	WEGn/CASGn	WEGn/CASGn	WEGn/CASGn	
194-195	I/O	2mA	PT5B01	MD[48:49]	MD[48:49]	MD[48:49]	
196	I		PT5D01+ PC5C01	MCLK	MCLK	MCLK	
197-198	I/O	2mA	PT5B01	MD[50:51]	MD[50:51]	MD[50:51]	
199	VDDB		PVDF	VDD4	VDD4	VDD4	
200-203	I/O	2mA	PT5B01	MD[52:55]	MD[52:55]	MD[52:55]	
204	O	4mA	PT5O02	WEHn/CASHn	WEHn/CASHn	WEHn/CASHn	
205	I/O	2mA	PT5B01	MD[56]	MD[56]	MD[56]	
206	GNDO		PV0A	VSSO10	VSSO10	VSSO10	
207-213	I/O	2mA	PT5B01	MD[57:63]	MD[57:63]	MD[57:63]	
214	O	2mA	PT5O01	DACWRn	DACWRn	DACWRn	
215	O	2mA	PT5O01	DACRDn	DACRDn	DACRDn	
216	I		PT5D01U	ESYNC	ESYNC	ESYNC	
217	O	4mA	PT5T02	BLANKn	BLANKn	BLANKn	
218	O	8mA	PT5T03	VSYNC	VSYNC	VSYNC	
219	O	8mA	PT5T03	HSYNC	HSYNC	HSYNC	
220	I		PT5D01U	EPCLK	EPCLK	EPCLK	
221	O	8mA	PT5T03	PCLK	PCLK	PCLK	
222	I		PT5D01U	EPDATA	EPDATA	EPDATA	
223	VDDB		PVDF	VDD5	VDD5	VDD5	
224-229	O	8mA	PT5T03	P[15:10]	P[15:10]	P[15:10]	
230	GNDO		PV0A	VSSO11	VSSO11	VSSO11	
231-240	O	8mA	PT5T03	P[9:0]	P[9:0]	P[9:0]	

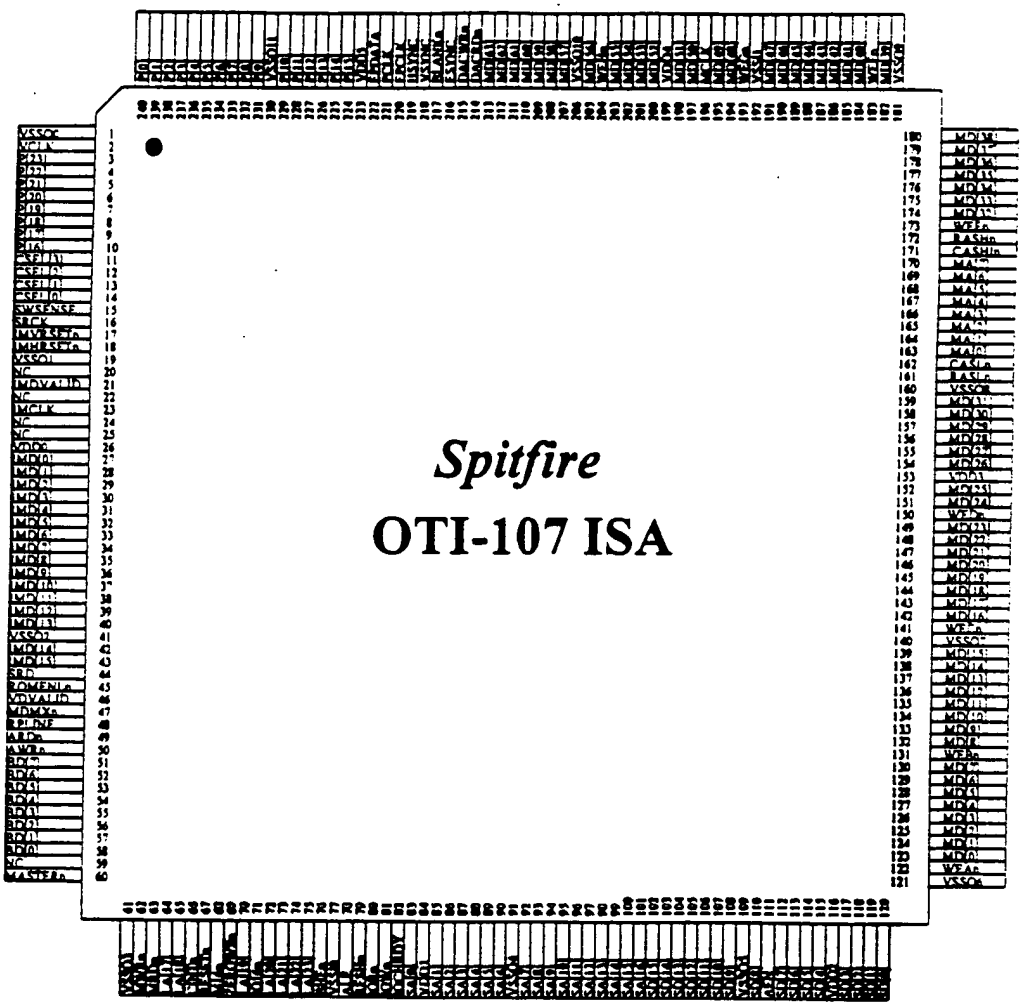
* Only pins with different definition option in revision B are listed in these two columns.

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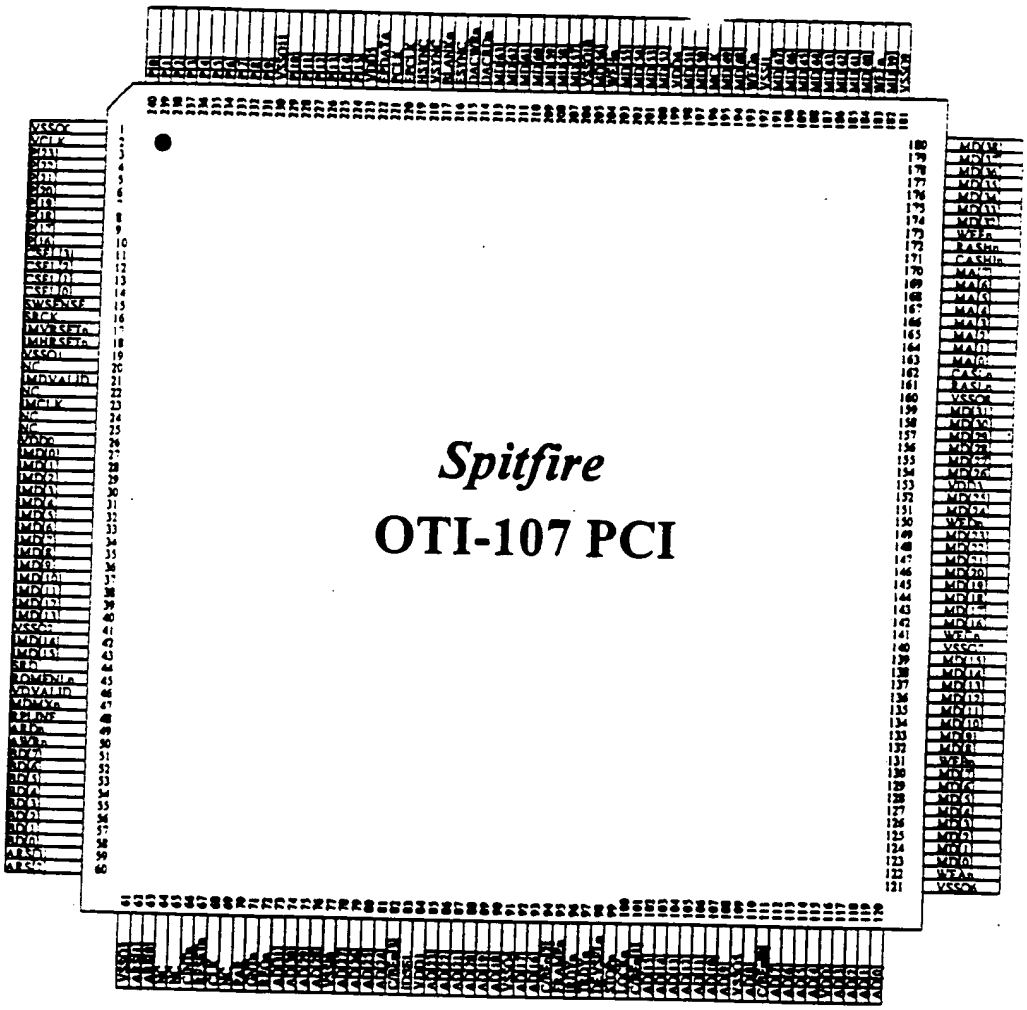
5.18 Pin Diagram

5.18.1 ISA Bus Pin Diagram - 240 Pins



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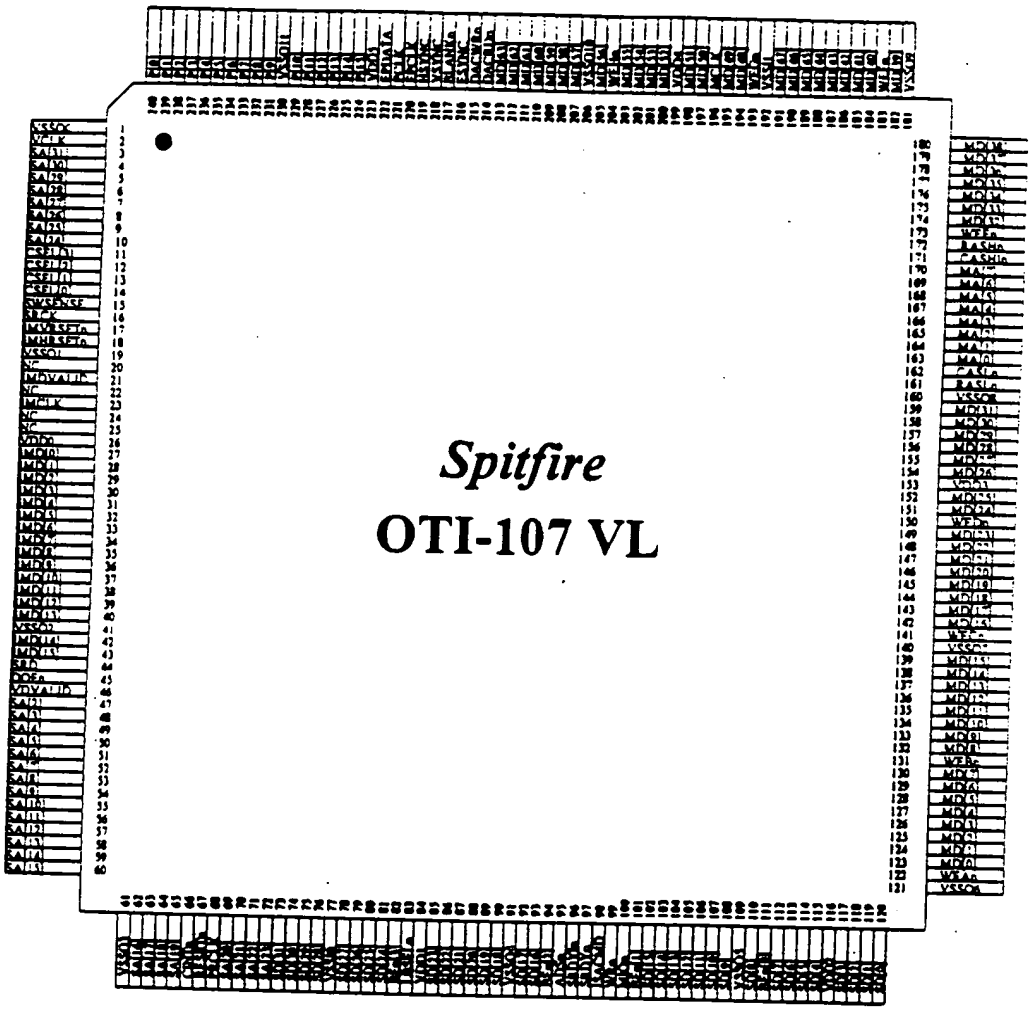
5.18.2 PCI Bus Pin Diagram - 240 Pins



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5.18.3 VL Bus Pin Diagram - 240 Pins



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5.19 Imaging Connector

There are two version of imaging connector: 1) OAK's proprietary connector which exists for all revisions of OTI-107, and 2) VMC connector which exists for revision B and later revisions of OTI-107. The connector is a 68-pin high density type, uulizing 0.050" pin spacing. The part number is 5-175473-8 made by AMP or equivalent.

OAK IMAGING CONNECTOR	PIN NUMBER	VMC CONNECTOR/ OTI-107 PINS
SRCK	1	SAn / SAn
NC	2	NC
NC	3	NC
GND	4	GND
IMVRSETn	5	BSn[0]/BSn[0]
IMHRSETn	6	BSn[1]/BSn[1]
GND	7	GND
NC	8	SNRDYn/SNRDYn
IMDVALID	9	CONTROL/CNTRL
GND	10	GND
NC	11	RESETn/IRESETn
GND	12	GND
IMCLK	13	DCLK/IMCLK
GND	14	GND
NC	15	NC
GND	16	GND
NC	17	M0/MASK[0]
NC	18	M1/MASK[1]
GND	19	GND
IMD[0]	20	P0/IMD[0]
IMD[1]	21	P1/IMD[1]
GND	22	GND
IMD[2]	23	P2/IMD[2]
IMD[3]	24	P3/IMD[3]
GND	25	GND
IMD[4]	26	P4/IMD[4]
IMD[5]	27	P5/IMD[5]
GND	28	GND
IMD[6]	29	P6/IMD[6]
IMD[7]	30	P7/IMD[7]
GND	31	GND
NC	32	P8
NC	33	P9
GND	34	GND

OAK IMAGING CONNECTOR	PIN NUMBER	VMC CONNECTOR/ OTI-107 PINS
NC	35	P10
NC	36	P11
GND	37	GND
NC	38	P12
NC	39	P13
GND	40	GND
NC	41	P14
NC	42	P15
GND	43	GND
IMD[8]	44	P16/IMD[8]
IMD[9]	45	P17/IMD[9]
GND	46	GND
IMD[10]	47	P18/IMD[10]
IMD[11]	48	P19/IMD[11]
GND	49	GND
IMD[12]	50	P20/IMD[12]
IMD[13]	51	P21/IMD[13]
GND	52	GND
IMD[14]	53	P22/IMD[14]
IMD[15]	54	P23/IMD[15]
GND	55	GND
NC	56	P24
NC	57	P25
GND	58	GND
NC	59	P26
NC	60	P27
GND	61	GND
NC	62	P28
NC	63	P29
GND	64	GND
NC	65	P30
NC	66	P31
GND	67	GND
SRD	68	SBn

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6 OTI-107 REGISTER DEFINITION

6.1 Register Revision History

6/21/93	Last released
8/2/93	ER0F[1:0] - added for power management
	ER10[3] - becomes reserved
	ER13[5] - this bit is removed. Use CFR30[0] instead.
	ER14[4] - added for 8M aperture
	ER20[7:6] - change definition for ease of design
	ER22[5] - added for write mode 4
	ER28[1:0] - remove 0 refresh condition
	ER33 - added default value
	CFR30[0] - changed from read-only to read/writeable
	HR9A-98 - change mapping description
	PR11[1] - added for master mode/CPU assist selection
	PR11[4:2] - status added CPU assisted mode
	PR18 - change description to -1, changed from 16-bit to 12-bit
	PR1A - change description to -1, changed from 16-bit to 12-bit
	PR20, PR24, PR28 - changed from 16-bit to 14-bit
	PR2C - add more description
	PR4A[2:0] - change ordering of function, add default value
	PR60, PR62, PR70, PR72, PR74, PR76 - changed from 16-bit to 12-bit
	PR6C, PR6E, PR78, PR7A - changed from 16-bit to 13-bit
8/27/93	ERC - dip switch moved to ERD, this register becomes scratch
	ERD - added for dipswitch
	ER15[7:6] - added for memory/memory mapped I/O to share address space
	CFR4 - default is changed from 'hA3 to 'hA0
	CFRE - added for multi-function PCI device
	CFR14[22:20] - these bits are now writeable in VL & ISA bus configuration
	CFR18 - is only 32-bit, ie CFR 1B-18, it's used to be 21-18
	CFR27-1C - these are reserved
	PR10 - added for cpu assisted blit
	PR11[7:6,4:2] - these bits have been moved to PR10, new definition for bits 7:6
9/10/93	HRA0[15:0] - added for line lenght of MM input
	ER10[7:4] - changed definition of wait states
10/25/93	HRA0 - deleted and replaced with IMHRSETn
	ER3 - new register definition for testing & debugging sequencer
	ER8[7:6] - added for auto configuration with VL bus using ID bits.
	ER8[1] - new definition
	ER9,A,B,C - moved to F0,F1,F2,F3
	ER9[1:0] - new definition and reserved for configuraiton 3
	ERC - now used for I²C control
	ERF[2] - added to disable IMCLK for power saving purpose
	ERF4-7 - added for scratch
	CFR6[10:9] - changed hardware configuration bit
	CFRE[7] - changed hardware configuraiton bit
	ER10[1] - becomes reserved
	ER29[2] - becomes reserved
	ER33[2:1] - become reserved
	PR11[7] - removed
	PR11[6] - invert definition
	PR7C[27:24] - added *TextBlt* mode for text output

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6.2 Convention

Convention for the registers are as followed

readport/writeport	register name	index	read/write

Default - some registers or register bits should be reset or preset to the default value at boot-up time. Hardware reset (come from reset pin, as oppose to software reset which is generated from sequencer reset register) should be used to set or preset these registers. Registers with no default values are not initialized during reset, and should be initialized by software before reading their contents.

Reserved - reserved bits should be implemented with tristate buffers only to save gates, and should always return 0 when read.

AR - attribute controller registers: 3C0, 3C1

CR - CRT controller registers: 3B4, 3B5, 3D4, 3D5

CFR - Configuration registers for PCI bus: 0-3C

ER - extended registers: 3DE, 3DF

GR - graphics controller registers: 3CE, 3CF

HR - hardware cursor registers: memory mapped

PR - co-processor registers: memory mapped

SR - sequencer registers: 3C4, 3C5

R/W - register is readable and writeable

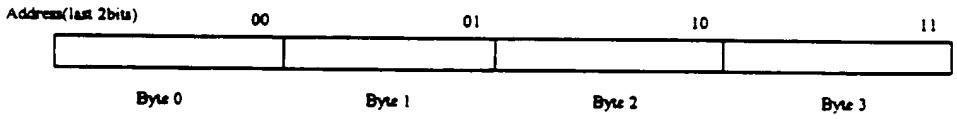
RO - register is read only

WO - register is write only

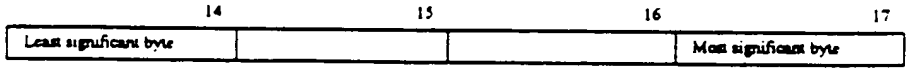
xRii[xx] - xR stands for register name, ii stands for index, [xx] represents bit number. For example, SR1[2:5,7] stands for sequencer register index 1 bits 2 through 5 and bit 7.

3?X - the "?" here stands for "B" if in monochrome emulation modes, and "D" if in color emulation modes as determined by bit 0 of Miscellaneous Output Register.

Register Order:



Example: Pixel Map n Base Address Register



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6.3 Enable Registers

There are two registers that control the enable/disable mechanism of the OTI-107 product on ISA and VL bus. One register controls access to the on-board video subsystem and the other register controls access to the add-on video subsystem. The OTI-107 chip contains both add-on and on-board registers. The register that control on-board operation may also reside in the system chipset or on the motherboard. The addresses for both register sets are:

Add-on configuration: 46E8 enable/disable (in OTI-107)

On-board configuration: 3C3 enable/disable (in OTI-107 and in some system chip set)

The setup/enable register sets 46E8/102 and 94/102 will not be implemented in this chip because of potential I/O conflict with system chip set. Only enable registers 46E8 and 3C3 are implemented.

46E8 Add-on Enable Register **R/W**

This register serves as the POS (power on setup) equivalent on MCA machines.

Bit	Description
2-0	Reserved.
3	0: Disable read/write access to OTI-107 registers, DAC registers, and video memory. 1: Enable read/write access to OTI-107 registers, DAC registers, and video memory (normal operational mode).
7-4	Reserved.

Default: 'h0

3C3 On-board Enable Register **WO**

This register may also reside inside some system chipsets. To avoid possible conflict, this register must be able to be written in one clock (zero wait state), signals LBSELn and SRDYn should not be asserted. SRDYn should be asserted by system chipset because either it has 3C3 or it has to pass this I/O cycle to the ISA bus.

Bit	Description
0	0: Disable read/write access to OTI-107 registers, DAC registers, and video memory. 1: Enable read/write access to OTI-107 registers, DAC registers, and video memory (normal operational mode).
7-1	Reserved.

Default: 'h0

For PCI bus, enable/disable are done through Configuration Register 4 bits 1:0 for both add-on and on-board. 46E8[3] and 3C3[0] are logically ORed with CFR4[1:0], thus either 46E8/3C3 or CFR4 can be used to enable, but both must be off to disable. Since all three registers are off at boot-up (hardware reset), only one set of registers is needed to complete the enable/disable function.

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6.4 Extended Register Summary

The OTI-107 extended registers are NOT downward compatible with any of the previous chip. New registers are defined in the OTI-107 to support enhanced functions and features which provide flexibility for different VGA configurations. A summary of these extended registers is given below.

Extended General Registers

Register Port	R/W	Port	Index	Bits	Block
Extension Address Register	R/W	3DE		8	BI
Status Register	R/W	3DF	2	3	BI
OTI Test Register 1	R/W	3DF	3	8	BI
OTI Test Register 2	R/W	3DF	4	0	BI
Clock Select Register/Scratch	R/W	3DF	6	8	BI
Configuration Register 1	RO	3DF	7	8	BI
Configuration Register 2	RO	3DF	8	8	BI
Configuration Register 3	RO	3DF	9	0	BI
I^2C Control Register	R/W	3DF	C	4	BI
Dip Switch Read	RO	3DF	D	8	BI
EEPROM Control Register	R/W	3DF	E	4	BI
Power Saving Register	R/W	3DF	F	3	CRT
Scratch Register 0	R/W	3DF	F0	8	BI
Scratch Register 1	R/W	3DF	F1	8	BI
Scratch Register 2	R/W	3DF	F2	8	BI
Scratch Register 3	R/W	3DF	F3	8	BI
Scratch Register 4	R/W	3DF	F4	8	BI
Scratch Register 5	R/W	3DF	F5	8	BI
Scratch Register 6	R/W	3DF	F6	8	BI
Scratch Register 7	R/W	3DF	F7	8	BI

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Extended System Interface Registers

There are two groups of Extended System Interface registers:

PCI compatible registers that locate at Configuration Register (CFR) space when on PCI bus, and at 2x00-2x3C when on ISA or VL bus. Some of the bits in these registers are good for all buses, and some are for PCI only. The "x" in the register address is reconfigurable through ER19b7:4 during hardware reset

QTI registers reside at 3DF index 10-1F for all bus configurations.

Register Port	R/W	Port/Index (ISA,VL)	CFR (PCI)	Bits	Block
Vendor ID Register	RO	2x00	0	16	BI
Device ID Register	RO	2x02	2	16	BI
System Bus Command Register	R/W	2x04	4	6	BI
System Bus Status Register	R/W		6	6	BI
Revision ID Register	RO	2x08	8	8	BI
Programming Interface Register	RO		B-9	24	BI
Cache Line Size Register	RO		C	0	BI
Latency Timer Register	R/W		D	0	BI
Header Type Register	RO		E	8	BI
Built-In Self Test Register	R/W		F	0	BI
Memory Mapped I/O Base Address Register	R/W	2x10	10	32	BI
Memory Base Address Register	R/W	2x14	14	32	BI
Auxiliary & DAC I/O Base Address Register	R/W		18	32	BI
Base Address Registers 5-3	R/W		27-1C	0	BI
Reserved Registers	RO		2F-28	0	BI
BIOS ROM Base Address Register	R/W	2x30	30	32	BI
Reserved Registers	RO		3B-34	0	BI
Interrupt Line Register	R/W	2x3C	3C	8	BI
Interrupt Pin Register	RO		3D	8	BI
Min_Gnt Register	RO		3E	8	BI
Max_Lat Register	RO		3F	8	BI
Local Bus Control 1	R/W	3DF/10		7	BI
ISA Bus Control	R/W	3DF/13		3	BI
Memory Mapping Register	R/W	3DF/14		7	BI
Memory & Memory Mapped I/O Enable	R/W	3DF/15		2	BI
Configuration/Auxiliary/DAC Address Range	R/W	3DF/19		6	BI

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Extended Sequencer Registers

Register Port	R/W	Port	Index	Bits	Block
Compatible Segment Register	R/W	3DF	11	8	SEQ
FIFO Depth Register	R/W	3DF	20	6	SEQ
Mode Select Register	R/W	3DF	21	7	SEQ
Feature Select Register	R/W	3DF	22	3	SEQ
Extended Read Segment Register	R/W	3DF	23	7	SEQ
Extended Write Segment Register	R/W	3DF	24	7	SEQ
Extended Common Read Write Register	R/W	3DF	25	7	SEQ
RASn Control Register	R/W	3DF	26	3	SEQ
CASn Control Register	R/W	3DF	27	5	SEQ
Refresh Control Register	R/W	3DF	28	3	SEQ
Hardware Window Arbitration Register	R/W	3DF	29	2	SEQ

Extended CRT Controller Registers

Register Port	R/W	Port	Index	Bits	Block
OTI CRT Overflow Register	R/W	3DF	30	4	CRTC
CRT Start Address Hi Register	R/W	3DF	31	7	CRTC
HSYNC/2 Start Register	R/W	3DF	32	8	CRTC
CRT Address Compatibility Register	R/W	3DF	33	1	CRTC

Extended Attribute Controller Registers

Register Port	R/W	Port	Index	Bits	Block
Pixel Interface Register	R/W	3DF	38	6	ATR

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Hardware Cursor/Hardware Window Registers

Register Description	R/W	Port	Offset	Bits	Block
HC/HW Horizontal Position Start	R/W		81.80	11	HC
HC/HW Vertical Position Start	R/W		83.82	11	HC
HC Horizontal Preset/HW Width Low	R/W		84	8	HC
HW Width High	R/W		85	3	HC
HC Vertical Preset /HW Height Low	R/W		86	8	HC
HW Height High	R/W		87	3	HC
HC Start Address	R/W		8A-88	24	SEQ
HC Color 0	R/W		8F-8C	32	ATR
HC Color 1	R/W		93-90	32	ATR
HC Control	R/W		94	6	HC
HW Control	R/W		96	8	HC
HW Mask Map Start Address	R/W		9A-98	24	SEQ
HW Start Address	R/W		9C-9E	24	SEQ
HW Address Offset	R/W		9F	8	SEQ

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Co-Processor Registers

Register Description	R/W	Port	Offset	Bits	Block
Co-Processor Status	RO		10	6	CP
Co-Processor Control	R/W		11	3	CP
Pixel Map Select	R/W		12	2	CP
Pixel Map n Base Pointer	R/W		17-13	32	CP
Pixel Map n Width	R/W		19,18	16	CP
Pixel Map n Height	R/W		1B,1A	16	CP
Pixel Map n Format	R/W		1C	8	CP
Bresenham Error Term	R/W		21,20	16	CP
Bresenham K1	R/W		25,24	16	CP
Bresenham K2	R/W		29,28	16	CP
Direction Steps	R/W		2F-2C	32	CP
ROP	R/W		48	8	CP
Destination Color Compare Condition	R/W		4A	3	CP
Destination Color Compare Value	R/W		4F-4C	32	CP
Pixel Bit Mask	R/W		53-50	32	CP
Foreground Color	R/W		5B-58	32	CP
Background Color	R/W		5F-5C	32	CP
Operation Dimension 1	R/W		61,60	16	CP
Operation Dimension 2	R/W		63,62	16	CP
Mask Map Origin X Offset	R/W		6D,6C	16	CP
Mask Map Origin Y Offset	R/W		6F,6E	16	CP
Source X Pointer	R/W		71,70	16	CP
Source Y Pointer	R/W		73,72	16	CP
Pattern X Pointer	R/W		75,74	16	CP
Pattern Y Pointer	R/W		77,76	16	CP
Destination X Pointer	R/W		79,78	16	CP
Destination Y Pointer	R/W		7B,7A	16	CP
Pixel Operations	R/W		7F-7C	32	CP

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6.5 Extended Register Description

6.5.1 Extended General Registers

3DE Extension Address Register R/W

Bit	Description
7-0	8-bit index pointer to the extended data registers. The content of this register needs to be programmed before the data register can be accessed.

3DF Status Register **Index = 2** R/W

Bit	Description
0	Reserved.
3-1	Memory size.

Bits 3-1	Memory Available
000	256K bytes
001	512K bytes
010	1M bytes
011	2M bytes
100	4M bytes
101	8M bytes

These bits are initially set to 'hA at power up, then set to proper value by BIOS, depending on how much memory is detected.

7-4 Reserved.

Default: 'h0A

3DF OTI Test Register 1 **Index = 3** R/W

Bit	Description
2-0	Test mode - These bits defined the test modes of the controller. Test mode is turned on by bit 7.

Bits 2-0	Test mode
0	CRT Counter testing. When in this mode, CRT counters are muxed out to pins SD[15:0]. An internal 3-bit counter is used to mux out the CRT counters' content

Internal Count	Tested Counter
000	Vertical Counter
001	Upper 3 bits of Vertical counter & RSC[4:0]
010	Vertical Counter
011	CRT address counter bits 7:0
100	CRT address counter bits 15:8
101	CRT address counter bits 22:16
110	Horizontal Counter
111	Horizontal Counter

1	Reserved.
2	Reserved.
3	Reserved.
4	Scan Test for Bypass mode.
5	Scan Test Attribute Controller. This bit forces the font data and attribute date to be replaced by the system data bus 15:8 and 7:0 respectively in text mode. In graphic mode, this bit replaces the APA data with system data bus 15:8.
6	Reserved.
7	Reserved.

3 Reserved.

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4 Flush write cache . This bit is used for chip testing.
0: Normal cache operation.
1: Flush write cache immediately after each memory write cycle.

5 Vsync Test. This bit will cause the vsync to toggle when it is changed from 1 to 0 or from 0 to 1

6 Enable debugging mode. When debugging mode is enabled, internal signals would be routed out to pins P[23:16]. The muxing selection of internal signals are defined by bits 2:0 of this register
0: Normal operation.
1: Enable debugging mode.

Bits 2-0	Test mode
000	CRT address for text mode (Font)
001	CRT address of graphic mode
010	CPU interface to Sequencer
011	Co-processor interface to Sequencer
100	Hardware window/cursor interface to Sequencer
101	Refresh address
110	Multimedia interface to Sequencer
111	Reserved

The pin muxing is as follow:

P[23:21]	P[20:18]	P[17]	P[16]
Address source	Internal states	Frame signal	Command to Sequencer

7 Enable test mode. Test mode is used for chip testing only.
0: Normal operation.
1: Enable global test modes. This bit must be 0 during normal operation.

Default: 'h00.

3DF OTI Test Register 2 **Index = 4** **R/W**

Bit	Description
7-0	Reserved for co-processor testing.

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3DF Video Clock Select Register Index = 6 R/W

Bit	Description
3-0	Video Clock Select. The state of these 4 bits are reflected in the pins CSEL[3:0]. Bits 1-0 of this register are the images of bits 3-2 of register 3C2. bit 2 of this register is the image of bit 5 of extended register D. See frequency tables for more details. These frequency tables reflect OTI-068 & OTI-088 only. Future OTI clock chips may have different frequencies
7-4	Scratch bits for BIOS used.

Frequency table for OTI-068

CSEL3	CSEL2	CSEL1	CSEL0	CLOCK (MHz)
0	0	0	0	25.2
0	0	0	1	28.3
0	0	1	0	65
0	0	1	1	44.9
0	1	0	0	28.3
0	1	0	1	36
0	1	1	0	40
0	1	1	1	36
1	0	0	0	25.2
1	0	0	1	28.3
1	0	1	0	78
1	0	1	1	65
1	1	0	0	63
1	1	0	1	72
1	1	1	0	40
1	1	1	1	50

Frequency Table for OTI-088

CSEL3	CSEL2	CSEL1	CSEL0	CLOCK (MHz)
X	X	0	0	Programmable/25.2
X	X	0	1	Programmable
X	X	1	0	Programmable
X	X	1	1	Programmable

Software reset must be executed each time this register is updated.

Default: 'hx0

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3DF Hardware Configuration Register 1 **Index = 7** **RO**

Bit	Description
0	This bit is used by hardware to determine ROM data width on the board and route the data out to system bus appropriately. This bis is used with ISA and PCI bus only. See ROM BIOS Interface for detail descriptions. 0: 8-bit BIOS (1 ROM) 1: 16-bit BIOS (2 ROM's)
1	On-board/add-on configuration. 0: on-board configuration. Enable chip through 3C3 1: add-on configuration. Enable chip through 46E8
4-2	Bus Types. These bits define the system bus configuration of the controller. Bits 3&2 should be derived from VL bus ID pins 1&0, respectively

Bits 4:2	Bus Type
000	Reserved for VL bus
001	386 VL bus
010	486 VL bus
011	486 VL bus
100	PCI bus
101	Reserved
110	Reserved
111	ISA bus

7-5 DRAM type. These bits define the type of DRAM used.

Bits 7-5	Dram type
000	64KxXX
001	256Kx16$_{10c3}$
010	256Kx4, 256Kx16$_{9c3}$
011	512Kx8
100	1Mx4
111	Reserved

The content of this register is loaded from MD[7:0] during hardware reset.
Note: For compatibility with future revisions, all reserved bits should be tied low through resistors.

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3DF Hardware Configuration Register 2 **Index = 8** **RO**

Bit	Description
0	Pixel bus width status Used by BIOS to determine the pixel bus width of the external DAC 0: 8-bit pixel bus. 1: 16-bit pixel bus.
1	Enable Auxiliary I/O support on VL bus. This bit does not apply to PCI or ISA bus. 0: normal operation. OTI-107 generates DACRDn and DACWRn. 1: enable auxiliary I/O. OTI-107 generates DACCSn & ACSn instead of DACRDn & DACWRn
2	Enable decoding for ROM BIOS 0: Disable decoding for ROM BIOS 1: Enable decoding for ROM BIOS (default address is C0000)
4-3	ROM BIOS size. Bits 4-3 — ROM BIOS size 00 — 32 Kbytes 01 — 64 Kbytes 10 — 128 Kbytes 11 — 256 Kbytes
5	CASxn/Wexn select. For x16 DRAM's, either CASn & WEHn & WELn, or CASHn & CASLn & WEn, both can be supported. This bit is used to select which type is selected. 0: CASn, WEHn & WELn 1: CASHn, CASLn & WEn
6	Fast Write Capable. This bit is used to indicate whether motherboard can handle zero wait write. This bit should be connected to ID[2] of the VL bus through a LS244 buffer. This bit can also be read at ER10[1]. ER10[1] can be written over, while this bit is read only. 0: motherboard can not handle zero wait - delay internal ADS/FRAME to push memory write cycle back by one clock. Data is latched at the end of second T2, or one clock after IRDYn. 1: no additional wait state for the cycle.
7	Bus speed. This bit is for BIOS to determine the bus speed, and therefore determine the appropriate wait states to insert. This bit should be connected to ID[3] of VL bus through a LS244 buffer. 0: bus speed is greater than 33MHz 1: bus speed is less than or equal to 33MHz.

The content of this register is loaded from MD[15:8] during hardware reset.
Note: For compatibility with future revisions, all reserved bits should be tied low through resistors.

3DF Hardware Configuration Register 3 **Index = 9** **RO**

Bit	Description
0	DEVSELn speed indication. OTI-107 can only be medium or slow response, but never fast. 0: forces CFR[10:9] to 01, medium response. 1: forces CFR[10:9] to 10, slow response.
1	Multi-function device selection for PCI bus. This bit can also be read at CFRE[7]. 0: sigle function device (forces CFRE[7] to 0). 1: multiple function device (forces CFRE[7] to 1).
7-2	Reserved.

The content of this register is loaded from MD[23:16] during hardware reset.
Note: For compatibility with future revisions, all reserved bits should be tied low through resistors.

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3DF I²C Control Register **Index = C** **R/W**

Bit	Description
0	Controls pin SRCK. 0: Drives pin SRCK low 1: Drives pin SRCK high
1	Controls pin SRD. 0: Drives pin SRD low 1: Drives pin SRD high
3-2	Reserved.
4	Status of pin SRCK. This bit is read only.
5	Status of pin SRD. This bit is read only.
7-6	Reserved.

Default: 'h0

3DF Dip Switch Register **Index = D** **RO**

Bit	Description
7-0	Dip switch status register. For BIOS used.

3DF EEPROM Control Register **Index = E** **R/W**

Bit	Description
0	EEPROM Data. This bit is the data line between the serial EEPROM and the VGA controller. The read data for this bit comes from CSEL[0]. Write data is send to CSEL[1]. CSEL[0] and CSEL[1] are connected to the EEPROM data out and the EEPROM data in pins respectively.
1	EEPROM CS. This bit is used as the chip select control for the EEPROM. It should be set to 1 for the VGA controller to access the EEPROM.
2	EEPROM Function Enable. This bit selects the function of the CSEL bus. When this bit is 1, CSEL[2:0] are used to interface with the EEPROM. When this bit is 0, the CSEL[2:0] funcuons as clock select signals.
3	EEPROM Clock(SK). The value of this bit which acts as the shift clock for the serial EEPROM is reflected on CSEL[2]. To program the EEPROM, this bit is programmed to toggle between 1 and 0 every 4us .
7-4	Reserved.

Default: 'h0

3DF Power Management Control Register **Index = F** **R/W**

Bit	Description
1-0	Display Power Management Modes. When in any of the power saving modes, memory controller stops fetching data for display (same as screen-off bit SR1b5) but continue to refresh DRAM. Bits 1-0 — Modes 00 — On - HSYNC, VSYNC, BLANKn, P[23:0] operate normally. 01 — Stand-by - VSYNC operates normally, HSYNC, BLANKn & P[23:0] off 10 — Suspend - HSYNC operates normally, VSYNC, BLANKn & P[23:0] off 11 — Off - HSYNC, VSYNC, BLANKn & P[23:0] off
2	Enable Imaging clock. 0: Disable imaging clock 1: Enable imaging clock
7-3	Reserved.

Default: 'h0

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3DF Scratch Registers 0-7 **Index = F0-F7** **R/W**

Bit	Description
7-0	8 scratch bits. These scratch registers are defined and reserved for internal use. Application programs should not use them.

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6.5.2 System Interface Registers

All 2xxx registers are PCI Configuration registers that can be used for other buses. On ISA or VL bus, these registers can be accessed at 2xxx, but they can only be accessed through configuration read/write on PCI bus. PCI Configuration registers only do not have 2xxx address and only respond to configuration cycle.

2x00 Vendor ID Register **CFR = 1,0** **RO**

Bit	Description
15-0	Vendor Identification used with PCI bus. The value is 104E.

2x02 Device ID Register **CFR = 3,2** **RO**

Bit	Description
15-0	Device Identification

Bits 15-0	Product
'h0107	OTI-107

2x04 System Bus Command Register **CFR = 5,4** **R/W**

Bit	Description
0	Enable I/O accesses. This bit is used for PCI bus only. 0: Disables all I/O space accesses. 1: Enables I/O space accesses.
1	Enable memory and memory mapped I/O accesses. Both this bit and 3C2[1] need to be 1's to enable memory accesses to the controller. 0: Disables all memory space accesses. 1: Enable memory space accesses.
2	Enable bus master mode. This bit is used for PCI bus only. 0: Disable bus master mode. 1: Enable bus master mode.
4-3	Reserved.
5	Enable bus snooping for palette registers. 0: Respond to palette register writes like ordinary I/O 1: Complete all palette register writes without asserting DEVSELn (LBSELn), allowing the cycle to propagate out to the standard ISA bus for other devices to shadow these registers.
6	Reserved.
7	Enable address/data stepping. This bit is used for PCI bus only. 0: Disable address/data stepping. 1: Allow address/data to be driven out in more than one clock.
8	Reserved.
9	Back-to-back cycle capable. This bit is used when the controller is in Master mode and on PCI bus only. Back-to-back cycles are transactions from one master to the same target without IDLE cycle in between. For revision A, this bit is not used, but it should be read/writeable. 0: Do not issue back-to-back cycle. 1: All target devices can accept back-to-back cycle.
15-10	Reserved.

Default: 'h00A0

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System Bus Status Register **CFR = 7,6** **R/W**

Read to this register behave normally. Writes are different in that writeable bits can only be reset, but not set. A bit is reset whenever a 1 is written to that particular bit. For example, to clear bit 14 and not effect any other bits, write the value 'h4000 to the register.

Bit	Description
6-0	Reserved.
7	Fast Back-to-Back Capable. This bit is read-only and default to 1 0: Not capable of fast back-to-back cycle **1: Capable of fast back-to-back cycle**
8	Reserved.
10-9	DEVSELn timing. These two bits are read only and are configurable through MD[16] during hardware reset. MD[16]=0 => CFR6[10:9]='b01, MD[16]=1 => CFR6[10:9]='b10. MD[16] state during reset can be read through ER9[0].

Bits 10-9	DEVSELn Timing
00	Fast
01	**Medium**
10	Slow
11	Reserved

11	Signaled Target-abort status. This bit is set whenever the OTI-107 while being a target device, terminates a transaction with target-abort.
12	Received Target-abort status. This bit is set whenever the OTI-107 while being a master, has its transaction terminates with target-abort.
13	Received Master-abort status. This bit is set whenever the OTI-107 while being a master, terminates its transaction (except for Special cycle) with master-abort.
15-14	Reserved.

Default: 'b00000xx010000000

2x08 Revision ID Register **CFR = 8** **RO**

Bit	Description
7-4	Chip functional revision. Chip revision only changes when there is a functional difference. The first revision is A.

Bits 7-4	Revision Letter
0000	A

3-0	Chip foundry revision. Chip foundry revision changes for each foundry tape out and/or library changes.

Bits 3-0	Revision Number
0000	0 - TSMC OASC672

Class Code Register **CFR = B,A,9** **RO**

Bit	Description
23-0	Register class encoding for backward compatibility.

Bits 23-0	Register class
'h000000	All currently implemented devices except for VGA compatible devices
'h030000	**VGA compatible devices**

Cache Line Size Register **CFR = C** **RO**

Bit	Description
7-0	Reserved.

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Latency Timer **CFR = D** **R/W**

Bit	Description
7-0	Specifies, in unit of PCI bus clocks, the value of the Latency Timer for OTI-107 while being a master. Bits 7-3 are read and writeable. Bits 2-0 are read only.

Default: 'h0

Header Type **CFR = E** **RO**

Bit	Description
6-0	Always zero's to indicate current offset for configuration register.
7	Multi-function device indicator. This bit is read only, but configurable through MD[17] during reset. Reset is used to latch in the value of MD[17] and data is routed to this bit. 0: single function device 1: multiple function device

Built-In Self Test Register **CFR = F** **RO**

Bit	Description
7-0	Reserved.

2x10 **Memory Mapped I/O Base Address (0) Register** **CFR = 13-10** **R/W**

Bit	Description
0	Memory or I/O indication. This bit is read only. **0: Memory mapped** 1: I/O mapped
2-1	Locatable area indication. These two bits are read only.

Bits 2-1	Locatable area
00	**Locate anywhere in 32-bit address space**
01	Locate below 1 Meg
10	Locate anywhere in 64-bit address space
11	Reserved

3	Prefetchable indication. This bit is read only **0: Memory is not prefetchable (not cacheable)** 1: Memory is prefetchable (cacheable)
7-4	Always zero's to occupy 256 bytes of address space. These bits are read only.
31-8	Upper 24 bits of the base address for memory mapped I/O. These bits are read-writeable.

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2x14 Graphic Memory Base Address (1) Register **CFR = 17-14** **R/W**

Bit	Description
0	Memory or I/O indication. This bit is read only. **0: Memory mapped** 1: I/O mapped
2-1	Locatable area indication. These two bits are read only. Bits 2-1 — Locatable area 00 — **Locate anywhere in 32-bit address space** 01 — Locate below 1 Meg 10 — Locate anywhere in 64-bit address space 11 — Reserved
3	Prefetchable indication. This bit is read only **0: Memory is not prefetchable (not cacheable)** 1: Memory is prefetchable (cacheable)
19-4	Always zero's to occupy at least 1Megabytes of memory address space. These bits are read only.
22-20	Always zero's and read only on PCI bus to occupy a block of 8 Megabytes of address space. On VL and ISA, however, these bits are read/writeable so that graphic memory can be located at 1 Megabytes incrementation.
31-23	Upper 9 bits of the base address for video memory. These bits are read-writeable.

Extended I/O Base Address (2) Register **CFR = 1B-18** **R/W**

Bit	Description
0	Memory or I/O indication. This bit is read only. 0: Memory mapped **1: I/O mapped**
1	Reserved.
3	Prefetchable indication. This bit is read only **0: Memory is not prefetchable (not cacheable)** 1: Memory is prefetchable (cacheable)
7-4	Always zero's to occupy minimum of 256 bytes of address space. These bits are read only.
31-8	Upper 24 bits of the base address for video memory. These bits are read-writeable.

Base Address 5-3 **CFR = 27-1C** **RO**

Bit	Description
31-0	Reserved.

Reserved Registers **CFR = 3B-34,2F-28** **RO**

Bit	Description
31-0	Reserved.

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2x30 BIOS ROM Base Address Register **CFR = 33-30** **R/W**

Bit	Description
0	BIOS ROM address decode enable. This bit is read/writeable only. 0: Disable address decode for BIOS ROM. 1: Enable address decode for BIOS ROM.
10-1	Reserved.
14-11	Always zero's to indicate that the BIOS ROM is minimally 32 Kbytes. These bits are read only
17-15	These bits are used to indicate how big the ROM BIOS is. These bits are either reset to 0's and read only, or read-writeable depending on Configuration Register 2 bits 4-3

ER8[4:3]	ROM size	RO or R/W
00	32 Kbytes	Bits 17-15 are read-writeable
01	64 Kbytes	Bits 17-16 are read-writeable, bit 15 is always 0 and RO
10	128 Kbytes	Bit 17 is read-writeable, bits 16-15 are always 0's and RO
11	256K bytes	Bits 17-15 are always 0's and RO

31-18 Upper 14 bits of the base address for BIOS ROM.
Default: 'h000C0001

2x3C Interrupt Line Register **CFR = 3C** **R/W**

Bit	Description
7-0	This is a scratch pad for POST software to write the interrupt line routing information during initialization and configuration of the system (PCI bus). Device drivers and OS's can use this information to determine priority and vector information. Non PCI BIOS may use this register as a general purpose scratch register in addition to registers 3DF index 9,A & B.

Interrupt Pin Register **CFR = 3D** **RO**

Bit	Description
7-0	This register indicates which interrupt pin is used by the OTI-107. The value of this register should be 01. This interrupt is for CINTn

Min_Gnt Register **CFR = 3E** **RO**

Bit	Description
7-0	This register is used to indicate to the system how long a burst period the OTI-107 need. The value of this register should be FF (maximum allowed)

Max_Lat Register **CFR = 3F** **RO**

Bit	Description
7-0	This register is used to indicate to the system how often the OTI-107 needs to get access to the PCI bus. The value of this register should be 01 (very often)

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3DF Local Bus Control Register 1 **Index = 10** **R/W**

Bit	Description
0	Wait state control. This bit delays internal ADS/FRAME to push all cycles back by one clock. This bit affects all I/O, memory mapped I/O and memory cycles. This bit works independently from other wait state bits. The total wait states for a cycle is equal to the individual wait state plus this wait. 0: No additional wait state asserted 1: One wait state asserted.
1	Reserved.
2	Memory write wait state. This bit delays SRDYn/TRDYn by one clock on memory write cycle 0: no additional wait state for the cycle. 1: one wait state is inserted for the cycle.
3	Reserved.
5-4	Memory mapped I/O wait state. These bits delay SRDYn/TRDYn by the specified amount of clocks on memory cycles for the memory mapped I/O.

Bits 5,4	Read Wait State	Write Wait State
00	1	0
01	2	1
10	3	2
11	4	3

7-6	I/O wait state. These bits delay SRDYn/TRDYn by the specified amount of clocks on I/O cycles.

Bits 5,4	Wait State
00	1
01	2
10	3
11	4

Default: 'hF5

3DF ISA Bus Control Register **Index = 13** **R/W**

Bit	Description
2-0	Reserved.
3	0: Disable zero wait state ISA bus operation. 1: Enable zero wait state ISA bus operation.
4	Reserved.
5	Reserved.
6	0: 8-bit I/O access. 1: 16-bit I/O access.
7	0: 8-bit memory access. 1: 16-bit memory access.

Default: 'h0

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3DF Video Memory Mapping Register **Index = 14** **R/W**

Bit	Description
0	Enable OTI address mapping. 0: VGA memory mapping at A0000 and B8000 as dictated by Graphics register 6 bits 3&2 1: OTI memory mapping as dictated by register 2x14.
1	Reserved.
4-2	Memory address aperture select. These bits define the memory address aperture that OTI-107 will respond. These bits have no effect if bit 0 = 0.

Bits 4-2	Memory address aperture
000	x00000-x3FFFF: 256K aperture.
001	x00000-x7FFFF: 512K aperture.
010	x00000-xFFFFF: 1MEG aperture.
011	x00000-1FFFFF: 2MEG aperture.
100	x00000-3FFFFF: 4MEG aperture.
101	x00000-7FFFFF: 8MEG aperture.
11x	Reserved.

7-5	Reserved.

Default: 'h0

3DF Memory & Memory Mapped I/O Enable **Index = 15** **R/W**

Bit	Description
5-0	Reserved
6	Enable graphic memory response. This bit and bit 7 of this register are needed in case graphic memory base address is the same or in the same range as memory mapped I/O base address. If the memory spaces are not the same, then both bits should be 1's. 0: disable access to graphic memory 1: enable access to graphic memory
7	Enable memory mapped I/O response. This bit and bit 6 of this register are needed in case graphic memory base address is the same or in the same range as memory mapped I/O base address. If the memory spaces are not the same, then both bits should be 1's. 0: disable access to memory mapped I/O 1: enable access to memory mapped I/O

Default: 'h40

3DF Configuration/DAC/Auxiliary Register Range **Index = 19** **R/W**

Bit	Description
3-0	This bits define the I/O address range for the PCI compatible configuration registers on ISA and VL bus, DAC register address range in addition to the IBM VGA DAC address range 3C6-3C9, and auxiliary register address range for other devices in graphic subsystem. The I/O range can be programmed to be from 2x00-2xBF where x is defined by these four bits. The I/O space is divided among the three sources as follow:

Source	Address Range
Configuration Registers	2x00-2x3C
DAC Registers	2x80-2x9F
Auxiliary Registers	2xA0-2xBF

4	Enable additional DAC address space. 0: DAC address space is at 3C6-3C9 only. 1: DAC address space is at both 3C6-3C9 and 2x80-2x9F.
5	Enable auxiliary address space. This will enable decoding for signal ACSn when on VL bus, or outputs ARDn and AWRn when on PCI or ISA bus. 0: Disable decoding for auxiliary registers. 1: Enable decoding for auxiliary registers.
7-6	Reserved.

Default: 'h01

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6.5.3 Extended Sequencer Registers

3DF Compatible Segment Register **Index = 11** **R/W**

Bit	Description
3-0	Read segment for CPU memory read.
7-4	Write segment for CPU memory write

These two 4 bits segment registers are used to extend the CPU address for video memory size greater than 256K. Bits 3-0 are used to address the memory read operation. Bit 7-4 are used to address the memory for write mode operation. Bits 3-0 are the image of index register 23 bits 3-0. Bits 7-4 are the image of index register 24 bits 3-0.

This register is provided for compatibility with OTI-077, 67, and 37 only. New software development should use registers 23, 24 & 25.

Default: 'h0

3DF Display FIFO Depth Register **Index = 20** **R/W**

Bit	Description
3-0	Graphic mode display FIFO depth control. This register defines the level of the display FIFO at which the CRT refresh will reclaim the memory bus during graphic modes. Note, this register has a different meaning than 67/77/87SX because of the new arbitration scheme.
5-4	Reserved.
7-6	Text mode display FIFO depth control. This register defines number of consecutive memory accesses for CRT refresh during text modes.

Bits 7-6	Consecutive accesses
00	6
01	8
10	10
11	12

Default: 'h81

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3DF Mode Select Register Index = 21 R/W

Bit	Description
0	Enable doubling horizontal timing. This bit is used for high color or true color modes. When this bit is enabled, all horizontal CRT parameters are multiplied by two. See Extended Attribute register for more information.
1	Enable tripling horizontal timing. This bit is used for true color modes. When this bit is enabled, all horizontal CRT parameters are multiplied by three. See Extended Attribute register for more information.
2	Extended graphics mode selection. These bits are used to control memory mapping. 0: VGA modes - 256K memory only 1: OTI packed pixel modes
3	Reserved.
4	CCLK clock frequency. 0: normal frequency as required by resolution (CCLK = VCLK/8, VCLK/9) 1: 1/2 normal frequency as required by resolution (CCLK = VCLK/4)
6-5	Shift/Load frequency.

Bits 6,5	Shift/Load Frequency
00	As specified by SR1[4,2]
01	One shift/load every two VCLK
10	One shift/load every four VCLK
11	One shift/load every six VCLK *

7	Enable synchronous mode (not implemented for revision A) 0: Asynchronous mode. Internal memory clock is MCLK, system interface clock is PROCLK, internal commands are generated with PROCLK and resync with MCLK. 1: Synchronous mode. Internal memory clock is PROCLK, system interface clock is PROCLK or PROCLK/2, internal commands are generated with PROCLK.

Default: 'h0

This register can only be updated during software reset. The correct sequence to update this register is as follow, assuming all I/O cycles are 16-bit transfer:

```
3C4 <= 'h0100
3DE <= 'hxx21
3C4 <= 'h0300
```

Updating this register on the fly will hang the system.

* For Attribute Mode 3 (24bpp/16-bit bus), SHFT/LD is generated once every three VCLK.

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3DF Feature Select Register **Index = 22** **R/W**

Bit	Description
2-0	Reserved.
3	Enable write cache - This bit enables the write cache in the controller. It should be set to 1 for higher performance operations.
4	Graphics Latch width 0: 32-bit - IBM compatible 1: 64-bit - Used with 256 color modes
5	Enable write mode 4. This write mode is used in packed pixel mode only. In this mode, system data is routed directly to the memory, by-passing barrel shifter and ALU. This mode is meant to improve straight Memory to Screen Source Copy. 0: Write mode as controlled by GR5[1:0] 1: Write mode 4.
7-6	Reserved.

Default: 'h0

3DF Extended Read Segment Register **Index = 23** **R/W**

Bit	Description
6-0	These 7 bits corresponds to the CPUADR[22:16] for CPU read operation. They are used to extend the 64K video memory space (A0000-AFFFF). Bits 3:0 are the image of ER11[3:0]. Updating bits 3:0 will also update bits 3:0 of ER11.
7	Reserved.

Default: 'h0

3DF Extended Write Segment Register **Index = 24** **R/W**

Bit	Description
6-0	These 7 bits corresponds to the CPUADR[22:16] for CPU write operation. They are used to extend the 64K video memory space (A0000-AFFFF). Bits 3:0 are the image of ER11b7:4. Updating bits 3:0 will also update bits 7:4 of ER11.
7	Reserved.

Default: 'h0

3DF Extended Common Read Write Register **Index = 25** **R/W**

Bit	Description
6-0	This 6 bits register is a write port for both register 23 and 24. A write to this register is equivalent to writing into both index registers 23 and 24. A read to this register is equivalent to reading the extended write segment register.
7	Reserved.

Default: 'h0

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3DF RASn Control Register **Index = 26** **R/W**

Bit	Description
1-0	RASn precharge width. RASn precharge consists of st1&st2, these bits control the number of st2's inserted. This timing is t_{rp}.

Bits 1,0	Precharge Width
00	2 Mclk (st1, st2)
01	3 Mclk (st1,st2,st2)
10	4 Mclk (st1,st2,st2,st2)
11	5 Mclk (st1,st2,st2,st2,st2)

2	Reserved.
3	Enable half clock option for RASn 0: RASn precharge is as defined by bits 1:0. 1: RASn precharge is decreased by half clock, and RASn pulse width is increased by half clock.
7-4	Reserved.

Default: 'h01 (3 Mclk for precharge)

Note: It is not necessary to program RASn pulse width, this parameter is equal to ras-to-cas-delay plus CASn precharge plus CASn pulse width.

3DF CASn Control Register **Index = 27** **R/W**

Bit	Description
0	CASn precharge width. This is to control number of st4's. This timing is t_{rp2}. 0: 1 Mclk precharge width 1: 2 Mclk precharge width
1	Enable half clock option for CASn. 0: CASn precharge and pulse width as defined by bit 0 and bit 2 respectively. 1: CASn precharge is reduced by half clock, and CASn pulse width is increased by half clock.
2	CASn pulse width. This is to control number of st5's. This timing is t_{wp}. 0: 1 Mclk pulse width (st5) 1: 2 Mclk pulse width (st5,st5)
3	Reserved.
5-4	CASn delay from RASn. This is to control number of st3's. This timing is t_{rp4}. Note that this is not the regular delay from RASn going low to CASn going low, but rather from RASn going low to CASn going low minus CASn precharge. Thus, DRAM specification $t_{RCD} = t_{rp4} + t_{wp}$

Bits 5,4	Delay
00	1 Mclk period
01	2 Mclk periods
10	3 Mclk periods
11	4 Mclk periods

7-6	Reserved.

Default: 'h10 (1 Mclk for precharge and pulse width, 2 Mclk for delay).

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3DF Refresh Control Register **Index = 28** **R/W**

Bit	Description
1-0	Number of refresh cycle per scan line. This register will override CR11[6].
	Bits 1-0 — Number of refresh
	00 — Reserved
	01 — 1 refresh cycle per line
	10 — 2 refresh cycles per line
	11 — Follow CR11[6]
2	Reserved.
3	Type of refresh cycle. 0: CAS-before-RAS refresh 1: RAS only refresh
7-4	Reserved.

Default: 'h03

3DF Hardware Window Arbitration **Index = 29** **R/W**

Bit	Description
1-0	Number of consecutive accesses each time during display fetch. Each access can be either 32-bit or 64-bit depending on memory bus width at the time.
	Bits 2-0 — Consecutive Accesses
	000 — 4
	001 — 8
	010 — 16
	011 — 32
7-2	Reserved.

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6.5.4 Extended CRT Controller Registers

3DF OTI CRT Overflow Register **Index = 30** **R/W**

Bit	Description
0	Vertical Total Bit 10
1	Vertical Blank Start Bit 10
2	Vertical Retrace Start Bit 10
6-3	Reserved.
7	Enable interlaced display. 0: non-interlaced display. 1: interlaced display.

Default: 'h0

3DF CRT Start Address Hi **Index = 31** **R/W**

Bit	Description
6-0	High order start address bits 22-16. Start address bits 15-0 are from CR0C and CR0D.
7	Reserved.

3DF Hsync Divided by Two Start Register **Index = 32** **R/W**

Bit	Description
7-0	This 7 bit value indicates when the vertical retrace will start in every odd frame during interlaced mode. The unit of this value is in character position.

3DF CRT Address Compatibility Register **Index = 33** **R/W**

Bit	Description
0	Address wrapping for compatibility with IBM's VGA. This is useful when application assumes that there are only 256K of memory, and expecting the display address to be these 256K only (JDOS is an example). 0: No wrapping, display full amount of memory available 1:Wrap around the first 256K of memory
7-1	Reserved.

Default: 'h0

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6.5.5 Extended Attribute Controller Registers

3DF Pixel Interface Register **Index = 38** **R/W**

Bit Description

2-0 Pixel Mode - Only in mode 0 that the memory data is routed through the Attribute controller datapath. For modes 1-7, memory data is routed directly to P[23:0] as shown below, bypassing the internal palette and PEL panning logic.

Bits 2-0 Mode	Bpp	P Bus Width	P Bus Ordering P[23:0]	VCLK	PCLK	CCLK	SHFT/LD	HCLK
0	VGA	8	XXP[7:0]	Normal	VCLK	8/9 VCLK	8/16/32 VCLK	CCLK
1	4	8	XX P_1[3:0]P_0[3:0]	1/2	VCLK	4 VCLK	4 VCLK	CCLK
2	8	8	XX P[7:0]	Normal	VCLK	8 VCLK	8 VCLK	CCLK
	16		XX P_0[7:0] XX P_1[15:8]	Double	VCLK	8 VCLK	8 VCLK	CCLK/2
	24		XX P_0[7:0] XX P_1[15:8] XX P_2[23:16]	Triple	VCLK	8 VCLK	6 VCLK	CCLK/3
3	24	16	XP_0[15:0] XP_1[23:16]P_1[7:0]	3/2	VCLK	4 VCLK	6/2 VCLK*	CCLK/3
4	8	16	XP_1[7:0]P_0[7:0]	1/2	VCLK	4 VCLK	4 VCLK	CCLK
5	16	16	XP[15:0]	Normal	VCLK	8 VCLK	4 VCLK	CCLK
6	32	16	XP_0[15:0] XP_1[31:16]	Double	VCLK	8 VCLK	4 VCLK	CCLK/2
7	24	24	P[23:0]	Normal	VCLK	8 VCLK	2 VCLK	CCLK

X - represents 8-bit P data.

3 Reserved

4 Color ordering - only applies to 16bpp and 24bpp modes

Bit 4	P[23:0]/Byte[2:0]	Bits/pixel
0	$GGGRRRRR_1$ $BBBBBGGGGGGRRRRR_0$	16bpp
0	BBBBBBBBGGGGGGGGRRRRRRRR	24bpp
1	$GGGBBBBB_1$ $RRRRRGGGGGGBBBBB_0$	16bpp
1	RRRRRRRRGGGGGGGGBBBBBBBB	24bpp

6-5 Bits per pixel. These bits are used in conjunction with bit 4 for RGB swapping.

Bits 6,5	Bits/pixel
00	8 bpp
01	16 bpp
10	24 bpp
11	32 bpp

7 Reserved

Default: 'h0

* SHFT/LD is programmed to be 6 VCLK , but with this mode, it is actually 3 VCLK.

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6.5.6 Hardware Cursor/Hardware Window Registers

These registers are shared between Hardware Cursor and Hardware Window because both of these can not exist simultaneously. These registers are memory mapped only.

HC/HW Horizontal Position Start Register **Offset = 81,80** **R/W**

Bit	Description
15-0	Horizontal starting position of the HC/HW relative to the start of the display area in pixel unit. This number can be negative and programmed in two's complement format. (0,0) is at left top corner.

HC/HW Vertical Position Start Register **Offset = 83,82** **R/W**

Bit	Description
15-0	Vertical starting position of the HC/HW relative to the start of the display area in scan line unit. This number can be negative and programmed in two's complement format. (0,0) is at left top corner.

HC Horizontal Preset/HW Width Low Register **Offset = 84** **R/W**

Bit	Description
7-0	For hardware cursor, this register defines the starting horizontal position of the HC within the 64x64 area in pixel unit. The HC always ends at position 63 (i.e., no wrapping). For hardware window, this is the lower 8 bits of the hardware window width register in double word unit.

HW Width High Register **Offset = 85** **R/W**

Bit	Description
7-0	For hardware window, this is the higher 8 bits of the hardware window width in double word unit.

HC Vertical Preset/HW Height Register Low **Offset = 86** **R/W**

Bit	Description
7-0	For hardware cursor, this register defines the starting vertical position of the HC within the 64x64 area in scan line unit. The HC always ends at position 63 (i.e., no wrapping). For hardware window, this the lower 8 bits of the hardware window height in pixel unit.

HW Height Register High **Offset = 87** **R/W**

Bit	Description
7-0	For hardware window, this is the higher 8 bits of the hardware window height in pixel unit.

HC Start Address Register **Offset = 8A-88** **R/W**

Bit	Description
23-0	Linear starting address of the buffer within the video memory. The value to be programmed is the system linear address divided by 4 when in planar modes, divided by 8 when in packed pixel modes.

HC Color 0 Register **Offset = 8F-8C** **R/W**

Bit	Description
31-0	HC color 0. Only the corresponding number of bits-per-pixel in the display mode are required in this register. For example, if the display mode is 8 bits-per-pixel, only the 8 low order bits of this register are used.

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HC Color 1 Red Register **Offset = 93-90** **R/W**

Bit	Description
31-0	HC color 1. Only the corresponding number of bits-per-pixel in the display mode are required in this register. For example, if the display mode is 8 bits-per-pixel, only the 8 low order bits of this register are used.

HC Control Register **Offset = 94** **R/W**

Bit	Description
0	Color HC control. Power up default to 0 0: Disable color HC. 1: Enable color HC.
1	HC display selection. 0: HC is under overscan. 1: HC is displayed over overscan.
2	HC data format. 0: Intel format, bit 0 is the first pixel 1: Motorola format, bit 7 is the first pixel
3	HC blink enable. Power up default to 0. 0: Disable HC blinking. 1: Enable HC blinking.
5-4	HC blink rate control. Power up default to 01 (8 frames on and off). Bits 5,4 — Blinking Rate 00 — 4 frames on and off 01 — 8 frames on and off 10 — 16 frame on and off 11 — 32 frames on and off
7-6	Reserved.

Default:'h10

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HW Control Register **Offset = 96** **R/W**

Bit	Description
0	Enable Hardware Window display. This bit will automatically disable Hardware Cursor. 0: Disable Hardware Window display. 1: Enable Hardware Window display. Disable HC.
2-1	Horizontal scaling factor for input data.

Bits 2-1	Scaling factor
00	No scaling.
01	Reduced by two
10	Reduced by four
11	Reduced by eight

Bit	Description
4-3	Vertical scaling factor for input data.

Bits 4-3	Scaling factor
00	No scaling.
01	Reduced by two
10	Reduced by four
11	Reduced by eight

Bit	Description
5	Select odd/even lines for vertical scaling. 0: select even lines for vertical scaling. Scaling by two would result in keeping all even lines. Scaling by 4 or 8 would result in keeping lines 0, 4, 8 ... or 0, 8, 16 ..., respectively. 1: select odd lines for vertical scaling. Scaling by two would result in keeping all odd lines. Scaling by 4 or 8 would result in keeping line 1, 5, 9 ... or 1, 9, 17 ..., respectively.
6	YUV/RGB selection 0: data accepted is decoded as YUV format. 1: data accepted is decoded as RGB format.
7	Enable mask map for imaging port. When enable, the imaging port update is masked by the imaging mask map (not to be confused with the co-processor mask map).

Default: 'h0

HW Mask Map Start Address Register **Offset = 9A-98** **R/W**

Bit	Description
23-0	Linear starting address of the image mask map buffer within the video memory. The value to be programmed is the system linear address divided by 4. Because there is no alignment hardware for this map, software should make sure to program this register in multiple of eight (byte boundary).

HW Start Address Register **Offset = 9E-9C** **R/W**

Bit	Description
23-0	Linear starting address of the buffer within the video memory. This register is used for both input port and output port. The value to be programmed is the system linear address divided by 4.

HW Address Offset Register **Offset = 9F** **R/W**

Bit	Description
7-0	Offset address in word unit. Used to calculate the address of the next line in the window. This register is used for both input port and output port.

HW Line Length Register **Offset = A1-A0** **R/W**

Bit	Description
8-0	Specifies the width of a hardware window line in double word unit. Used for input only.
15-9	Reserved.

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6.5.7 Co-Processor Registers

Unlike XGA registers, most of these registers are read/writeable so that register save/restore can easily be accomplished. Also, all registers are Motorola format only.

Co-Processor Status Register **Offset = 10** **RO**

Bit	Description
1-0	Indicates which map needs data next. These 2 bits are read only. They are used in CPU assisted mode, where driver can find out which map the co-processor would need data to be fetched (memory to screen) by the CPU, or which map would need data to be written to (screen to memory). Bits 3-2 Map 00 Pattern 01 Mask 10 Source 11 Destination
2	Indicates the above map needs to be written to screen memory or read back to system memory. 0 = read back to system memory 1 = write data to screen memory
3	Map status valid. This bit is read only. This bit is used to indicate whether bit 3-2 values are valid or not. When not valid, software should reread bits 3-2 until this bit is valid. 0 = Bits 3-2 are invalid 1 = Bits 3-2 are valid
4	Indicates that the address of the next access needs to be reset to the beginning of the map. 0 = Increment address for next access 1 = Reset address to beginning of the map
5	Advance to next line indication 0 = remain on current line 1 = advance to next line
6	Reserved
7	Co-processor busy status bit (this bit is read only). Reading this bit does not stop Co-processor. 0 = Co-processor is idle. 1 = Co-processor is busy executing.

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Co-Processor Control Register **Offset = 11** **R/W**

Bit	Description
0	Enable co-processor operation complete interrupt. Interrupt is always generated but is routed out to pin CINTn only when this bit is enabled 0 = VGA interrupt is routed out to CINTn 1 = Co-processor operation complete interrupt is routed out to CINTn
1	Enable master mode. This bit should be used with PCI bus only. 0 = CPU assisted mode operation 1 = Master mode operation
4-2	Reserved
5	Terminate co-processor operation. 0 = Allow co-processor to finish the operation. 1 = Terminate co-processor operation.
6	Enable turbo co-processor data-path. Used with slower mclk frequency (50MHz or less) 0 = default datapath delay 1 = delete an extra clock for datapath delay
7	Reserved.

Default: 'h0

Pixel Map Select Register **Offset = 12** **R/W**

Bit	Description
1-0	Index to indicate which pixel map registers are being accessed.

Bit 1,0	Pixel Map Select
00	Mask Map
01	Pixel Map A
10	Pixel Map B
11	Pixel Map C

7-2	Reserved.

Pixel Map n Base Pointer Register **Offset = 17-14** **R/W**

Bit	Description
31-0	This register specifies the start of a Pixel Map in byte address.

Pixel Map n Width Register **Offset = 19,18** **R/W**

Bit	Description
11-0	This register specifies the width of a Pixel Map minus one in pixel unit. The programmed value is one less than the actual value.
15-12	Reserved.

Pixel Map n Height Register **Offset = 1B,1A** **R/W**

Bit	Description
11-0	This register specifies the height of a Pixel Map minus one in pixel unit. The programmed value is one less than the actual value.
15-12	Reserved.

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Pixel Map n Format Register **Offset = 1C** **R/W**

Bit	Description
2-0	Specifies the number of bits/pixel in the Pixel Map.

Bits 1,0	Number of bits/pixel
000	1 bit
001	Reserved
010	Reserved
011	8 bits
100	16 bits
101	32 bits
110	Reserved.
111	Reserved.

6-3 Reserved.

7 System memory indication.
0: Map is in local frame buffer, no special treatment is needed.
1: Map is in system memory, master cycle or CPU assisted cycle is needed.

Source and Destination Pixel Maps and have 1, 8, 16 or 32 bits/pixel. Pattern Pixel Map can only have 1 bit/pixel. Programming Pattern Pixel Map to be anything other than 1 bit/pixel will produce undefined results. Mask Map Format Register can not be programmed at all because it is assumed to be 1 bit/pixel. However, one should still program it to be 1 bit/pixel to ensure future compatibility.

Bresenham Error Term Register **Offset = 21,20** **R/W**

Bit	Description
13-0	This register specifies the Bresenham Error Term for the Draw Line function. This value is ((2*deltaY) - deltaX). This number is 14-bit sign extended two's complement ranged from -8192 to +8191.
15-14	Reserved.

Bresenham Constant K1 **Offset = 25,24** **R/W**

Bit	Description
13-0	This register specifies the Bresenham Constant K1 for the Draw Line function. This value is (2*deltaY). This number is 14-bit sign extended two's complement ranged from -8192 to +8191
15-14	Reserved.

Bresenham Constant K2 **Offset = 29,28** **R/W**

Bit	Description
13-0	This register specifies the Bresenham Constant K2 for the Draw Line function. This value is 2*(deltaY - deltaX). This number is 14-bit sign extended two's complement ranged from -8192 to +8191.
15-14	Reserved.

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Direction Steps Register **Offset = 2F-2C** **R/W**

This register specifies up to four Draw and Step codes and initiate a Draw and Step operation by writing to byte three of this register. Each code is one byte. Not all bytes have to be programmed

Bit	Description
3-0	Number of steps for code-1 from 1-16. The programmed number is one less than actual drawn length.
4	Move/draw operation select for code-1 0: move operation - update X-Y pointers but the no pixels are drawn. 1: draws pixels as normal
7-5	Direction step for code-1. Direction is as follow:

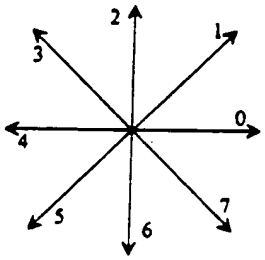


Figure 6.1 - Draw & Step Direction Codes

11-8	Number of steps for code-2 from 1-16. The programmed number is one less than actual drawn length.
12	Move/draw operation select for code-2. 0: move operation - update X-Y pointers but the no pixels are drawn. 1: draws pixels as normal
15-13	Direction step for code-2.
19-16	Number of steps for code-3 from 1-16. The programmed number is one less than actual drawn length.
20	Move/draw operation select for code-3. 0: move operation - update X-Y pointers but the no pixels are drawn. 1: draws pixels as normal
23-21	Direction step for code-3.
27-24	Number of steps for code-4 from 1-16. The programmed number is one less than actual drawn length.
28	Move/draw operation select for code-4. 0: move operation - update X-Y pointers but the no pixels are drawn. 1: draws pixels as normal
31-29	Direction step for code-4.

Write to byte 3 (bits 31-24) will start the Draw & Step process.

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ROP Register **Offset = 48** **R/W**

Bit	Description
3-0	These bits specified the Background ROP function to be performed between Destination and Source pixels during an operation where the Pattern pixel value is 0.
7-4	These bits specified the Foreground ROP function to be performed between Destination and Source pixels during an operation where the Pattern pixel value is 1.

Bits 7-4 (3-0)	Function	Reverse Polish
0h	zeros	0
1h	(NOT source) AND (NOT destination)	SDon
2h	(NOT source) AND destination	DSna
3h	NOT source	Sn
4h	source AND (NOT destination)	SDna
5h	NOT destination	Dn
6h	source XOR destination	SDx
7h	(NOT source) OR (NOT destination)	SDan
8h	source AND destination	SDa
9h	source XOR (NOT destination)	SDnx
Ah	destination	D
Bh	(NOT source) OR destination	DSno
Ch	source	S
Dh	source OR (NOT destination)	SDno
Eh	source OR destination	SDo
Fh	ones	1

With the combination of Foreground ROP and Background ROP under control of Pattern, the OTI-107 can support all 256 ROP as defined by Windows.

Destination Color Compare Condition Register **Offset = 4A** **R/W**

Bit	Description
2-0	These bits specify the Color Compare Condition under which Destination update is inhibited.

Bits 2-0	Destination Color Compare Condition
000	Always true (disable update)
001	Reserved.
010	Dest = color compare value
011	Reserved.
100	Dest <> color compare value
101	Reserved.
110	Always false (enable update)
111	Reserved.

7-3 Reserved.

Default: 'b06

Destination Color Compare Value Register **Offset = 4F-4C** **R/W**

Bit	Description
31-0	Color value to be compared to Destination pixels when Color Compare is enabled. Only the corresponding number of bits-per-pixel in the Destination are required in this register. For example, if the Destination is 8 bits-per-pixel, only the 8 low order bits of this register are used, and only bit 0 is used for 1bpp.

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Pixel Bit Mask Register **Offset = 53-50** **R/W**

Bit	Description
31-0	This register specifies which bits within each pixel are subject to be updated. 0 = Disable update for the particular bit 1 = Enable update for the particular bit. Only the corresponding number of bits-per-pixel in the Destination are required in this register. For example, if the Destination is 8 bits-per-pixel, only the 8 low order bits of this register are used, and only bit 0 is used for 1bpp.

Foreground Color Register **Offset = 5B-58** **R/W**

Bit	Description
31-0	This register specifies the foreground color to be used as the Foreground Source during operations. Only the corresponding number of bits-per-pixel in the Destination are required in this register. For example, if the Destination is 8 bits-per-pixel, only the 8 low order bits of this register are used, and only bit 0 is used for 1bpp.

Background Color Register **Offset = 5F-5C** **R/W**

Bit	Description
31-0	This register specifies the background color to be used as the Background Source during operations. Only the corresponding number of bits-per-pixel in the Destination are required in this register. For example, if the Destination is 8 bits-per-pixel, only the 8 low order bits of this register are used, and only bit 0 is used for 1bpp.

Operation Dimension 1 Register **Offset = 61,60** **R/W**

Bit	Description
11-0	This register specifies the width of the rectangle to be drawn by the PxBlt function. The programmed number should be one less than the required number.
15-12	Reserved.

Operation Dimension 2 Register **Offset = 63,62** **R/W**

Bit	Description
11-0	This register specifies the height of the rectangle to be drawn by the PxBlt function. The programmed number should be one less than the required number.
15-12	Reserved.

The following registers 6C-7B have two stages, first stage is the register where data is written to, and the second stage is the actual counter where the data is read from. Since the counters are not loaded until a co-processor start is issued, it is not possible to read the registers correctly after they were written.

Mask Map Origin X Offset Register **Offset = 6D,6C** **R/W**

Bit	Description
12-0	This register specifies the X offset of the Mask Map origin relative to the origin of the Destination Map.
15-13	Reserved.

Mask Map Origin Y Offset Register **Offset = 6F,6E** **R/W**

Bit	Description
12-0	This register specifies the Y offset of the Mask Map origin relative to the origin of the Destination Map.
15-13	Reserved.

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Source X Pointer Register **Offset = 71,70** **R/W**

Bit	Description
11-0	This register specifies the X coordinate of the Source Map.
15-12	Reserved.

Source Y Pointer Register **Offset = 73,72** **R/W**

Bit	Description
11-0	This register specifies the Y coordinate of the Source Map.
15-12	Reserved.

Pattern X Pointer Register **Offset = 75,74** **R/W**

Bit	Description
11-0	This register specifies the X coordinate of the Pattern Map.
15-12	Reserved.

Pattern Y Pointer Register **Offset = 77,76** **R/W**

Bit	Description
11-0	This register specifies the Y coordinate of the Pattern Map.
15-12	Reserved.

Destination X Pointer Register **Offset = 79,78** **R/W**

Bit	Description
12-0	This register specifies the X coordinate of the Destination Map.
15-13	Reserved.

Destination Y Pointer Register **Offset = 7B,7A** **R/W**

Bit	Description
12-0	This register specifies the Y coordinate of the Destination Map.
15-13	Reserved.

Pixel Operations Register **Offset = 7F-7C** **R/W**

Bit	Description
2-0	These bits specify the direction octant for PxBlt and Line Draw operations.

Bits 2,1	Direction Octant for PxBlt
00	Start at top left corner of area increasing right and down
01	Start at bottom left corner of area increasing right and up
10	Start at top right corner of are increasing left and down
11	Start at bottom right corner of are increasing left and up

Bits 2-0	Direction Octant for Line Draw
000	Octant 0
.	.
111	Octant 8

3	Reserved.
5-4	Drawing Mode Register. These bits determine the attributes of Line Draw and Draw and Step operations.

Bits 5,4	Drawing Mode
00	Draw all pixels
01	Draw first pixel null
10	Draw last pixel null
11	Draw area boundary

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7-6 Mask Pixel Map Control.

Bits 7,6	Mask Functions
00	Mask Map Disabled
01	Mask Map Boundary Enabled
10	Mask Map Enabled
11	Reserved

11-8 Reserved.

15-12 Pattern Pixel Map Control.

Bits 15-12	Pattern Map Control
0000	Reserved
0001	Use Pixel Map A for Pattern Map
0010	Use Pixel Map B for Pattern Map
0011	Use Pixel Map C for Pattern Map
01xx	Reserved
1000	Use Foreground ROP
1001	Generate Pattern from Source
1010	Reserved
1111	Reserved

19-16 Destination Pixel Map Control.

Bits 19-16	Destination Map Control
0000	Reserved
0001	Use Pixel Map A for Destination Map
0010	Use Pixel Map B for Destination Map
0011	Use Pixel Map C for Destination Map
0100	Reserved
1111	Reserved

23-20 Source Pixel Map Control.

Bits 23-20	Source Map Control
0000	Reserved
0001	Use Pixel Map A for Source Map
0010	Use Pixel Map B for Source Map
0011	Use Pixel Map C for Source Map
0100	Reserved
1111	Reserved

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27-24 Co-processor Function Control

Bits 27-24	Function Control
0000	Reserved
0001	Reserved
0010	Draw and Step Read
0011	Line Draw Read
0100	Draw and Step Write
0101	Line Draw Write
0110	Reserved
0111	Reserved
1000	PxBlt
1001	Inverting PxBlt
1010	Area Fill PxBlt
1011	TextBlt. This mode is designed to enhance text output. To use this mode, the monochrome font must be stored as pattern map, and the font (pattern) map base address plus map width must always be within one quad word (64-bit), and operation dimension 1 must be less than or equal to map width (no tiling) For example, if base address=0, then map width can be any size up to 64, if base address='h38, then map width can only be up to 8.
1100	Reserved
1111	Reserved

29-28 Foreground Source. These bits specify what foreground source to be combined with Destination when the Pattern pixel is a 1.

Bits 29-28	Foreground Source
00	Use Foreground Color Register
01	Reserved
10	Use Source pixel map
11	Reserved

31-30 Background Source. These bits specify what background source to be combined with Destination when the Pattern pixel is a 0.

Bits 31-30	Background Source
00	Use Background Color Register
01	Reserved
10	Use Source pixel map
11	Reserved

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7 VGA REGISTERS

7.1 VGA Register Summary

General Registers

Register Description	R/W	Port	Index	Bits	Block
Miscellaneous Output Register	R/W	3CC/3C2		7	BI
Input Status Register 0	RO	3C2		2	BI
Input Status Register 1	RO	3?A		4	BI
Feature Control Register	R/W	3CA/3?A		1	BI

Sequencer Registers

Register Description	R/W	Port	Index	Bits	Block
Sequencer Address	R/W	3C4		3	SEQ
Reset	R/W	3C5	0	2	SEQ
Clocking Mode	R/W	3C5	1	5	SEQ
Map Mask	R/W	3C5	2	4	SEQ
Character Map Select	R/W	3C5	3	6	SEQ
Memory Mode	R/W	3C5	4	3	SEQ

CRT Controller Registers

Register Description	R/W	Port	Index	Bits	Block
CRT Controller Address	R/W	3?4		6	CRT
Horizontal Total	R/W	3?5	0	8	CRT
Horizontal Display Enable End	R/W	3?5	1	8	CRT
Start Horizontal Blanking	R/W	3?5	2	8	CRT
End Horizontal Blanking	R/W	3?5	3	8	CRT
Start Horizontal Retrace Pulse	R/W	3?5	4	8	CRT
End Horizontal Retrace	R/W	3?5	5	8	CRT
Vertical Total	R/W	3?5	6	8	CRT
Overflow	R/W	3?5	7	8	CRT
Preset Row Scan	R/W	3?5	8	7	CRT
Maximum Scan Line	R/W	3?5	9	8	CRT
Cursor Start	R/W	3?5	A	6	CRT
Cursor End	R/W	3?5	B	7	CRT
Start Address High	R/W	3?5	C	8	CRT
Start Address Low	R/W	3?5	D	8	CRT
Cursor Location High	R/W	3?5	E	8	CRT
Cursor Location Low	R/W	3?5	F	8	CRT
Vertical Retrace Start	R/W	3?5	10	8	CRT

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Vertical Retrace End	R/W	3?5	11	8	CRT
Vertical Display Enable End	R/W	3?5	12	8	CRT
Offset	R/W	3?5	13	8	CRT
Underline Location	R/W	3?5	14	7	CRT
Start Vertical Blank	R/W	3?5	15	8	CRT
End Vertical Blank	R/W	3?5	16	8	CRT
CRTC Mode Control	R/W	3?5	17	7	CRT
Line Compare	R/W	3?5	18	8	CRT

Graphics Controller Registers

Register Description	R/W	Port	Index	Bits	Block
Graphics Address	R/W	3CE		4	GRF
Set/Reset	R/W	3CF	0	4	GRF
Enable Set/Reset	R/W	3CF	1	4	GRF
Color Compare	R/W	3CF	2	4	GRF
Data Rotate	R/W	3CF	3	5	GRF
Read Map Select	R/W	3CF	4	2	GRF
Graphics Mode	R/W	3CF	5	6	GRF
Miscellaneous	R/W	3CF	6	4	GRF
Color Don't Care	R/W	3CF	7	4	GRF
Bit Mask	R/W	3CF	8	8	GRF

Attribute Controller Registers

Register Description	R/W	Port	Index	Bits	Block
Attribute Address	R/W	3C0		6	ATR
Palette	R/W	3C1/3C0	00-0F	6x16	ATR
Attribute Mode Control	R/W	3C1/3C0	10	7	ATR
Overscan Color	R/W	3C1/3C0	11	8	ATR
Color Plane Enable	R/W	3C1/3C0	12	6	ATR
Horizontal Pel Panning	R/W	3C1/3C0	13	4	ATR
Color Select	R/W	3C1/3C0	14	4	ATR

DAC Registers

Register Description	R/W	Port	Index	Bits	Block
PEL Address (Write Mode)	R/W	3C8			BI
PEL Address (Read Mode)	WO	3C7			BI
DAC State	RO	3C7			BI
PEL Data	R/W	3C9			BI
PEL Mask	R/W	3C6			BI

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7.2 General Purpose Registers

3CC/3C2 **Miscellaneous Output Register** R/W

Bit	Description
0	Input/Output Address Select - This bit maps the CRTC I/O addresses for monochrome or color emulation. 0 = Monochrome emulation with CRTC addresses set to 3Bx hex, Input Status 1 register set to 3BA hex. 1 = Color emulation with CRTC addresses set to 3Dx, Input Status 1 register set to 3DA hex.
1	Enable RAM 0 = Disable Video RAM address decode from the system microprocessor. 1 = Enable Video RAM to the system microprocessor.
3,2	Clock Select - These bits are the same as bits 1-0 of Clock Select Register. These bit represent the state of signals CSEL[1] and CSEL[0], respectively.
4	Reserved
5	Page Bit For Odd/Even - Selects between two pages of memory when in the odd or even modes (0-5). 0 = Low 64K page of memory. 1 = High 64K page of memory.
6	Horizontal Sync Polarity 0 = Positive Vertical Retrace 1 = Negative Vertical Retrace
7	Vertical Sync Polarity 0 = Positive Vertical Retrace 1 = Negative Vertical Retrace

Bits 7 and 6 are used to select the vertical size of the monitor as follows:

Bits 7,6	Vertical Size
00	Reserved
01	400 lines
10	350 lines
11	480 lines

3C2 **Input Status Register 0** RO

Bit	Description
3-0	Reserved
4	Switch Sense Bit - Reports the status of one of the four switches selected via the clock select of the Miscellaneous Output register. This bit allows the power-on initialization to determine if a monochrome or color monitor is connected to the system. 0 = Selected sense switch is off or 0. 1 = Selected sense switch is on or 1.
6,5	Reserved
7	CRT Interrupt 0 = Vertical retrace interrupt is pending. 1 = Vertical retrace interrupt is cleared.

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3?A **Input Status Register 1** **R**

Bit	Description
0	Display Enable - Monitors the status of the display. To avoid glitches on the display, some programs use this bit to restrict screen updates to de-activate display intervals. The VGA has been designed to eliminate this software requirement, so display screen updates may be made at any time. 0 = The display of video data is enabled. 1 = The display is in horizontal or vertical retrace mode.
2,1	Reserved
3	Vertical Retrace 0 = Video information is being displayed. 1 = A vertical retrace interval is in progress.
5,4	Diagnostic Usage - Reports the status of two of the eight VGA attribute controller outputs. The values set into the Video Status MUX field of the Color Plane Enable Register determine which colors are input to these two diagnostic bits.
7,6	Reserved

Bits 5,4	Pixel Data
00	P2, P0
01	P5, P4
10	P3, P1
11	P7, P6

3CA/3?A **Feature Control Register** **R/W**

Bit	Description
2-0	Reserved
3	Vertical Sync Select 0 = This bit should always be set to 0 to enab . normal vertical sync output to the monitor. 1 = The vertical sync output is the logical OR of vertical sync and vertical display enable.
7-4	Reserved

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7.3 Sequencer Registers

3C4 **Sequencer Address Register** R/W

Bit	Description
2-0	Sequencer Address Bits - A binary value pointing to the register where data is to be read or written.
7-3	Reserved

3C5 **Reset Register** **Index=0** R/W

Bit	Description
0	Asynchronous Reset 0 = Asynchronous clear and halt the sequencer. This may cause data loss in the dynamic RAMs 1 = Bit 1 and 0 must be 1 to allow the sequencer to operate.
1	Synchronous Reset - This bit should be set to 0 before changing bit 0 or bit 3 of the Clocking Mode register or bit 2 or bit 3 of the Miscellaneous Output register, or all bits of register 3DF index D. 0 = Synchronous clear and halt the sequencer. 1 = Bit 1 and 0 must be 1 to allow the sequencer to operate.
7-2	Reserved

Default: 'h0

3C5 **Clocking Mode Register** **Index=1** R/W

Bit	Description
0	8/9 Dot Clocks - The 9 dot mode is for Alphanumeric modes only. The ninth dot equals the eighth dot for ASCII codes C0 though DF hex. Also, see the Line Graphics Character Code bit in the Attribute Mode Control register section. 0 = Directs the sequencer to generate nine dot wide character clocks. 1 = Generate eight dot wide character clocks.
1	Reserved
2	Shift Load 0 = If bit 4 is set to 0, also, the video serializers are reloaded every character clock. 1 = The video serializers are reloaded every other character clock. this mode is useful when 16 bits are fetched per cycle and chained together in the shift load registers.
3	Dot Clock divided by two 0 = Select normal dot clocks from video clock input. 1 = The master clock will be divided by 2 to generate the dot clock. This is used for 320 and 360 horizontal PEL modes.
4	Shift 4 0 = The video serializers are reloaded every character clock. 1 = The serializers are loaded every fourth character clock. This is useful when 32 bits are fetched per cycle and chained together in the shift registers.
5	Screen Off - This bit is used for fast full-screen updates. 0 = Normal screen operation. 1 = Turns off the video screen and assigns the maximum memory bandwidth to the system CPU.
7,6	Reserved

Default: 'h0

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3C5 **Map Mask Register** **Index=2** **R/W**

Bit	Description
3-0	Map Mask for planes 0-3, respectively. For odd/even modes, maps 0 and 1, and maps 2 ad 3 should have the same map mask value. When chain 4 mode is selected, all maps should be enabled. This is a read-modify-write operation. 0 = Disable memory write to the corresponding map. 1 = Enables the system to write to the corresponding map. If all four bits are set to 1, the system CPU can perform a 32-bit operation with only one memory cycle.
7-4	Map Mask for planes 4-7 respectively. These bits are only enabled, readable and writeable when high resolution (640x480 and up) 256 colors, planar modes are enabled. Otherwise, they are treated like reserved bits.

3C5 **Character Map Select Register** **Index=3** **R/W**

Bit 1,0 Character Map Select B - Selects the portion of map 2 used to generate Alpha characters with bit 4 as the high bit when attribute bit 3 is 0.

Bit 4,1,0 Map	Table Location	
000	0	1st 8k of Map 2
001	1	3rd 8k of Map 2
010	2	5th 8k of Map 2
011	3	7th 8k of Map 2
100	4	2nd 8k of Map 2
101	5	4th 8k of Map 2
110	6	6th 8k of Map 2
111	7	8th 8k of Map 2

3,2 Character Map Select A - Selects the portion of map 2 used to generate Alpha characters with bit 5 as the high bit when attribute bit 3 is 1.

Bit 5,3,2 Map	Table Location	
000	0	1st 8k of Map 2
001	1	3rd 8k of Map 2
010	2	5th 8k of Map 2
011	3	7th 8k of Map 2
100	4	2nd 8k of Map 2
101	5	4th 8k of Map 2
110	6	6th 8k of Map 2
111	7	8th 8k of Map 2

4 Character Map Select High Bit B

5 Character Map Select high Bit A

7,6 Reserved

Default: 'h0

Bit 3 of the attribute byte normally controls the ON/OFF of the foreground intensity in text modes. This bit may be redefined as a switch between character sets. For this feature to be enabled, the following smust be true: 1) the setting value of Character Map Select A does not equal the value of Character Map Select B, 2) the Memory Mode register bit 1, must be equal to 1, 3) if either of these are not true, the first 16K of Map 2 is used.

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3C5 **Memory Mode Register** **Index=4** **R/W**

Bit	Description
0	Reserved
1	Extended Memory 0 = No extended memory present. Display memory is less than 64 Kbytes. 1 = Extended memory is present. Display memory is greater than 64 Kbytes. If set to 1 the VGA is permitted to use the 256k bytes of video memory. This also enables character map selection
2	Odd/Even 0 = Directs even CPU addresses to access maps 0 and 2, and odd CPU addresses to access maps 1 and 3. 1 = If bit 3 is set to 0, this bit causes system CPU addresses to sequentially address data within a bit map.
3	Chain 4 0 = If bit 2 is set to 1, this bit enables the system CPU to address data sequentially within a bit map by use of the Map Mask register. 1 = Causes two low-order address bits to select the map that will be accessed as follows:
7-4	Reserved

A1	A0	Map Selected
0	0	0
0	1	1
1	0	2
1	1	3

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7.4 CRT Controller Registers

CRT Contriler registers resides at either 3B4/5 for Monochrome emulation modes or 3D4/5 for Color emulation modes depending on bit 0 of the Miscellaneous output register at address 3C2 hex.

3?4 **CRT Controller Address Register** R/W

Bit	Description
4-0	CRT Controller Address Bits - A binary value programmed in these bits selects one of the CRT Controller registers where data is to accessed.
5	Test Bit - Must remain 0.
7,6	Reserved.

3?5 **Horizontal Total Register** **Index=0** R/W

Bit	Description
7-0	Horizontal Total - This register defines the total number of characters in the horizontal scan interval including the retrace time. This value directly controls the period of the horizontal retrace output signal. Character clock inputs to the CRT controller and counted by an internal horizontal character counter. This value is is compared with the horizontal character values to provide horizontal timings. All horizontal and vertical timings are based upon the horizontal register. The value programmed is 5 less than the desired value.

3?5 **Horizontal Display Enable End Register** **Index=1** R/W

Bit	Description
7-0	Horizontal Display Enable End - The total number of displayed characters minus 1. This register defines the length of the horizontal display enable signal. It determines the number of displayed characters per horizontal line.

3?5 **Start Horizontal Blanking Register** **Index=2** R/W

Bit	Description
7-0	Start Horizontal Blanking - Determines when to start the internal horizontal blanking output signal. When the internal character counter reaches this value, the horizontal blanking signal becomes active.

3?5 **End Horizontal Blanking Register** **Index=3** R/W

Bit	Description
4-0	End Horizontal Blanking - The horizontal blanking signal width is determined as follows: Value of Start Blanking register + width of blanking signal in character clock units = 6-bit result to be programmed into the End Horizontal blanking register. Bit number 5 is located in the End Horizontal Retrace register. If these six bits equal the the six least significant bits the horizontal character counter, the horizontal blanking signal becomes inactive.
6,5	Display Enable Skew Control - These two bits indicate the magnitude of display enable skew. Bits 5 and 6 and the amount of skew are as follows:

Bits 6,5	Skew
00	Zero character clock skew
01	One character clock skew
10	Two character clock skew
11	Three character clock skew

Bit	Description
7	Test Bit - Must be set to 1.

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3?5 **Start Horizontal Retrace Pulse Register** **Index=4** **R/W**

Bit	Description
7-0	Start Horizontal Retrace Pulse - This register is used to center the screen horizontally and to specify the character position at which the Horizontal Retrace Pulse becomes active. The value in this register is a binary count of the character position number at which the signal becomes active.

3?5 **End Horizontal Retrace Register** **Index=5** **R/W**

Bit	Description
4-0	End horizontal Retrace - The value programmed here is compared to the five least-significant bits of the horizontal character counter. When they are equal, the horizontal retrace signal becomes inactive (logical 0). To calculate the width of the retrace signal use the following algorithm: Value of Start Horizontal Retrace register + width of Horizontal Retrace signal in character clock units = 5-bit result to be programmed into the End Horizontal Retrace register
6,5	Horizontal Retrace Delay - These bits control the skew of the Horizontal Retrace signal as follows:

Bit 6,5	Amount of Skew
00	Zero skew
01	One skew
10	Two skew
11	Three skew

Bit	Description
7	End Horizontal Blanking, Bit number 5 - The first 4 bits are located in the End Horizontal Blanking register (index 03 hex).

3?5 **Vertical Total Register** **Index=6** **R/W**

Bit	Description
7-0	Vertical Total - This is the low-order 8 bits of a 10 bit register that represents the number of horizontal raster scans on the CRT screen, minus 2, including vertical retrace. This value determines the period of the vertical retrace signal. Bit 8 and 9 of this register is located in the CRT Controller Overflow register 07 hex bit 0 and 5, respectively.

3?5 **CRT Controller Overflow Register** **Index=7** **R/W**

Bit	Description
0	Vertical Total - Bit 8 of the Vertical Total register (index 06 hex).
1	Vertical Display Enable End - Bit 8 of the Vertical Display Enable End register (index 12 hex).
2	Vertical Retrace Start - Bit 8 of Vertical Retrace Start register (index 10 hex).
3	Start Vertical Blank - Bit 8 of the Start Vertical Blank register (index 15 hex).
4	Line Compare - Bit 8 of the Line Compare register (index 18 hex).
5	Vertical Total - Bit 9 of the Vertical Total register (index 06 hex).
6	Vertical Display Enable END - Bit 9 of the Vertical display Enable end register (index 12 hex).
7	Vertical Retrace Start - Bit 9 of the Vertical Retrace Start register (index 10 hex).

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3?5 **Preset Row Scan Register** **Index=8** **R/W**

Bit	Description
4-0	Preset Row Scan (PEL Scrolling) - These bits specify the starting row scan count after a vertical retrace. The row scan counter increments each horizontal retrace time until a maximum row scan occurs. At maximum row scan compare time, the scan is cleared (not preset).
6.5	Byte Panning Control - This field controls byte panning in modes programmed as multiple shift modes, which is required for PEL-panning operations. The Horizontal PEL Panning register in the Attribute Controller provides panning of up to 8 individual PEL-panning operations. In single byte shift modes, the CRT Controller start address is incremented and attribute panning is reset to 0 to pa to the next higher PEL. In multiple shift modes, the byte pan bits are used as extensions to the attribute PEL Panning register. This allows panning across the width of the video output shift.
7	Reserved

3?5 **Maximum Scan Line Register** **Index=9** **R/W**

Bit	Description
4-0	Maximum Scan Line - These bits specify the number of scan lines per character row. The number to be programmed is the maximum row number minus 1.
5	Start Vertical Blank - Bit 9 of the Start Vertical Blank register (index 15 hex).
6	Line Compare - Bit 9 of the Line Compare register (index 18 hex).
7	200 to 400 Line Conversion - 0 = The clock to the row scan counter is equal to the horizontal scan rate. Line doubling is disabled. 1 = The clock in the row scan counter is divided by 2. This allows the older 200-line modes to be displayed as 400 lines on the display. This is referred to as line doubling.

3?5 **Cursor Start Register** **Index=A** **R/W**

Bit	Description
4-0	Cursor Start - This field specifies the row scan line of a character line where the cursor is to begin. The number programmed is one less than the starting cursor row scan. If the Cursor Start register is programmed with a value greater than the cursor End register, no cursor is generated.
5	Cursor Off 0 = Turns on the cursor. 1 = Turns off the cursor.
7,6	Reserved.

3?5 **Cursor End Register** **Index=B** **R/W**

Bit	Description
4-0	Cursor End - This field specifies the row scan of a character line where the cursor is to end.
6,5	Cursor Skew - These bits control the skew of the cursor signal. Cursor skew delays the cursor by the selected number of clocks.
7	Reserved.

Bits 6,5	Function
00	Zero-character clock skew
01	One-character clock skew
10	Two-character clock skew
11	Three-character clock skew

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3?5 **Start Address High Register** **Index=C** **R/W**

Bit	Description
7-0	Start Address High - This register contains the high-order 8-bits of the start address. The 16-bit value, from the high-order and low-order Start Address registers, is the first address after the vertical retrace on each screen refresh.

3?5 **Start Address Low Register** **Index=D** **R/W**

Bit	Description
7-0	Start Address Low - This register contains the low-order 8-bits of the start address

3?5 **Cursor Location High Register** **Index=E** **R/W**

Bit	Description
7-0	Cursor High - This register contains the high-order 8-bits of the cursor location

3?5 **Cursor Location Low Register** **Index=F** **R/W**

Bit	Description
7-0	Cursor Low - This register contains the low-order 8-bits of the cursor location.

3?5 **Vertical Retrace Start Register** **Index=10** **R/W**

Bit	Description
7-0	Vertical Retrace Start -This register contains the low-order 8-bits of the vertical retrace pulse start position, Programmed in horizontal scan lines. Bit 8 and 9 are in the CRTC Overflow register (index 07 hex).

3?5 **Vertical Retrace End Register** **Index=11** **R/W**

Bit	Description
3-0	Vertical Retrace End -This field determines the horizontal scan count value when the vertical retrace output signal becomes inactive. This register is programmed in units of horizontal scan lines. To obtain a vertical retrace signal of width W, use the following algorithm: Value of Start Vertical Retrace register + width of vertical retrace signal in horizontal scan units = 4-bit result to be programmed into the End Horizontal Retrace register.
4	Clear Vertical Interrupt 0 = Clears the vertical retrace interrupt flip-flop 1 = Allows the vertical interrupt to be set at the start of the next vertical retrace interval.
5	Enable Vertical Interrupt 0 = Enables a vertical retrace interrupt (on IRQ2). This interrupt level may be shared so the Input Status register 0, bit 7 should be checked to find out is the VGA caused the interrupt to occur. 1 = Disable the vertical retrace interrupt.
6	Select 5 Refresh Cycles 0 = Selects three refresh cycles. The BIOS sets this bit to 0 during a mode set, a reset, or power on. 1 = Selects five refresh cycles per horizontal line. This allow the use of the VGA chip with slow sweep rate displays (15.75 kHz).
7	Protect CRT Registers 0-7 0 = Enables writing to CRTC registers 0-7. 1 = Disables writing to CRTC registers 0-7. The line compare bit 4 in register 07 hex is not protected.

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3?5	**Vertical Display Enable End Register**	**Index=12**	**R/W**
Bit	Description		
7-0	Vertical Display Enable End - This register contains the low-order 8 bits of a 10-bit register that defines the vertical display enable end position. Bit 8 and 9 is located in the CRT Controller Overflow register 07 hex, bit 1 and 6, respectively.		

3?5	**Offset Register**	**Index=13**	**R/W**
Bit	Description		
7-0	Offset - This register specifies the logical line width of the screen. The starting memory address for the next character row is larger than the current character row by a factor of two or four times the the Offset register contents.		

3?5	**Underline Location Register**	**Index=14**	**R/W**
Bit	Description		
4-0	Underline Location - This field specifies the horizontal row scan of a character row on which an underline occurs. The value programmed is one less than the scan line number desired.		
5	Count By 4 0 = Normal clocking. 1 = The memory address counter is clocked with the character clock divided by 4.		
6	Doubleword Mode 0 = Normal word addressing mode. 1 = Memory addresses are doubleword addresses.		
7	Reserved.		

3?5	**Start Vertical Blanking Register**	**Index=15**	**R/W**
Bit	Description		
7-0	Start vertical blank - This register contains the low 8-bits of a 10-bit register. Bit 8 is in the CRTC Overflow register (index 07 hex). Bit 9 is in the Maximum Scan Line register (index 09 hex).		

3?5	**End Vertical Blanking Register**	**Index=16**	**R/W**
Bit	Description		
7-0	End Vertical Blank - This register specifies the horizontal scan count value when the vertical blank output signal becomes inactive. It is programmed in units of horizontal scan lines. To obtain the vertical blank signal of width W, use the following algorithm: Value of Start Vertical Blank register minus 1 + width of vertical blank signal in horizontal scan units = 8-bit result to be programmed into the End Vertical Blank register.		

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3?5 **CRTC Mode Control Register** **Index=17** **R/W**

Bit	Description
0	Compatibility Mode Support 0 = Row scan address bit 0 is substituted for memory address bit 13 during active display time. 1 = Enables memory address bit 13 to appear on the memory address output bit 13 of the CRT controller.
1	Select Row Scan Counter 0 = Selects row scan counter bit 1 for CRT memory address bit MA14. 1 = Selects MA14 counter bit for CRT memory address bit MA14.
2	Horizontal Retrace Select 0 = Selects normal horizontal retrace as the clock that controls the vertical timing counter 1 = Selects horizontal retrace divided by 2 as the clock that controls the vertical timing counter Therefore, the vertical resolution is doubled to 2048 horizontal scan lines.
3	Count By Two 0 = The memory address counter is clocked with the character clock input. 1 = Clocks the memory address counter with the character clock input divided by 2.
4	Reserved.
5	Address Wrap - Selects memory address counter bit MA13 or bit MA15, and it appears on the MA0 output pin in the word address mode. I the VGA is not in word address mode, MA0 counter output appears on the MA0 output pin. 0 = Selects MA13. This is selected in applications where only 64K memory is present. 1 = Selects MA15. This should be selected in odd/even mode since 256K of video memory is installed on the system board.
6	Word Mode or Byte Mode - Bit 6 of the End Vertical Blanking register in the CRT Controller also controls the addressing. When it is set to 0, bit 6 of this register has control. When it is set to 1, the addressing is forced to be shifted by two bits. 0 = The word mode shifts all memory address counter bits down one bit, and the most-significant bit of the counter appears on the least-significant bit of the memory address outputs. 1 = Selects the byte address mode.
7	Hardware Reset 0 = Forces horizontal and vertical retrace to clear. 1 = Forces horizontal and vertical retrace to be enabled.

3?5 **Line Compare Register** **Index=18** **R/W**

Bit	Description
7-0	Line Compare - This register is the low-order 8-bits of the compare target. When the vertical counter reaches this value, the internal start of the line counter is cleared. Because of this, an area of the screen is not affected by scrolling. Bit 8 is located in the Overflow register 07 hex. Bit 9 is located in the Maximum Scan Line register 09 hex.

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7.5 Graphics Controller Registers

3CE **Graphics Address Register** **R/W**

Bit	Description
3-0	Graphics Address Bits - These bits are used to point to the other registers in the graphics section
7-4	Reserved.

3CF **Set/Reset Register** **Index=0** **R/W**

Bit	Description
3-0	This field represents the value written to all 4 bits of the respective memory map when the system CPU does a memory write with write mode 0 selected and Set/Reset mode is enabled for the corresponding map.
7-4	Reserved.

3CF **Enable Set/Reset Register** **Index=1** **R/W**

Bit	Description
3-0	Enable Set/Reset - This field enables the set/reset function. 0 = If write mode is 0 and Set/Reset is not enabled on a map, that map is written with the value of the system CPU. 1 = If write mode is 0 and Set/Reset is enabled on a map, the respective memory is written with the value of the Set/Reset register.
7-4	Reserved.

3CF **Color Compare Register** **Index=2** **R/W**

Bit	Description
3-0	This field represents a 4-bit color value to be compared. If the system CPU sets read mode 1 in the graphics section and does a memory read, the data returned from the memory cycle will be a 1 in each bit position where the 4 maps equal the Color compare register. All the bits of the corresponding map's byte are compared with the value of the color compare bit. Each of the 8-bit positions of the selected byte are then compared across the 4 maps and a 1 is returned in each bit position where the bits of all 4 maps equal their respective color compare values.
7-4	Reserved.

3CF **Data Rotate Register** **Index=3** **R/W**

Bit	Description
2-0	Rotate Count - This field represents a binary encoded value of the number of positions to right-rotate the system CPU data bus during system CPU memory writes. This operation is done when write mode is 0. To write non-rotated data the system CPU must select a count of 0.
4,3	Function Select - Data written to memory can operate logically with data already in the system CPU latches. Data can be any of the choices selected by the Write Mode register except system CPU latches, which may not be modified. If rotated data is selected, the rotate applies before the logical function. The bit functions are defined as follows:

Bits 4,3	Function
00	Data unmodified
01	Data ANDed with latch data
10	Data ORed with latch data
11	Data XORed with latch data

7-5 Reserved

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3CF **Read Map Select Register** **Index=4** **R/W**

Bit	Description
1.0	Map Select - This field represents a binary encoded value of the memory map number from which the system CPU reads data. This register has no effect on the color compare read mode In odd/even modes the value may be 00 or 01 (10 or 11) for chained maps 0,1 (2,3).
7-5	Reserved

3CF **Graphics Mode Register** **Index=5** **R/W**

Bit	Description
1.0	Write Mode - The logic function specified by the Function Select register is applied to data being written to memory following modes 0,2, and 3 below. The bit functions are defined as follows

Bits 1,0	Function
00	Each memory map is written with the system CPU data rotated by the number of counts in the Rotated register, unless Set/Reset is enabled for the map. Maps for which Set/Reset is enabled are written with 8-bits of the value contained in the Set/Reset register for that map.
01	Each memory map is written with the contents of the system CPU latches. These latches are loaded by a system CPU Read operation.
10	Memory map n (0-3) is filled with 8-bits of the value of data bit n.
11	Each map is written with 8-bits of the value contained in the Set/Reset register for that map (Enable Set/Reset register has no effect). Rotated system CPU data is ANDed with the Bit Mask register data to form an 8-bit value that performs the same function as the Bit Mask register does in write modes 0 and 2.

5	Shift Register - A logical 1 instruct the Shift registers in the graphics section to format the serial data stream with even-numbered bits from both maps on the even-numbered maps and odd-numbered bits from both maps on the odd maps. This bit is used for modes 4 and 5.
6	256 Color Mode 0 = Allows bit 5 to control the loading of the Shift registers. 1 = Causes the Shift register to be loaded in a manner that supports the 256-color mode.
7	Reserved

3CF **Miscellaneous Register** **Index=6** **R/W**

Bit	Description
0	Graphics Mode - This bit controls text mode addressing control. 0 = Selects text mode operation. 1 = Selects graphics mode. When this mode is selected, the character generator address latches are disabled.
1	Odd/Even 0 = Standard VGA addressing. 1 = Replace system CPU address bit 0 with a higher-order address bit and select odd/even maps with odd/even values of the system CPU A0 bit, respectively.
3,2	Memory Map - This field controls the mapping of the regenerative buffer into the system CPU address space. The bits are defined as follows:

Bits 3,2	Function
00	Hex A0000 for 128K bytes
01	Hex A0000 for 64K bytes
10	Hex B0000 for 32K bytes
11	Hex B8000 for 32K bytes

4-7	Reserved.

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3CF	Color Don't Care Register	Index=7	R/W
Bit	Description		
0	Map 0 0 = Don't participate in the color compare cycle. 1 = Participate in the color compare cycle.		
1	Map 1 0 = Don't participate in the color compare cycle. 1 = Participate in the color compare cycle.		
2	Map 2 0 = Don't participate in the color compare cycle. 1 = Participate in the color compare cycle.		
3	Map 3 0 = Don't participate in the color compare cycle. 1 = Participate in the color compare cycle.		
7-4	Reserved.		

3CF	Bit Mask Register	Index=8	R/W
Bit	Description		
7-0	Bit Mask - Bit mask applies to write modes 0 and 2. To preserve bits using the bit mask, data must be latched internally by reading the location. When data is written to preserve the bits, the most current data it the latches is written in those positions. The bits mask applies to all map simultaneously. 0 = Any bit set to 0 causes the corresponding bit n in each map to be immune to change, provided that the location being written was the last location read by the system CPU. 1 = Bits set to 1 allow unimpeded writes to the corresponding bits in the maps.		

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7.6 Attribute Controller Registers

3C0 Attribute Address Register **R/W**

Bit	Description
4-0	Attribute Address Bits -These bits point the other registers in the Attribute section. The address and data registers share the same I/O address during write operation. An internal address flip-flop controls this selection. To initialize the flip-flop, an I/O Read instruction must be sent to the Attribute Controller at address 03BA or 03DA. This clears the flip-flop, and selects the Address register. After the Address register has been loaded with a write operation to 03C0, the next I/O write to 03C0 loads the Data register. The flip-flop toggles each time an I/O write instruction is sent to the Attribute controller.
5	Palette Address Source - Bit 5 must be cleared to 0 when loading the color Palette registers. For normal operation, bit 5 is set to 1. This enables the video memory data to access the palette registers.
7,6	Reserved

3C1/3C0 Palette Registers Hex 00 Through 0F **Index=0-F** **R/W**

Bit	Description
5-0	Palette - These bits allow a dynamic mapping between the text attribute or graphic color input value and the display color on the CRT screen. A logical 1 selects the appropriate color. The palette registers should be modified only during the vertical retrace interval to avoid problems with the display image. These internal Palette register values are sent off the chip to the video DAC, where they in turn serve as addresses into the DAC internal registers.
7,6	Reserved

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3C1/3C0	Attribute Mode Control Register	Index=10	R/W

Bit	Description
0	Graphics/Alphanumeric Mode 0 = Selects alphanumeric mode. 1 = Selects graphics mode
1	Mono Emulation 0 = Color emulation mode is set. 1 = Monochrome emulation mode is set.
2	Enable line Graphics Character Codes 0 = The ninth dot will be the same as the background. 1 = Enables the special line graphics character codes for Monochrome emulation mode. When enabled, this bit forces the ninth dot of a line graphic character to be identical to the eighth dot of the character. the line graphics character modes for the Monochrome emulation mode are C0 hex through DF hex. For character fonts that do not use the line graphics character codes this range, bit 2 should be set to 0. Otherwise, unwanted video information will be displayed on the CRT screen.
3	Enable Blink/Select Background Intensity 0 = Selects the background intensity of the attribute input, which was available on the Monochrome and CGA adapters. 1 = Enables the blink attribute in text modes and blinking graphics modes.
4	Reserved
5	PEL Panning Compatibility 0 = Line compare has no effect on the output of the PEL Panning register. 1 = A successful line compare in the CRT controller forces the output of the PEL Panning registers to 0 until +VSYNC occurs, at which time the output returns to its programmed value. This bit allows a selected portion of the screen to be panned.
6	PEL Width 0 = All modes except for mode 13 hex. 1 = The video pipeline is sampled so that 8-bits are available to select a color in the 256-color mode (hex 13).
7	P5,P4 Select - This bit selects the source for the P5 and P4 digital video bits that go off the chip. 0 = P5 and P4 are the outputs of the Palette registers 1 = P5 and P4 are bits 1 and 0 of the Color Select register.

3C1/3C0	Overscan Color Register	Index=11	R/W

Bit	Description
7-0	Overscan Color- This register determines the overscan (border) color displayed on the CRT screen. This border is a band of color around the perimeter of the display area. Its width is defined by the time when display enable and blank are both inactive and is not supported in the 40-column text modes or the 320-PEL graphics modes, except for mode 13 hex.

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3C1/3C0	**Color Plane Enable Register**	**Index=12**	**R/W**

Bit	Description
3-0	Enable Color Plane - Setting any of these bits to 1 enables the respecuve display memory color plane.
5,4	Video Status MUX - Selects two of the eight color outputs to be available on the status port The combinations available and the color output wiring are shown below:

Color Plane Register Bits 5,4	Input Status Register 1 Bits 5,4
00	P2, P0
01	P5, P4
10	P3, P1
11	P7, P6

6,7	Reserved.

3C1/3C0	**Horizontal PEL Panning Register**	**Index=13**	**R/W**

Bit	Description
3-0	Horizontal PEL Panning - This register selects the number of picture elements (PELs) to shift the video data horizontally to the left. PEL panning is available in both graphics and text modes In monochrome emulation text modes and modes 0+, 1+, 2+, 3+ , the image can be shifted a maximum of 8 PELs. Mode 13 allows a maximum shift of 3 PELs. All other modes, the image can be shifted a maximum of 7 PELs. The sequence for shifting the image is as follows.

PEL Panning Register Value	Number of PELs Shifted to the left 0+,1+,2+,3+,7,7+	All Other modes	Mode 13
0	1	0	0
1	2	1	-
2	3	2	1
3	4	3	-
4	5	4	2
5	6	5	-
6	7	6	3
7	8	7	-
8	0	-	-

7-4	Reserved

3C1/3C0	**Color Select Register**	**Index=14**	**R/W**

Bit	Description
1,0	S_color 4,5 - These two bits can be used in place of the P4 and P5 bits from the Attribute Palette registers to form the 8-bit digital color value sent off-chip. this feature is used to rapidly switch between sets of colors in the video DAC.
3,2	S_color 6,7 - These two bits are the two high-order bits of the 8-bit digital color value sent off-chip in all modes but the 256 color graphics. In the 256-color graphics, the 8-bit attribute stored in video memory becomes the 8-bit digital color value set off-chip to the video DAC. These bits are also used to rapidly switch between sets of colors in the video DAC.
7-4	Reserved

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7.7 DAC Registers

The following registers are external registers, the VGA controller only genrates DACRDn/DACWRn and route the data for DAC.

3C6	**PEL Mask**	R/W
3C7	**DAC State Register**	RO
3C7	**PEL Address (Read Mode)**	WO
3C8	**PEL Address (Write Mode)**	R/W
3C9	**PEL Data Register**	R/W

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8 DC SPECIFICATION

8.1 Absolute Maximum Ratings

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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8.2 DC Characteristics

TA = 0° C to 70° C, VDD = 5V +/- 5%, VSS = 0V

Symbol	Parameter	Min	Max	Unit	Condition	Notes
V_{oh}	Output High Voltage	2.4		V	I_{oh} = 400 uA	
V_{ol}	Output Low Voltage		0.4	V	I_{ol} = 24 mA	1,2
V_{ol}	Output Low Voltage		0.4	V	I_{ol} = 12 mA	1
V_{ol}	Output Low Voltage		0.4	V	I_{ol} = 10 mA	1
V_{ol}	Output Low Voltage		0.4	V	I_{ol} = 8 mA	1
V_{ol}	Output Low Voltage		0.4	V	I_{ol} = 4 mA	1
V_{ol}	Output Low Voltage		0.4	V	I_{ol} = 2 mA	1
V_{ih}	Input High Voltage	2	VCC+0.5	V	TTL	3
V_{il}	Input High Voltage	-0.5	0.8	V	TTL	3
V_{st}	Schmitt Input Voltage	2.4	VCC+.05	V	Schmitt	3
V_{ic}	CMOS Input Voltage	3.8	VCC+0.5	V	CMOS	3
ILI	Input Leakage Current	-10	10	uA		
OLI	Output Leakage Current	-10	10	uA		
ICC	Operating Supply Current		500	mA	Input=VCC or GND No Output Load	
CI	Input Capacitance		8	pF		
CO	Output Capacitance		8	pF		
CIO	I/O Capacitance		8	pF		

Notes: Other than ISA bus interface and Monitor interface, there is no DC requirements on the outputs. The other interfaces only have AC requirements.

1. Output Current (Iol) Capabilities:
   - 24mA: SD[15:0] (ISA)
   - 8mA: HSYNC, VSYNC
2. Open Drain Outputs:
   - 24mA: IOCHRDY, CINTn, IO16n, M16n, ZEROWSn (ISA)
3. Input Structures:
   - TTL: All inputs
   - TTL w/ pull-ups: ESYNC, EPDATA, EPCLK

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9 AC SPECIFICATION

All AC Timing Diagrams are strictly to show relative timing from one signal to the next. These diagrams are not necessarily logically correct or complete. For better understanding of logical cycles for ISA, VL and PCI bus, please refer to the respective specifications.

The AC values in here are design target values, not designed values or tested values.

9.1 ISA Bus Timing

9.1.1 ISA Memory Read/Write Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
	tBCLK	*ISA Bus Clock Period*	*80*			1
ISA1	tALE	ALE Active to Inactive	40			
ISA2	tLAS	LA[23:17] Setup to Falling Edge of ALE	15			
ISA3	tLAH	LA[23:17] Hold from Falling Edge of ALE	10			
ISA4	tM16	M16n Active from Valid LA[23:17]		40	200	
ISA5	tASMC	SA[16:0] & BHEn Setup to Memory Command Active	20			
ISA6	tAHMC	SA[16:0] & BHEn Hold to Memory Command Inactive	20			
ISA7	tMCP	Memory Command Pulse Width	80			
ISA8	t0WS	ZEROWSn Delay from Command		10	200	
ISA9	tMRDY	IOCHRDY Inactive from Memory Command Active		30	200	
ISA10	tDVMR	Read Data Valid from MRDn Active		160	200	2
ISA11	tDVRDY	Read Data Valid from IOCHRDY Active		50	200	
ISA12	tDHMR	Read Data Hold from MRDn Inactive	0		200	
ISA13	tDSMW	Write Data Setup to MRWn Active	-45			
ISA14	tDHMW	Write Data Hold from MWRn Inactive	15			

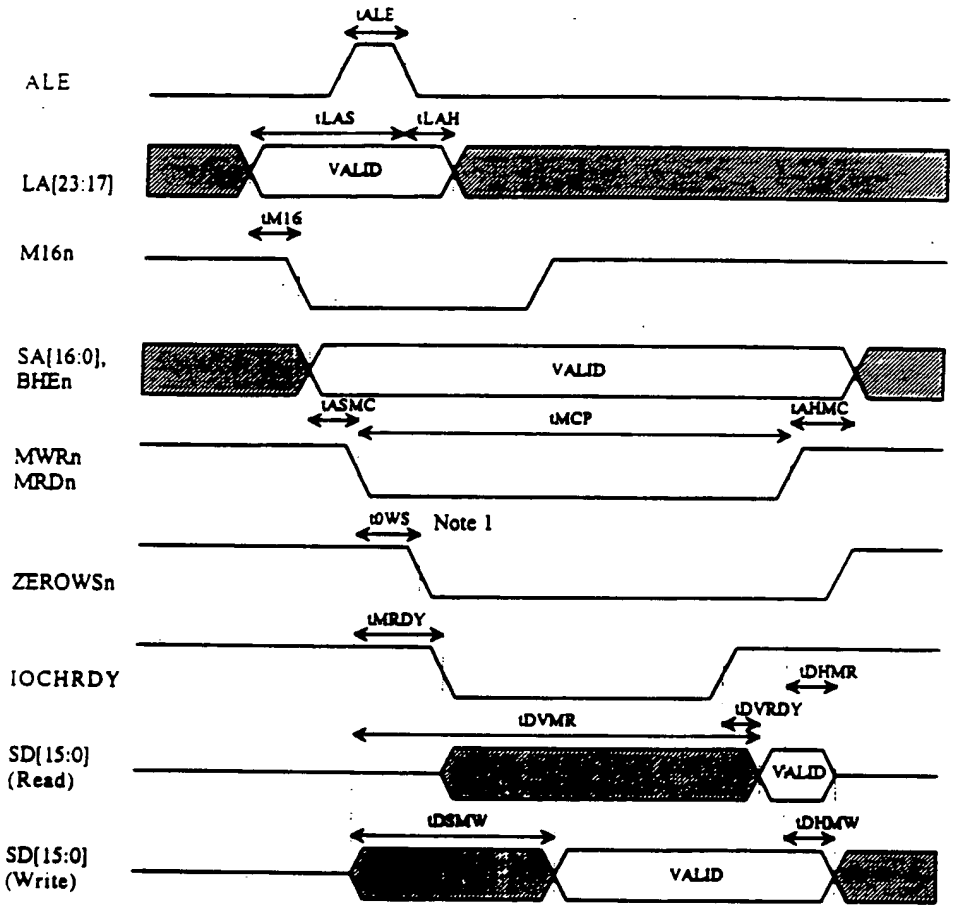
Notes:

1. This parameter is for reference only. It is intended to be the recommanded maximum bus speed. The design of this controller, however, is asynchronous to the BCLK, and therefore theoretically can run at any BCLK, as long as setup, hold and propagation delay timings met all the above specifications.
2. tDVMR is valid for memory mapped I/O only, which is standard memory read cycle (1 wait state). Normal read access to graphics memory requires wait states, and only tDVRDY is of interest.

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ISA Memory Read/Write Timing



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Notes:

1. ZEROWSn and IOCHRDY are mutually exclusive, only one signal can be active at time. The drawing merely indicates the AC timing of the signals, but not the actual logical cycle timing.

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9.1.2 ISA ROM Read Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
ISA1	tALE	ALE Active to Inactive	40			
ISA2	tLAS	LA[23:17] Setup to Falling Edge of ALE	15			
ISA3	tLAH	LA[23:17] Hold from Falling Edge of ALE	10			
ISA4	tM16	M16n Active from Valid LA[23:17]		40	200	1
ISA5	tASMC	SA[16:0] & BHEn Setup to Memory Command Active	23			4
ISA6	tAHMC	SA[16:0] & BHEn Hold from Memory Command Inactive	20			
ISA7	tMCP	Memory Read Command Pulse Width	80			3
ISA15	tRE	ROMENLn Active from MRDn Active		40	50	1,4
	tROMA	*ROM Data Valid from SA[14:0]*		*48/448*	*50*	2,3,4
	tROME	*ROM Data Valid from MRDn*		*125/425*	*50*	2,4
ISA16	tBDSD	BD[7:0] Valid to SD[15:0] Valid		35	200	4
	t244P	*ROM Data Valid to SD[15:8] Valid through 244 Buffer*		*35*	*200*	1,4,5
ISA10	tDVMR	Read Data Valid from MRDn Active		160/460	200	3,4,6
ISA12	tDHMR	Read Data Hold from MRDn Inactive	0		200	

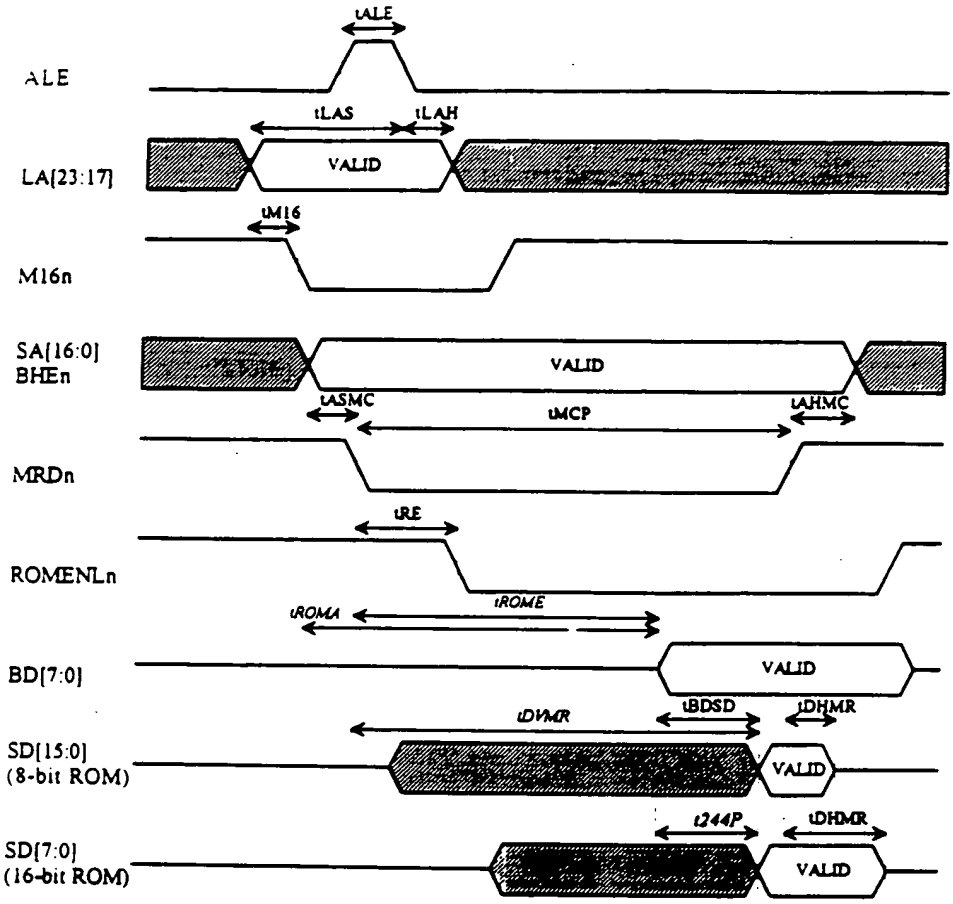
Notes:

1. These parameters are relevant only for 16-bit ROM (2 pieces). For 8-bit ROM, M16n is not generated, ROMENLn is "don't care", and no additional buffer required.
2. This specification is for reference only. This is the required ROM access timing. Depending on tASMC, tROMA or tROME can be used to select the correct ROM speed. In general, 120ns ROM should be used for 8.33MHz. Faster bus will require faster ROM. See note 4 for more details.
3. A/B where A is for 16-bit ROM, and B is for 8-bit ROM.
4. tDVMR is the specification that must be met. The calculation for tDVMR is not straight forward. If tROMA-tROME>tASMC, then tDVMR=tROMA-tASMC+tBDSD for 8-bit ROM, or for SD[7:0] of 16-bit ROM, and tDVMR=tROMA-tASMC+t244 for SD[15:8] of 16-bit ROM. If tASMC>tROMA-tROME, then tDVMR=tROME+tBDSD for 8-bit ROM, or for SD[7:0] of 16-bit ROM, and tDVMR=tROME+t244 for SD[15:8] of 16-bit ROM.
5. This specification is for reference only. The general rule of thumb is that the speed of the 244 buffer should not be more than tBDSD. See note 4 for more details.
6. tDVMR as specified here is based on 8.33MHz bus, this number is reduced for faster bus, and there is no standard for it.

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ISA ROM Read Timing



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9.1.3 ISA General I/O Access Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
ISA17	tASIO	SA[15:0] & BHEn Setup to I/O Command Active	25			
ISA18	tAHIO	SA[15:0] & BHEn Hold from I/O Command Inactive	25			
ISA19	tIOCP	I/O Command Pulse Width	115			
ISA20	tIO16	IO16n Active from Valid SA[15:0]		60	200	
ISA21	tDVIR	Read Data Valid from IORn Active		70	200	
ISA22	tDVRDY	Read Data Valid from IOCHRDY Active		50	200	
ISA23	tDHIR	Read Data Hold from IORn Inactive	0		200	
ISA24	tDIVW	Write Data Valid from IOWn Active	-55			
ISA25	tDHIW	Write Data Hold from IOWn Inactive	15			
ISA26	tIORDY	IOCHRDY Inactive from I/O Command Active		30	200	1

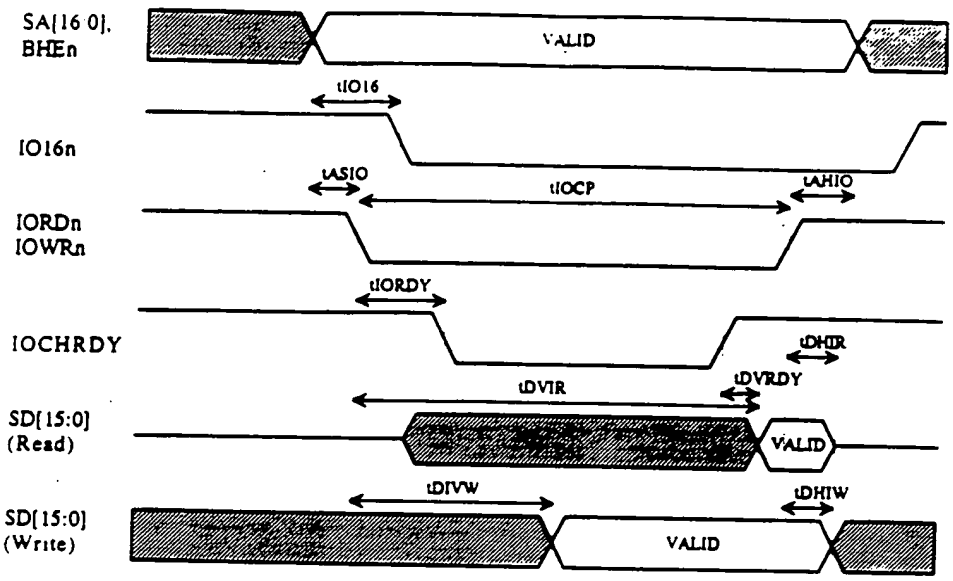
Notes:

1. IOCHRDY is normally not needed for I/O cycles. It is needed for special reset sequence and power saving modes only.

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ISA General I/O Access Timing



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9.1.4 ISA DAC & Auxiliary I/O Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
ISA17	tASIO	SA[15:0] & BHEn Setup to I/O Command Active	25			
ISA18	tAHIO	SA[15:0] & BHEn Hold from I/O Command Active	25			
ISA19	tIOCP	I/O Command Pulse Width	115			
ISA27	tICDC	DAC Command Delay from I/O Command		25	50	
	tRLQV	*DAC Data Valid from DACRDn*		*395*	*50*	1
	tDVIR8	*SD[15:0] Valid from IORDn for DAC or Auxiliary Cycle*		*460*	*200*	2
ISA23	tDHIR	Read Data Hold from IORn Inactive	0		200	
ISA24	tDVIW	Write Data Valid from IOWn Active	-55			
ISA25	tDHIW	Write Data Hold from IOWn Inactive	15			
ISA28	tDWP	DACWRn Pulse Width	70			
ISA29	tSDBD	SD[7:0] Valid to BD[7:0] Valid		40	50	
ISA30	tBDSD	BD[7:0] Valid to SD[15:0] Valid		40	200	
ISA31	tACSn	Auxiliary Chip Select Delay from SA[15:0]		20	50	

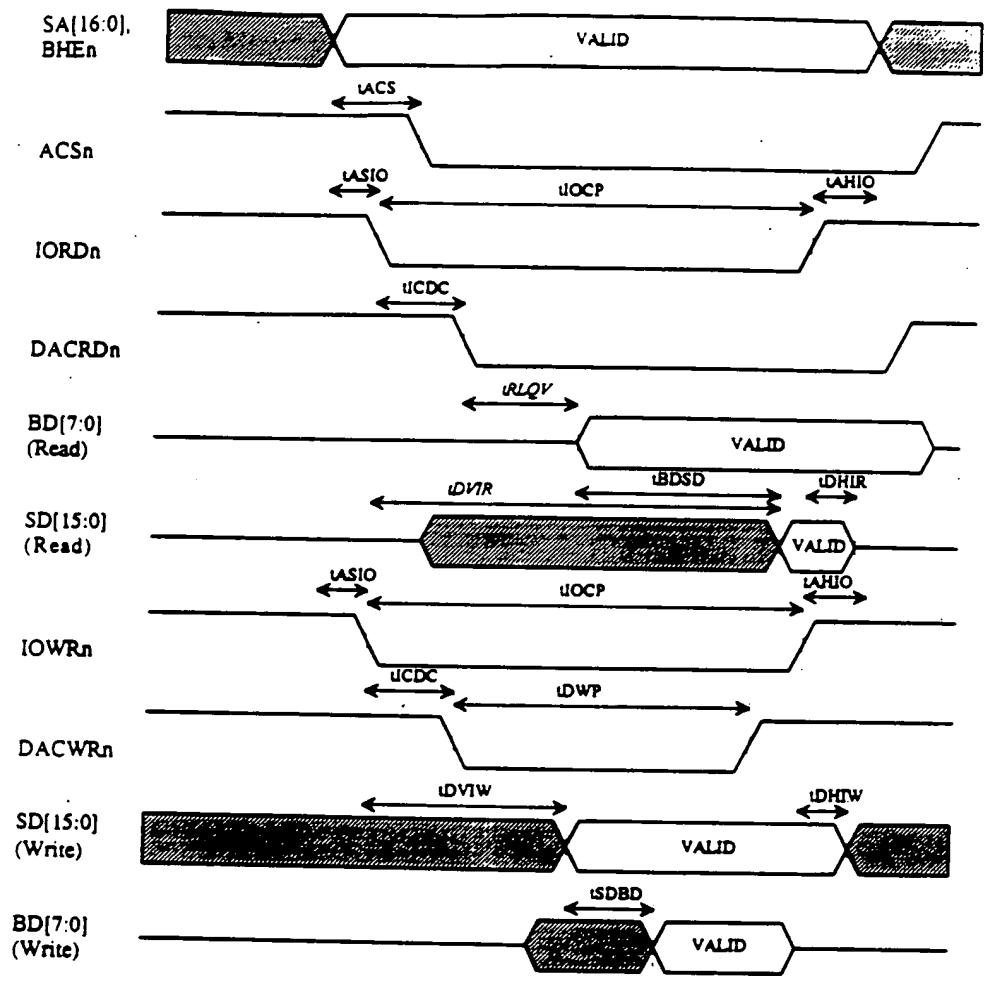
Notes:

1. This is for reference only. This specification belongs to the DAC I/O access time.
2. This is for reference only. This is the specification for 8-bit I/O ISA bus. The real data valid time for the DAC should be calculated as follow: tDVIR=tICDC+tRLQV+tBDSD.

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ISA DAC & Auxiliary I/O Timing



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9.2 VL Bus Timing

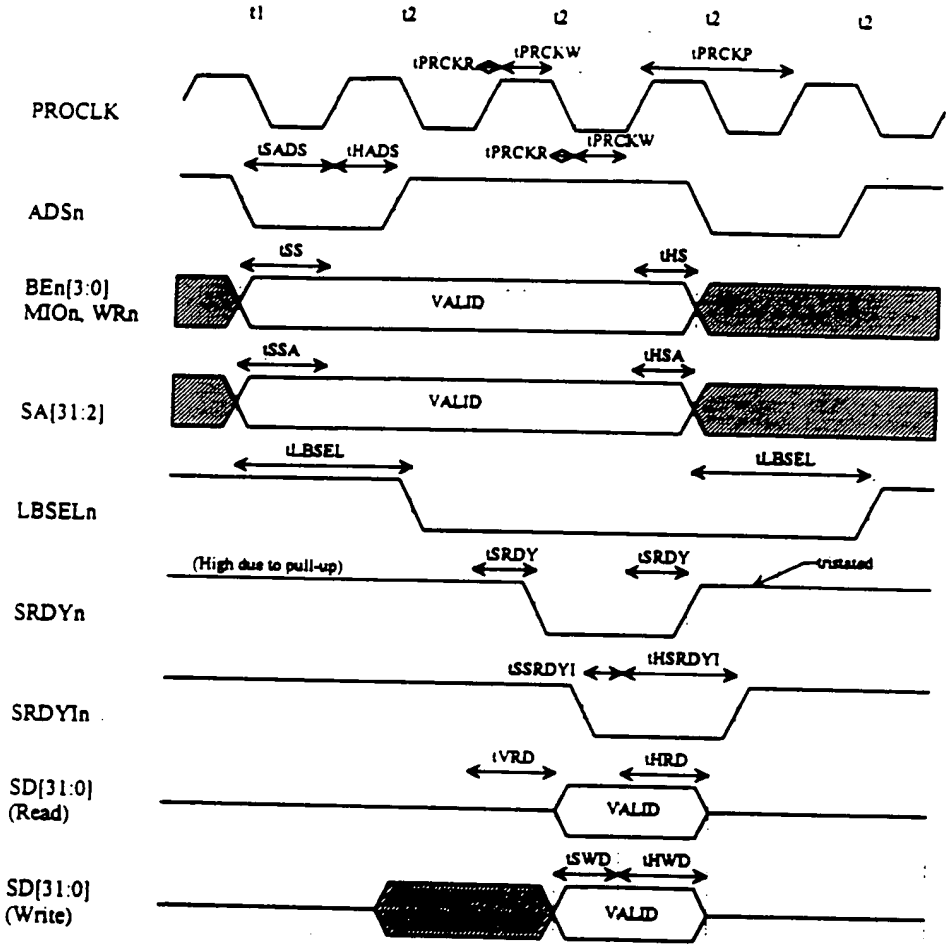
9.2.1 VL Bus Interface Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
VL1	tPRCKP	Processor Clock Period	20			
VL2	tPRCKW	Processor Clock Pulse Width	8			
VL3	tPRCKR	Processor Clock Rise/Fall		2		
VL4	tSADS	ADS Setup Time	4			
VL5	tHADS	ADS Hold Time	2			
VL6	tSSA	Address Setup Time	4			
VL7	tHSA	Address Hold Time	2			
VL8	tSS	Status Setup Time	4			
VL9	tHS	Status Hold Time	2			
VL10	tLBSEL	LBSELn Valid from SA[31:2] & Status		20	25	
VL11	tSRDY	SRDYn Delay Time		13	75	
VL12	tSSRDYI	SRDYI Setup Time	5			
VL13	tHSRDYI	SRDYI Hold Time	2			
VL14	tVRD	Read Data Delay Time	3	14	125	
VL15	tHRD	Read Data Hold Time		2	125	
VL16	tSWD	Write Data Setup Time	4			
VL17	tHWD	Write Data Hold Time	2			

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VL Bus Interface Timing



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9.2.2 VL ROM Read Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
VL4	tSADS	ADS Setup Time	4			
VL5	tHADS	ADS Hold Time	2			
VL6	tSSA	Address Setup Time	4			
VL7	tHSA	Address Hold Time	2			
VL8	tSS	Status Setup Time	4			
VL9	tHS	Status Hold Time	2			
VL18	tDOE	DOEn Delay from ISACMD		25	50	
ISA5	tASMC	SA[14:0] Setup to MRDn Active	23			
ISA6	tAHMC	SA[14:0] Hold from MRDn Inactive	20			
	tDVMR	*Read Data Valid from MRDn Active*		*460*	*200*	1,3
	tADSIC	*ISA Command (MRDn) Active Delay from ADSn*		*?*		1,2
	tROMA	*ROM Data Valid from SA[14:0]*		*448*	*50*	1
	tROME	*ROM Data Valid from MRDn Active*		*425*	*50*	1
	tROMO	*ROM Data Float from MRDn Inactive*	*0*		*50*	1
	t10P	*ISACMD Active from MRDn through LS10*		*35*	*50*	1
	t245P	*ROM Data Valid to SD[7:0] Valid through 245 Buffer*		*35*	*200*	1
	t245E	*DOEn Valid to SD[7:0] Valid through 245 Buffer*		*35*	*200*	1
	t245O	*SD[7:0] Tristated from DOEn Inactive through 245 Buffer*		*35*	*200*	1

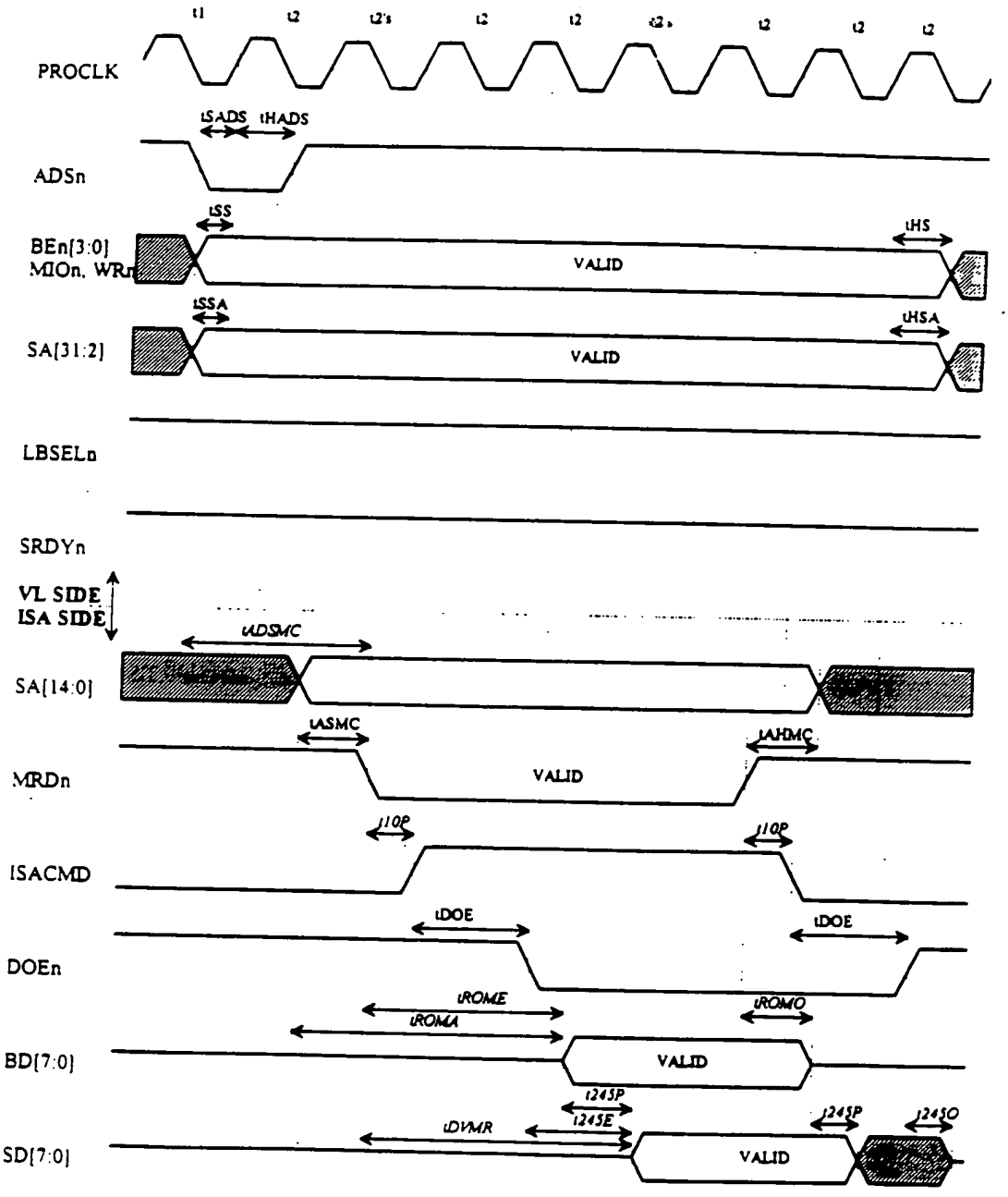
Notes:

1. These parameters are for reference only.
2. This parameter is chipset dependent. A reasonable calculation for tADSMC should be as follow: tADSMC=(2*tPRCKP)+(2*tBCLK).
3. This is the required specification for 8-bit Memory on ISA bus. The actual timing can be calculated in two different ways, whichever worst is the number to use. 1) tDVMR=tROME+t245P, or 2) tDVMR=tROMA+t245P-tASMC.

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VL ROM Read Timing



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9.2.3 VL DAC I/O Read Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
VL4	tSADS	ADS Setup Time	4			
VL5	tHADS	ADS Hold Time	2			
VL6	tSSA	Address Setup Time	4			
VL7	tHSA	Address Hold Time	2			
VL8	tSS	Status Setup Time	4			
VL9	tHS	Status Hold Time	2			
	t10P	*ISACMD Active from IORn through LS10*		*35*	*50*	1
VL18	tDOE	DOEn Delay from ISACMD		25	50	
VL19	tDCDC	DAC Command Delay from ISACMD		25	50	4
	tADSIC	*ISA Command (IORn) Active Delay from ADSn*		?		1,2
	tRLQV	*DAC Data Valid from DACRDn*		*395*	*50*	1
	tDVIR8	*SD[15:0] Valid from IORDn for DAC Cycle*		*460*	*200*	1,3
	t245P	*DAC Data Valid to SD[7:0] Valid through 245 Buffer*		*40*	*200*	1

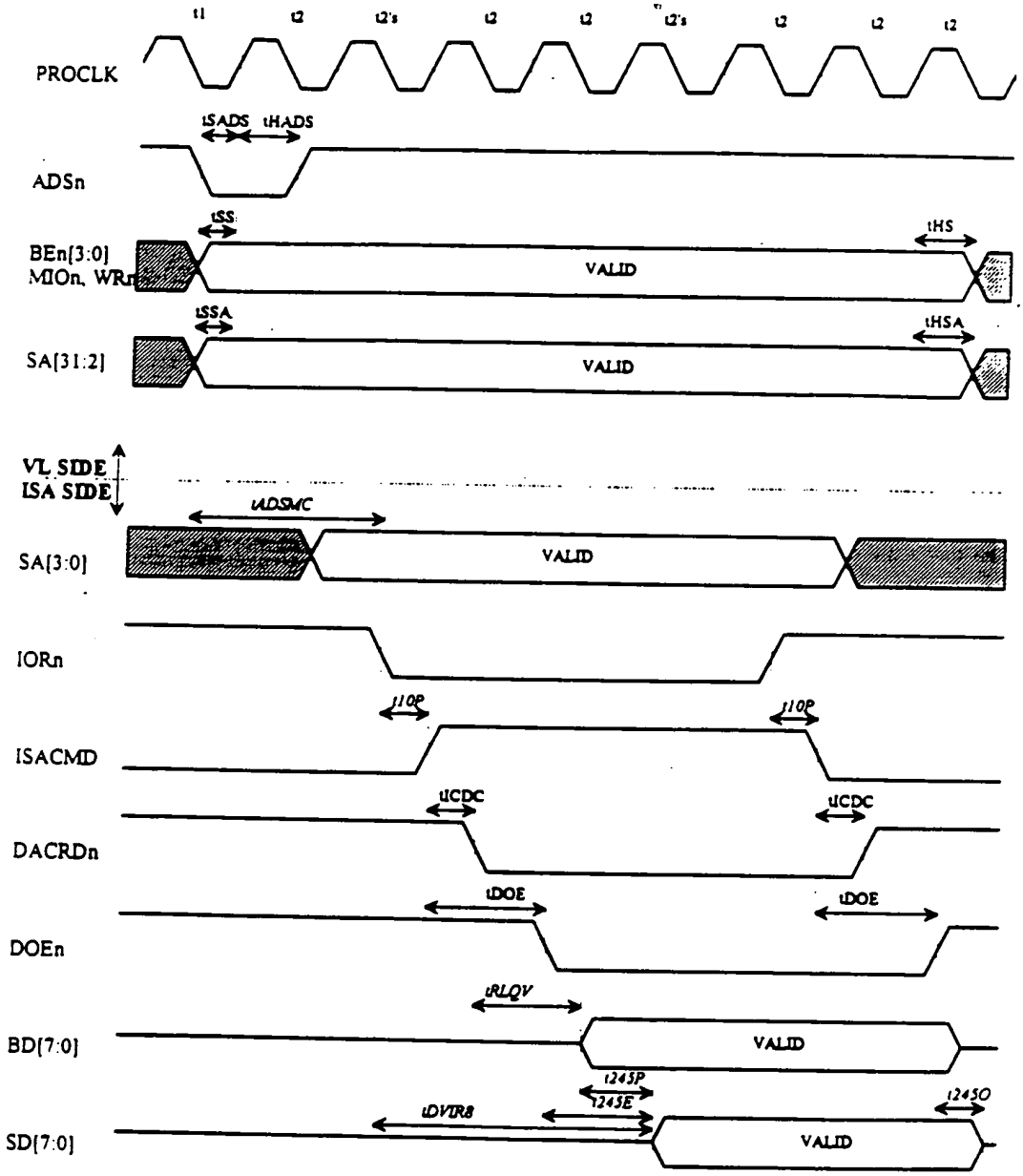
Notes:

1. These parameters are for reference only.
2. Thid parameter is chipset dependent. A reasonable calculation for tADSMC should be as follow: tADSMC=(2*tPRCKP)+(2*tBCLK).
3. This is the required specification for 8-bit Memory on ISA bus. The actual timing can be calculated as follow: tDVIR8=t10P+tDCDC+tRLQV+t245P.
4. Although this parameter is similar to ISA27 parameter, it is essential to test this under VL configuration because the address decoding is from VL bus.

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VL DAC I/O Read Timing



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9.2.4 VL DAC I/O Write Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
VL4	tSADS	ADS Setup Time	4			
VL5	tHADS	ADS Hold Time	2			
VL6	tSSA	Address Setup Time	4			
VL7	tHSA	Address Hold Time	2			
VL8	tSS	Status Setup Time	4			
VL9	tHS	Status Hold Time	2			
	t10P	*ISACMD Active from IOWn through LS10*		*35*	*50*	1
VL18	tDOE	DOEn Delay from ISACMD		25	50	
VL19	tDCDC	DAC Command Delay from ISACMD		25	50	2
ISA24	tDVIW	Write Data Valid from IOWn Active	-55			
ISA28	tDWP	DACWRn Pulse Width	70			
	t245D	*DACWRn Valid to BD[7:0] Valid through 245 Buffer (DIR)*		*35*	*50*	1
	t245E	*DOEn Valid to BD[7:0] Valid through 245 Buffer (OEn)*		*35*	*50*	1
	t245P	*SD[7:0] Valid to BD[7:0] Valid through 245 Buffer (A-B)*		*35*	*50*	1

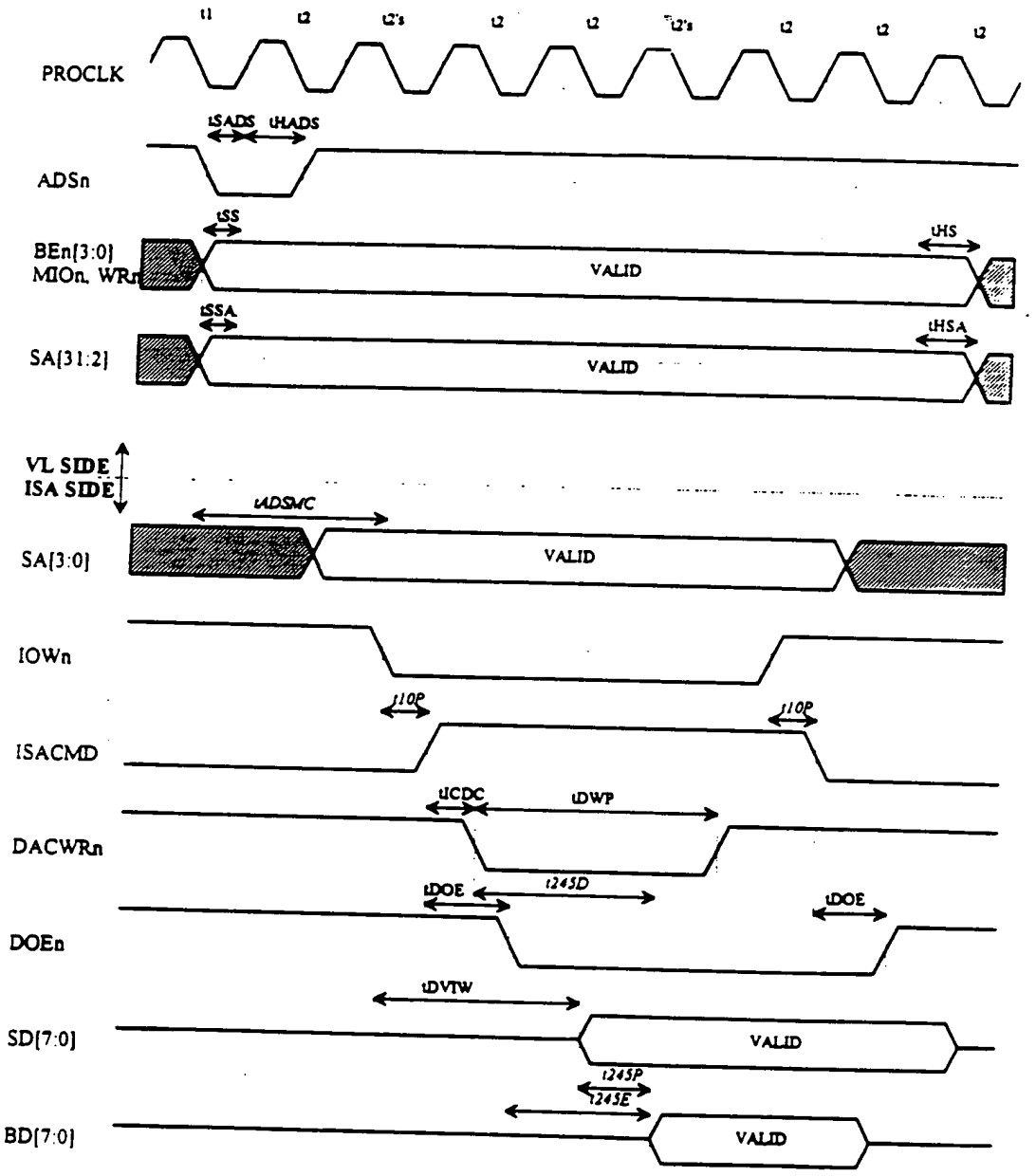
Notes:

1. These parameters are for reference only.
2. Although this parameter is similar to ISA27 parameter, it is essential to test this under VL configuration because the address decoding is from VL bus.

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VL DAC I/O Write Timing



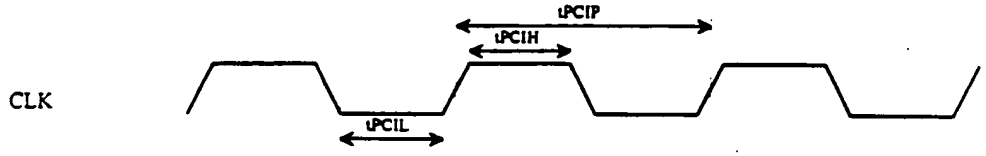
ATI033429

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9.3 PCI Bus Timing

9.3.1 PCI Bus Clock Requirement

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI1	tPCKP	PCI Bus Clock Period	30			
PCI2	tPCKL	PCI Bus Clock Low Time	12			
PCI3	tPCKH	PCI Bus Clock High Time	12			

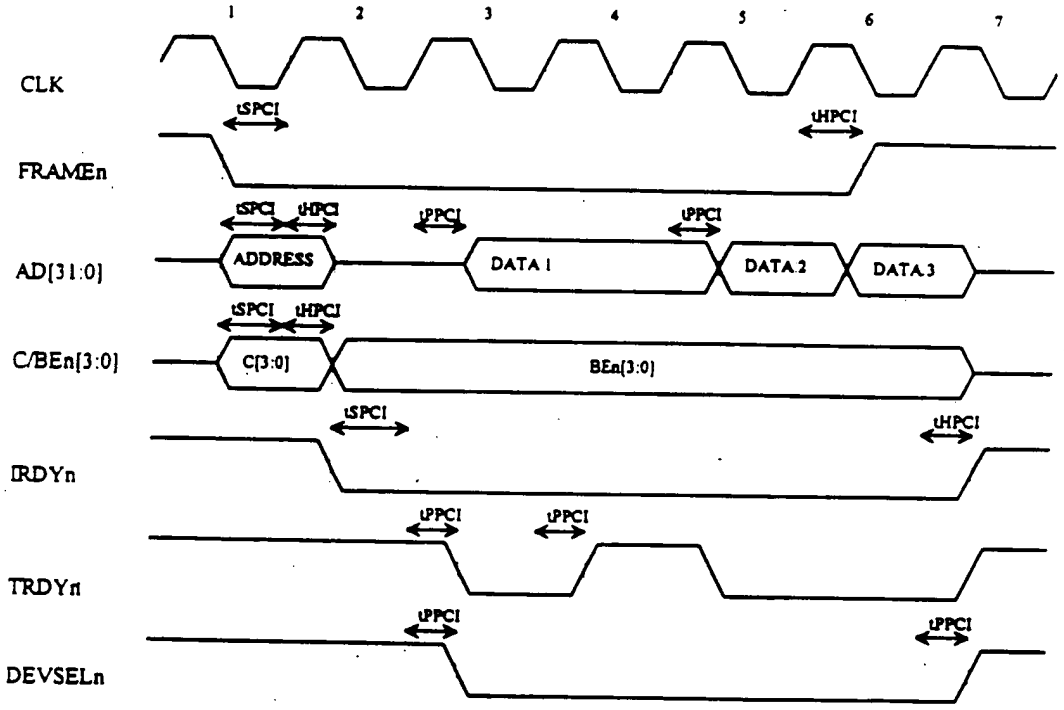


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9.3.2 PCI Bus Timing (Read Operation)

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI4	tSPCI	Input Setup Time to CLK	7			
PCI5	tHPCI	Input Hold Time to CLK	0			
PCI6	tPPCI	Ouput Propagation Delay from CLK	2	11	0/50	1



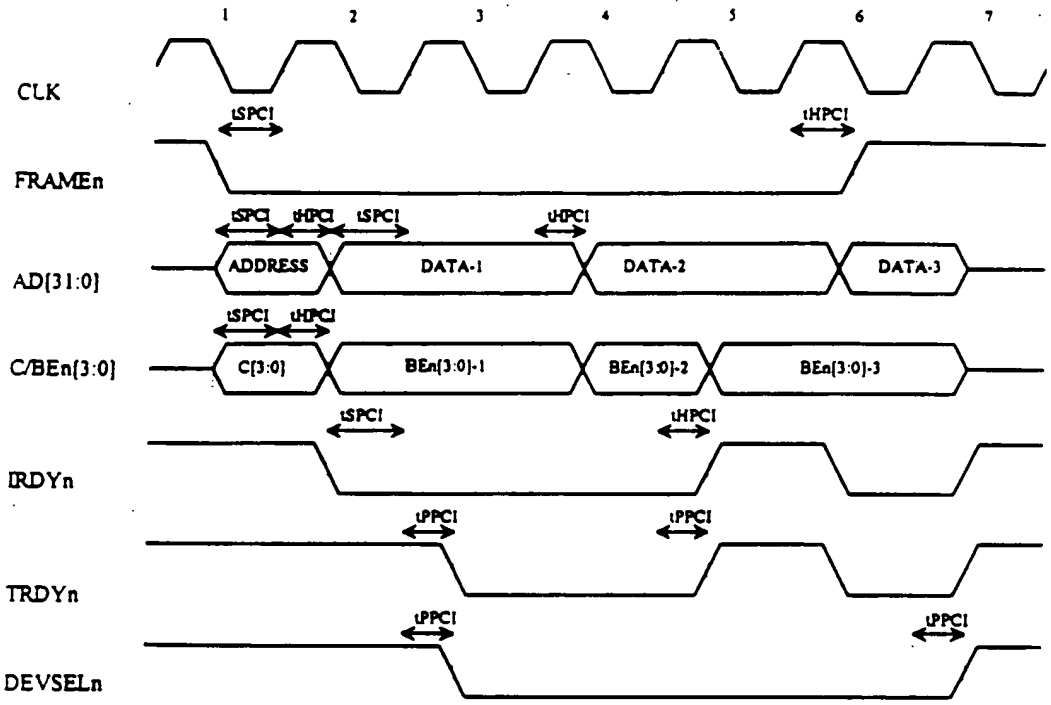
Notes:

1. Minimum timing is when load=0pF, and maximum timing is when load=50pF

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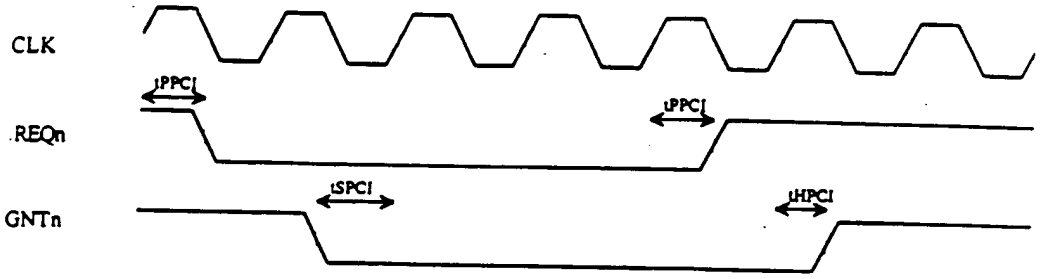
9.3.3 PCI Bus Timing (Write Operation)



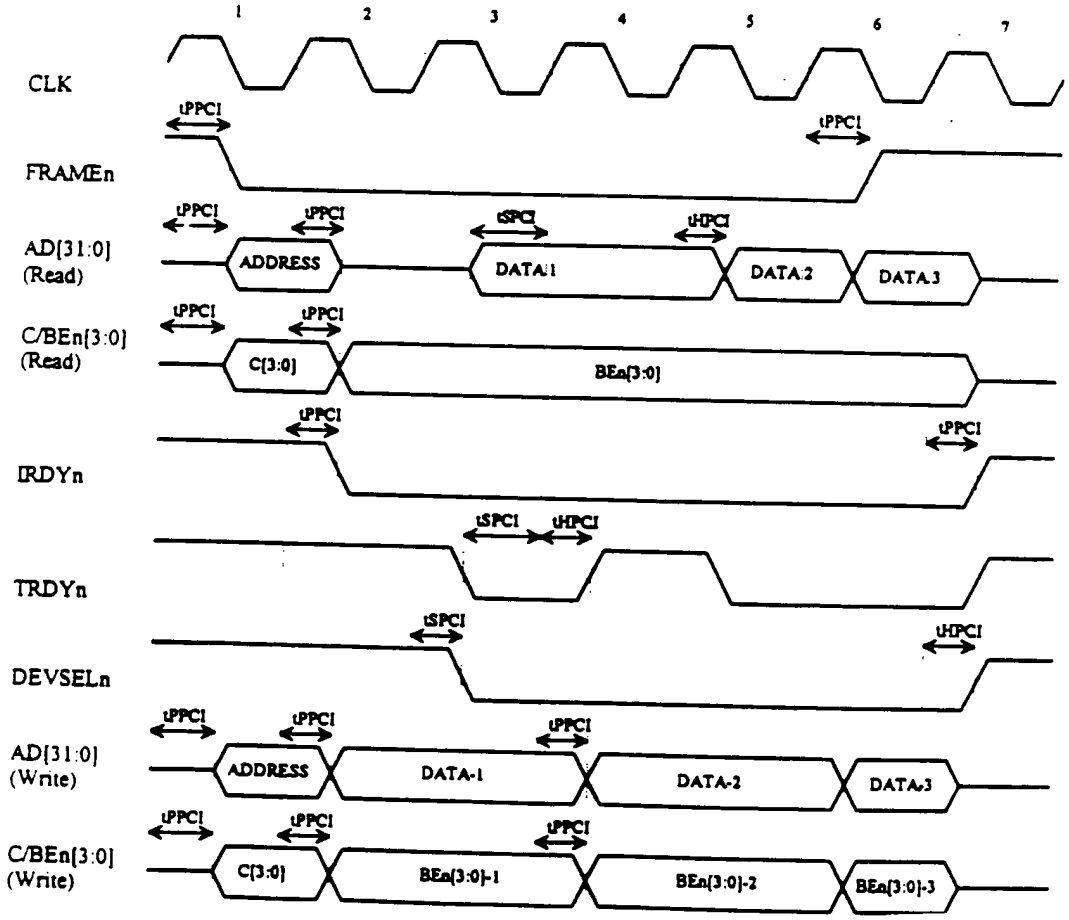
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9.3.4 PCI Bus Master Request Timing



9.3.5 PCI Bus Master Read/Write Timing



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9.3.6 PCI ROM Read Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI4	tSPCI	Input Setup Time to CLK	7			
PCI5	tHPCI	Input Hold Time to CLK	0			
PCI6	tPPCI	Ouput Propagation Delay from CLK	2	11	0/50	1
PCI7	tROMENL	ROMENLn Delay from CLK		25	50	
	tROMA	*ROM Data Valid from RA[14:0] (AD[30:16])*		*120*	*50*	2
	tROME	*ROM Data Valid from ROMENLn*		*60*	*50*	2
	tROMO	*ROM Data Float from ROMENLn*		*55*	*50*	2

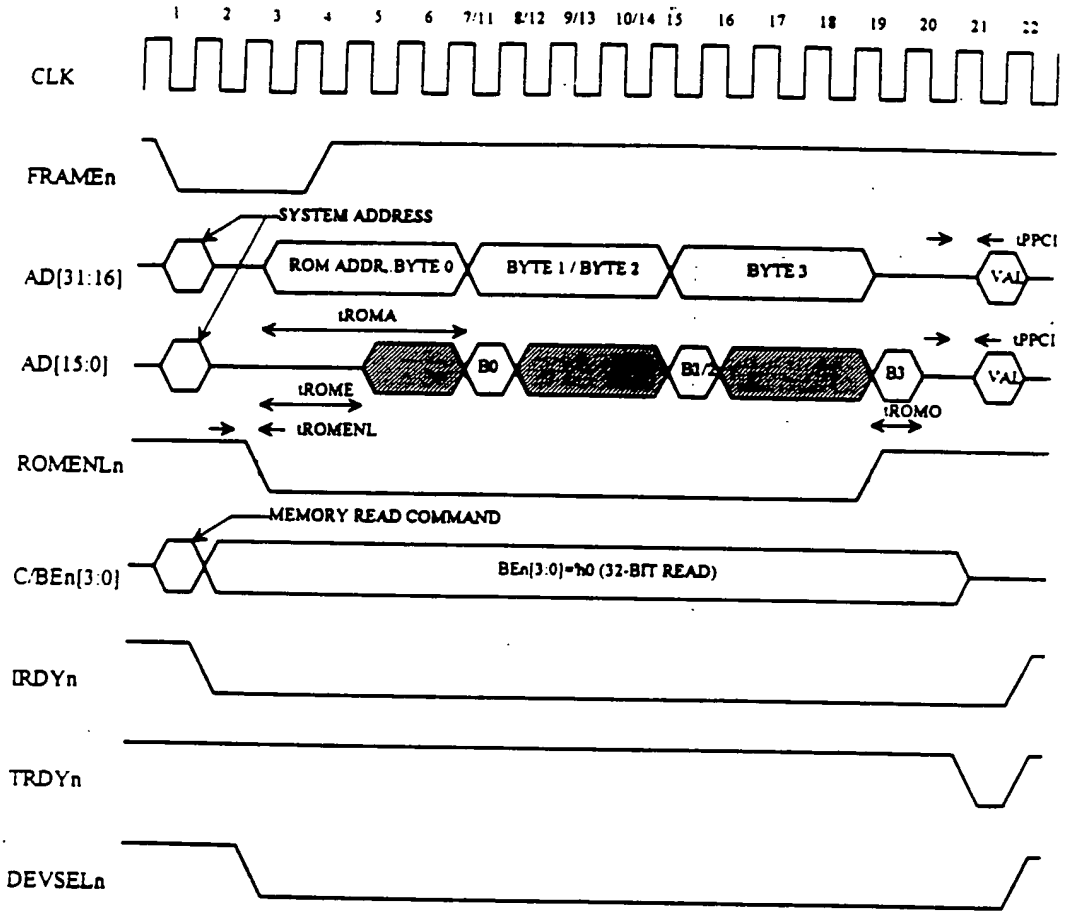
Notes:

1. Minimum timing is when load=0pF, and maximum timing is when load=50pF
2. These parameters are for reference only. They can be used to choose the appropriate EPROM speed. These requirements are based on the bus clock being 33MHz.

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PCI ROM Read Timing



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9.3.7 PCI DAC & Auxiliary I/O Timing

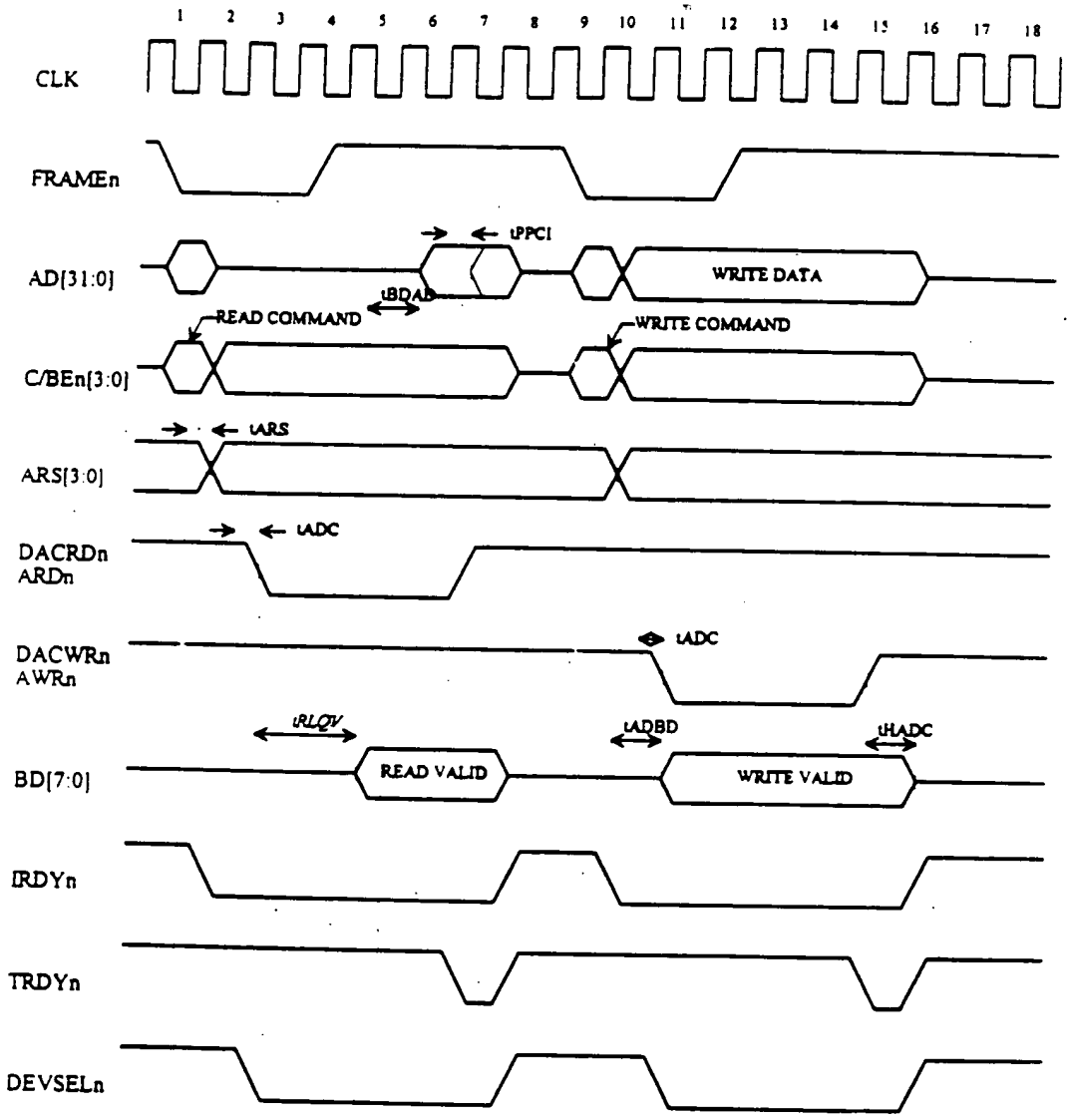
No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
PCI4	tSPCI	Input Setup Time to CLK	7			
PCI5	tHPCI	Input Hold Time to CLK	0			
PCI6	tPPCI	Ouput Propagation Delay from CLK	2	11	0/50	1
PCI8	tARS	ARS[3:0] Delay from CLK		25	50	
PCI9	tADC	Auxiliary or DAC Command Delay from CLK		25	50	
PCI10	tBDAD	BD[7:0] Valid to AD[31:0] Valid		40	50	
PCI11	tADBD	AD[31:0] Valid to BD[7:0] Valid		40	50	
PCI12	tHADC	BD[7:0] Valid Hold from DACWRn/AWRn Inactive	tPCIP		50	
	tRLQV	*BD[7:0] Valid from ARDn or DACRDn*		*65*	*50*	2

Notes:

1. Minimum timing is when load=0pF, and maximum timing is when load=50pF
2. This parameter is for reference only. They can be used to choose the appropriate DAC or Auxiliary I/O speed. These requirements are based on the bus clock being 33MHz.

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PCI DAC & Auxiliary I/O Timing



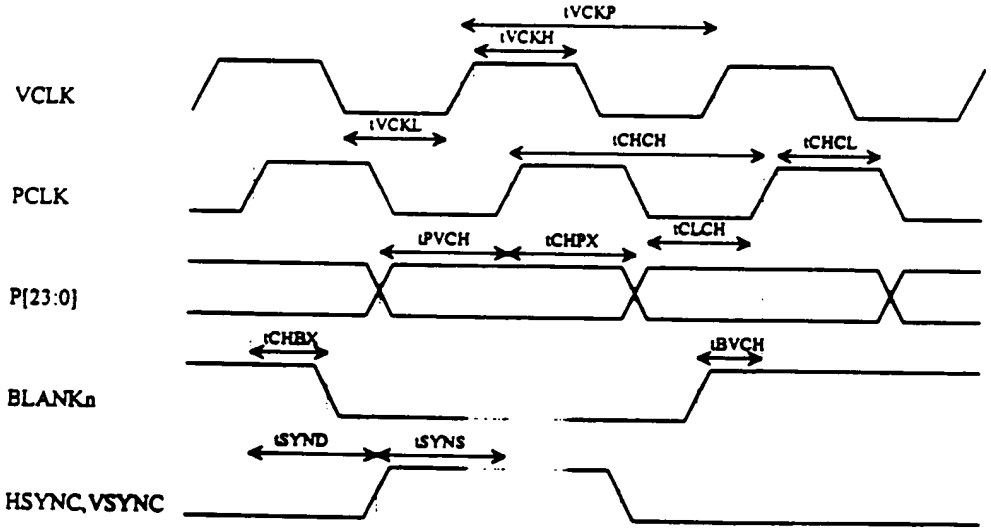
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9.4 DAC Interface Timing

9.4.1 DAC Pixel Port Interface Timing

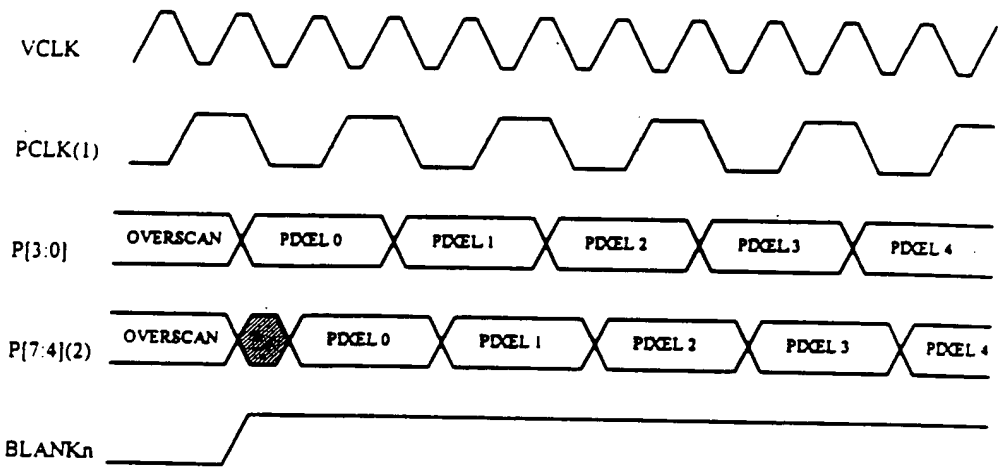
No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
DAC1	tVCKP	Video Clock Period	9			
DAC2	tVCKL	Video Clock Low Time	3			
DAC3	tVCKH	Video Clock High Time	3			
DAC4	tCHCH	Pixel Clock Period	9		50	1
DAC5	tCLCH	Pixel Clock Low Time	3		50	
DAC6	tCHCL	Pixel Clock High Time	3		50	
DAC7	tPVCH	P[23:0] Setup to PCLK	2		50	1
DAC8	tCHPX	P[23:0] Hold to PCLK	2		50	
DAC9	tBVCH	BLANKn Setup to PCLK	2		50	1
DAC10	tCHBX	BLANKn Hold to PCLK	2		50	



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9.4.2 DAC Interface - Attribute Mode 0, VGA Mode 13 (8bpp, 8-bit port)



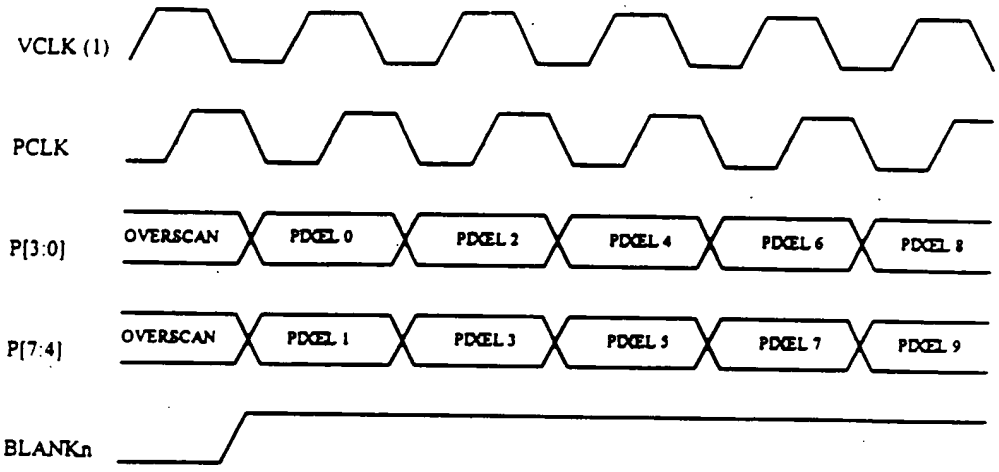
Notes:

1. PCLK frequency is half that of VLCK frequency.
2. Nible P[7:4] is one VCLK delayed from nible P[3:0] for the same pixel.

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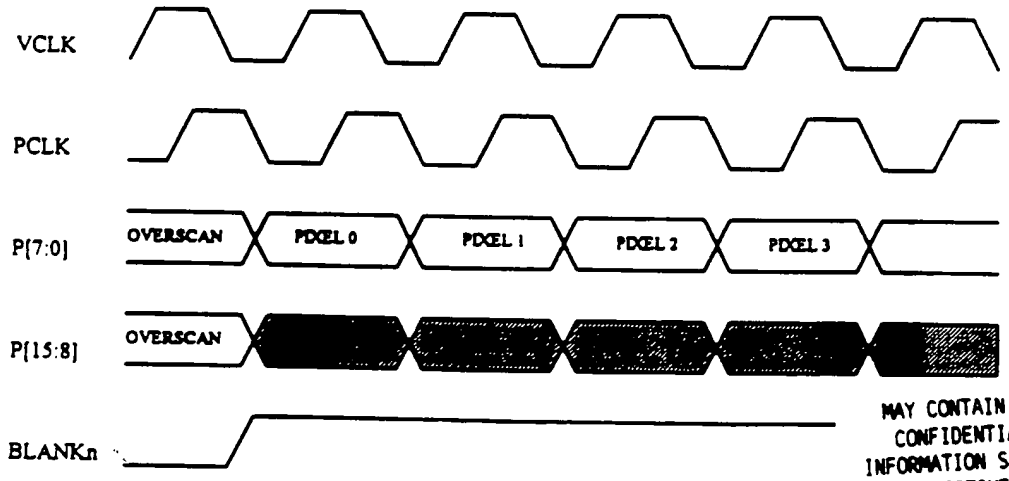
9.4.3 DAC Interface - Attribute Mode 1 (4bpp, 8-bit port)



Notes:

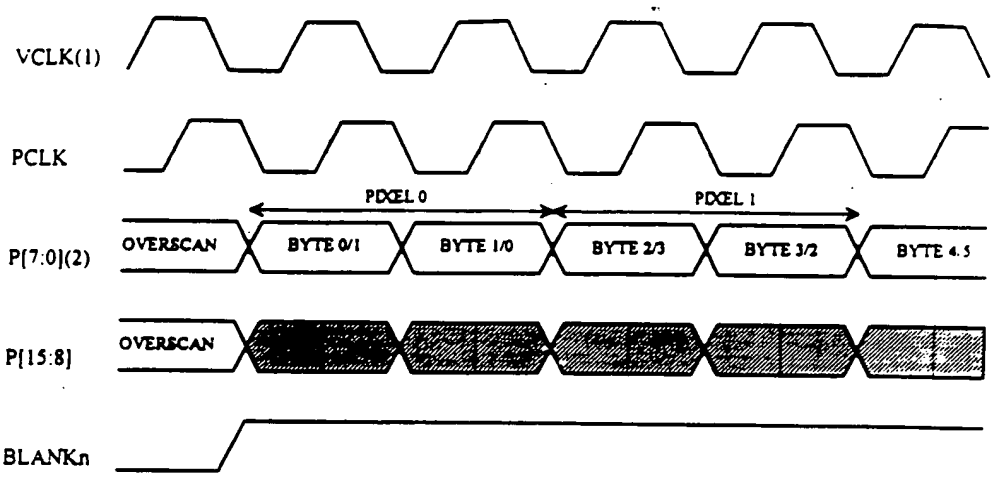
1. The VCLK frequency is only half of the normally required frequency. For example, normal frequency for 1280x1024 70Hz is 135MHz, but it only has to be 67.5MHz for this mode.

9.4.4 DAC Interface - Attribute Mode 2A (8bpp, 8-bit port)



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9.4.5 DAC Interface - Attribute Mode 2B (15/16bpp, 8-bit port)



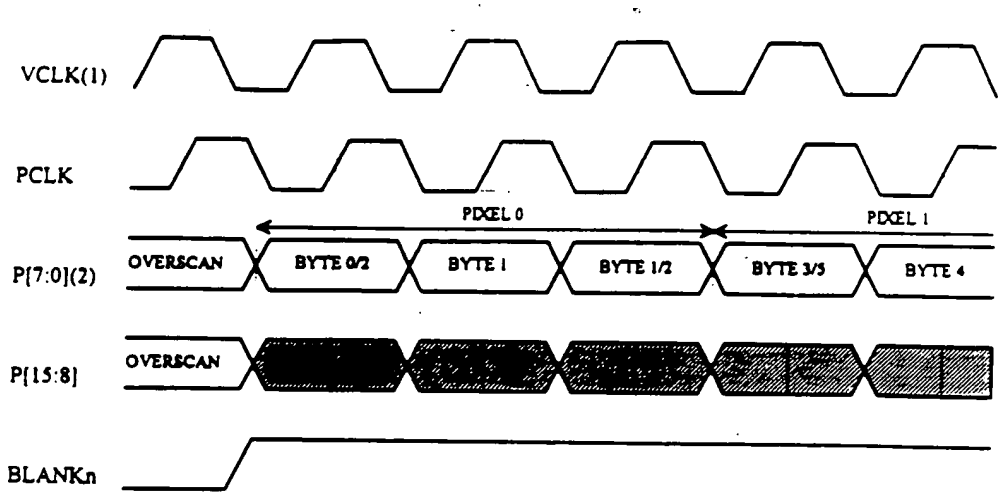
Notes:

1. VLCK frequency is twice that of normally required frequency. For example, the normal frequency for 640x480 60 Hz is 25MHz, but it has to be 50MHz for this mode.
2. The pixel data ordering can be byte 0, byte 1, byte 2, byte 3, ... or byte 1, byte 0, byte 3, byte 2, ..., depending on ER38b4.

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9.4.6 DAC Interface - Attribute Mode 2C (24bpp, 8-bit port)



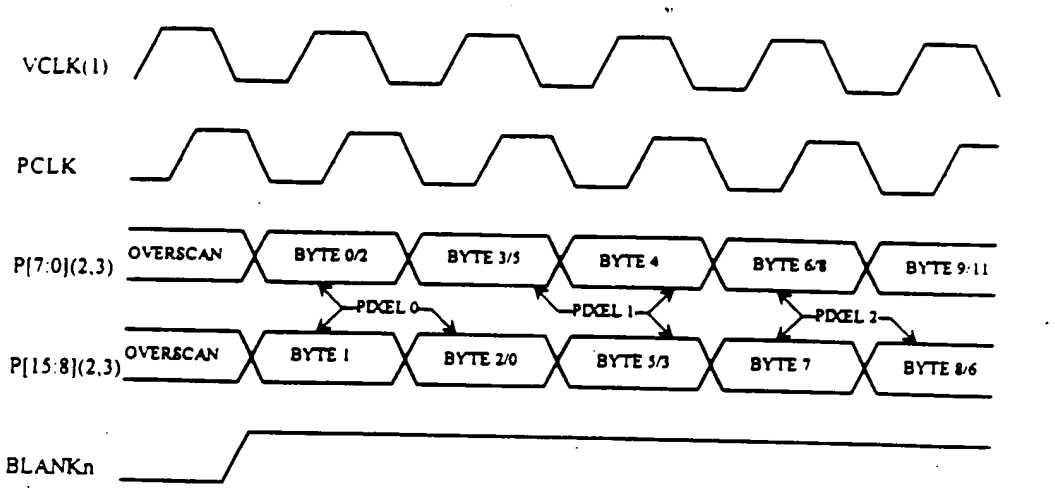
Notes:

1. VLCK frequency is three times that of normally required frequency. For example, the normal frequency for 640x480 60 Hz is 25MHz, but it has to be 75MHz for this mode.
2. The pixel data ordering can be byte 0, byte 1, byte 2, byte 3, byte 4, byte 5 ... or byte 2, byte 1, byte 0, byte 5, byte 4, byte 3, ..., depending on ER38b4.

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9.4.7 DAC Interface - Attribute Mode 3 (24bpp, 16-bit port)



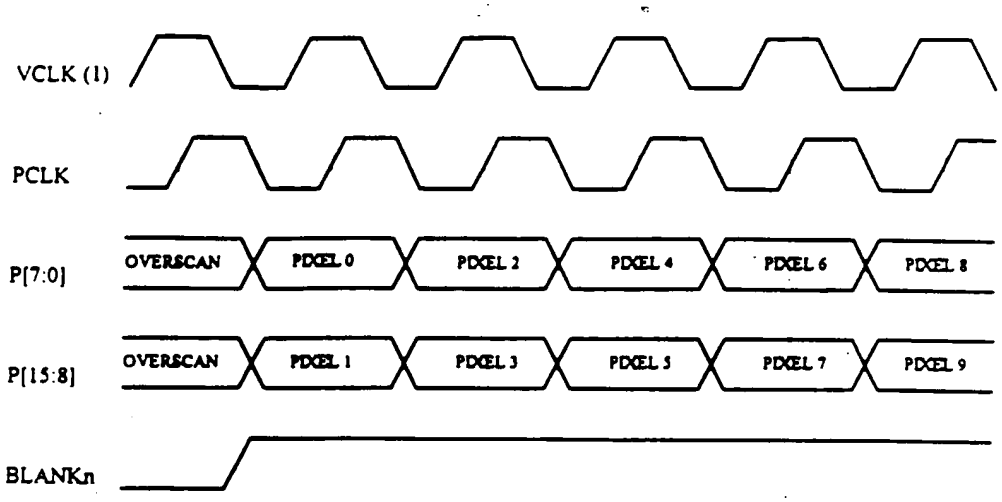
Notes:

1. VLCK frequency is 3/2 times that of normally required frequency. For example, the normal frequency for 640x480 60 Hz is 25MHz, but it has to be 37.5MHz for this mode.
2. The pixel data ordering can be byte 0, byte 1, byte 2, byte 3, byte 4, byte 5 ... or byte 2, byte 1, byte 0, byte 5, byte 4, byte 3, ..., depending on ER38b4.
3. The third byte of a pixel is always on the high byte of P bus (P[15:8]).

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9.4.8 DAC Interface - Attribute Mode 4 (8bpp, 16-bit port)



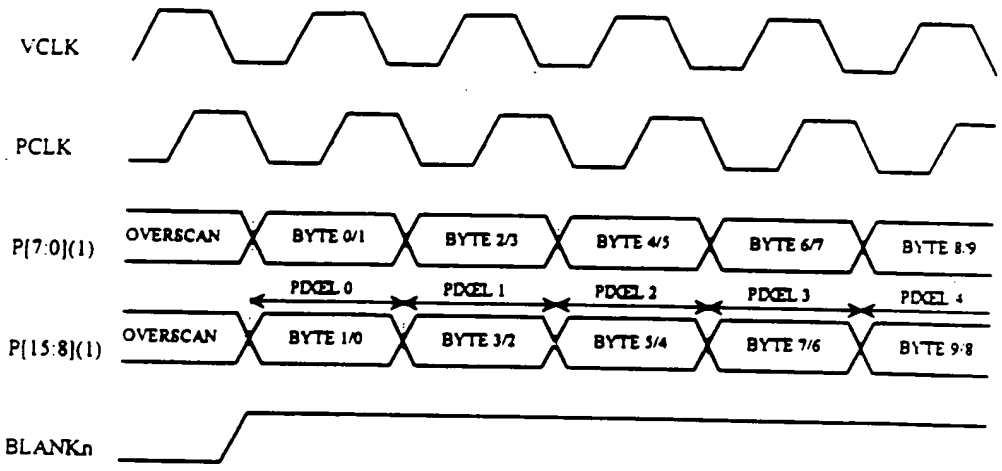
Notes:

1. The VCLK frequency is only half of the normally required frequency. For example, normal frequency for 1280x1024 70Hz is 135MHz, but it only has to be 67.5MHz for this mode.

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9.4.9 DAC Interface - Attribute Mode 5 (15/16bpp, 16-bit port)



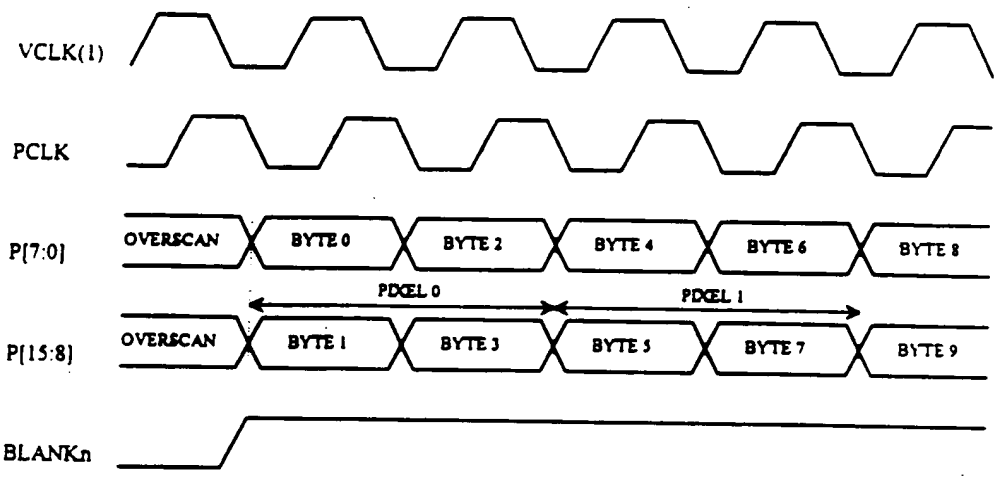
Notes:

1. The pixel data ordering can be byte 0, byte 1, byte 2, byte 3, ... or byte 1, byte 0, byte 3, byte 2, ..., depending on ER38b4.

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9.4.10 DAC Interface - Attribute Mode 6 (32bpp, 16-bit port)



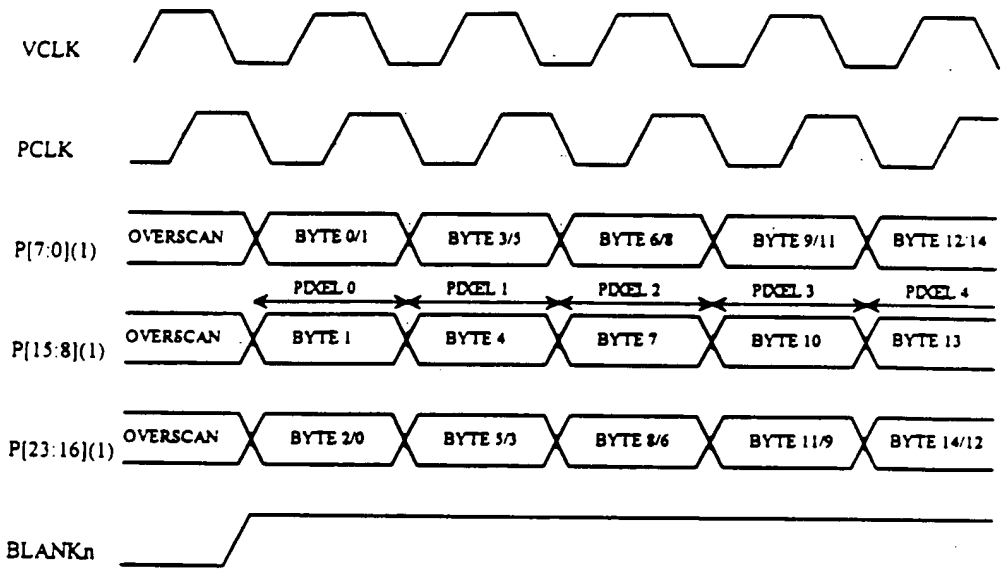
Notes:

1. VLCK frequency is twice that of normally required frequency. For example, the normal frequency for 640x480 60 Hz is 25MHz, but it has to be 50MHz for this mode.

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9.4.11 DAC Interface - Attribute Mode 7 (24bpp, 24-bit port)



Notes:

1 The pixel data ordering can be byte 0, byte 1, byte 2, byte 3, ... or byte 2, byte 1, byte 0, byte 5, ..., depending on ER38b4.

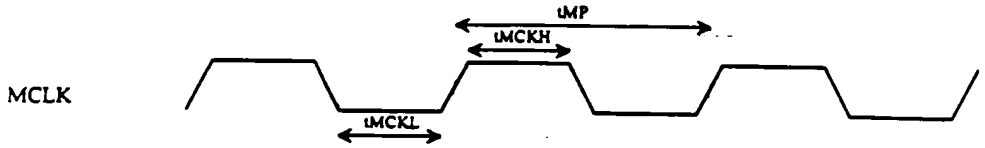
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9.5 Memory Interface Timing

9.5.1 Memory Clock Requirement

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
M1	tMP	Memory Clock Period	15	25		1
M2	tMCKL	Memory Clock Low Time	6			
M3	tMCKH	Memory Clock High Time	6			



Notes:

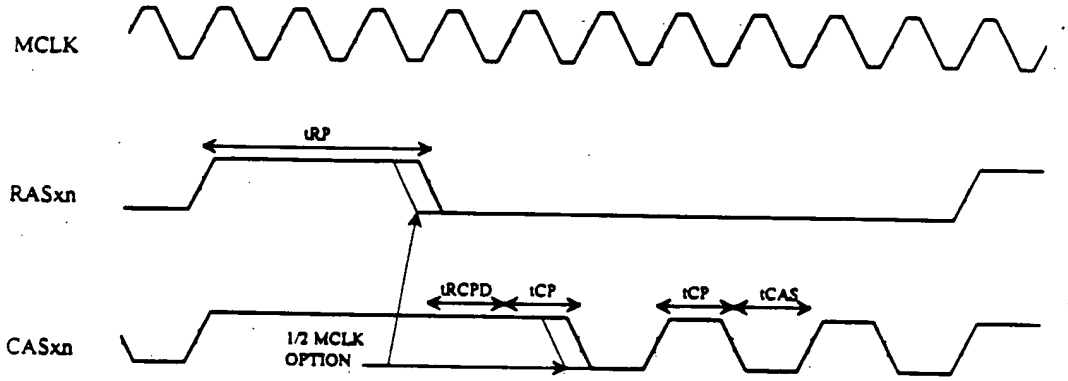
1. The maximum requirement is to guaranteed minimum bandwidth required at MD16 to run normal VGA modes.

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9.5.2 Programmable Parameters

No	Symbol	Parameter	Min (tMP)	Max (tMP)	Register	Notes
M4	tRP	RASxn Precharge	1.5	5	ER26[3.1.0]	
M9	tCP	CASxn Precharge	0.5	2	ER27[1:0]	
M8	tCAS	CASxn Pulse Width	1	2.5	ER27[2:1]	
	tRCPD	RASxn Low to CASxn Precharge Delay	1	4	ER27[5:4]	



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9.5.3 Memory Interface Timing

No	Symbol	Parameter	Min (tMP)	Max (tMP)	Tol. (ns)	Load (pF)	Notes
	tRC	*Random Rd/Wr Cycle time*	*5*	*13*			1
	tPC	*Fast Page Mode Cycle Time*	*2*	*4*			1
	tRAC	*Access Time From RASn*	*3*	*8*			1
	tCAC	*Access Time From CASn*	*1*	*2.5*			1
	tAA	*Access Time From Col. Addr. (MA)*	*2*	*4*			1
	tCPA	*Access Time From CASn Precharge*	*2*	*4*			1
	tOFF	*Output Buffer Turn-off Delay* •••	*1*	*2*			1
M4	tRP	RASn Precharge Time	1.5	5		100	
M5	tRAS	RASn Pulse Width	3	8		100	2
M6	tRSH	RASn Hold Referenced to CASn	1	2		100	
M7	tCSH	CASn Hold Referenced to RASn	3	8		100	
M8	tCAS	CASxn Pulse Width	1	2.5		100	
M9	tCP	CASxn Precharge Time	0.5	2		100	
M10	tRCD	RASxn to CASn Delay Time	1.5	6		100	
M11	tRAD	RASxn to Column Address Delay Time	1	4		100	
M12	tASR	Row Address Setup Time	0.5	1		100	
M13	tRAH	Row Address Hold Time	1	1.5		100	
M14	tASC	Column Address Setup Time	0.5	2		100	
M15	tCAH	Column Address Hold Time	1	2.5		100	
M16	tAR	Column Address Hold Ref. to RASxn	3	8		100	2
M17	tRAL	Column Address to RASn Lead Time	2	4		100	
M18	tWCH	WExxn Hold Ref. to CASxn	1	2		100	
M19	tWCR	WExxn Hold Ref. to RASxn	3	8		100	
M20	tWP	WExxn Pulse Width	1.5	2.5		100	
M21	tRWL	WExxn to RASn Lead Time	1.5	2.5		100	2
M22	tCWL	WExxn to CASn Lead Time	1.5	2.5		100	
M23	tWCS	WExxn Setup to CASxn	0	0.5		100	
M24	tDS	MD Setup to CASxn	1	2		100	
M25	tDH	MD Hold to CASxn	1	2		100	
M26	tDHR	MD Hold Ref. to RASxn	3	8		100	
M27	tCSR	CASn Setup to RASxn (Ref. Cycle)	0.5	1		100	3
M28	tCHR	CASn Hold to RASxn (Ref. Cycle)	2	2.5		100	3

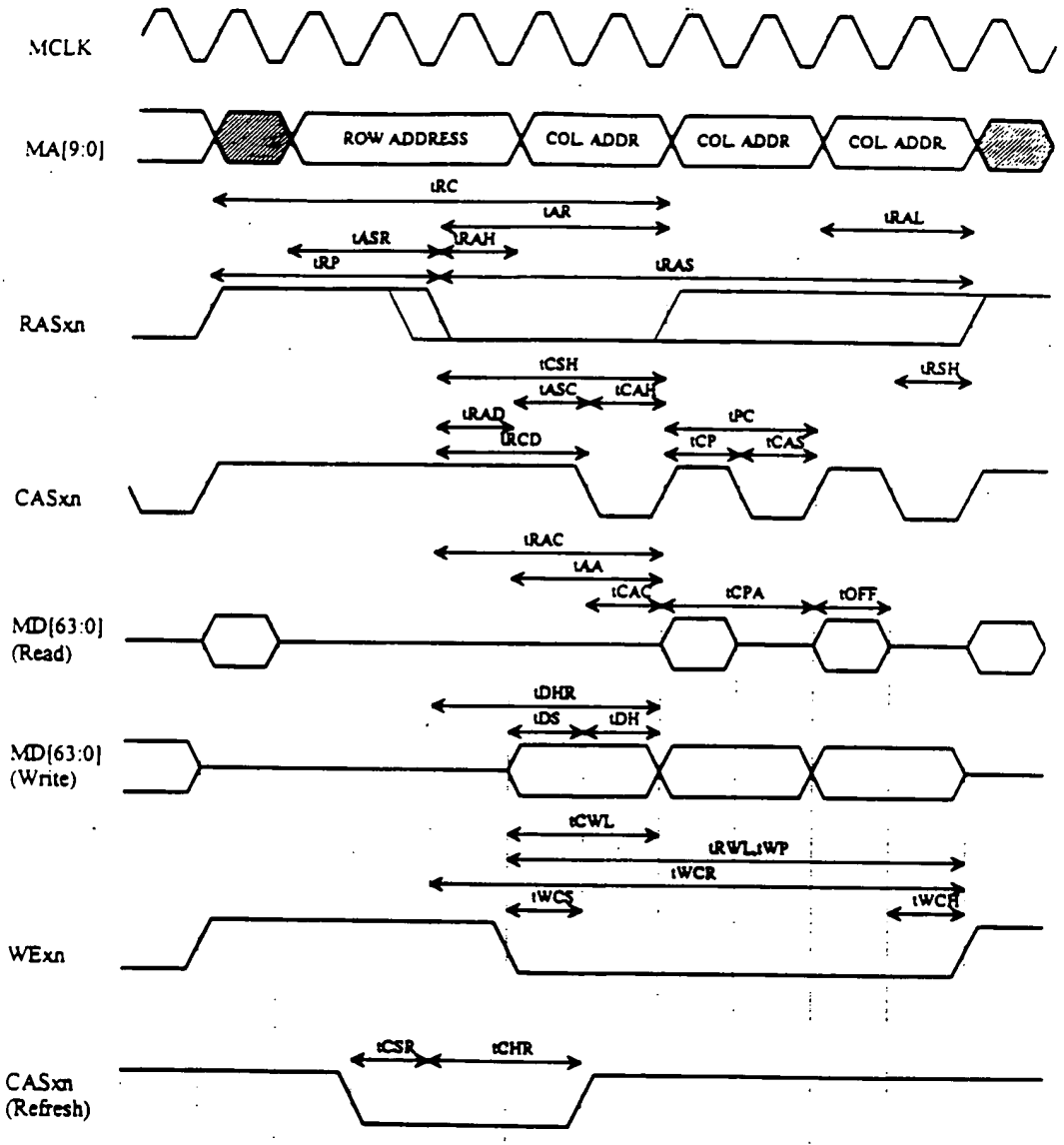
Notes:

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1. These parameters are for reference only.
2. The maximum specified is for maximum programmablefor a single cycle, it is not the absolute maximum.
3. These parameters are for CAS-Before-RAS refresh only.

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Memory Interface Timing



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9.5.4 Standard Memory Design for 70ns & 45ns DRAM's

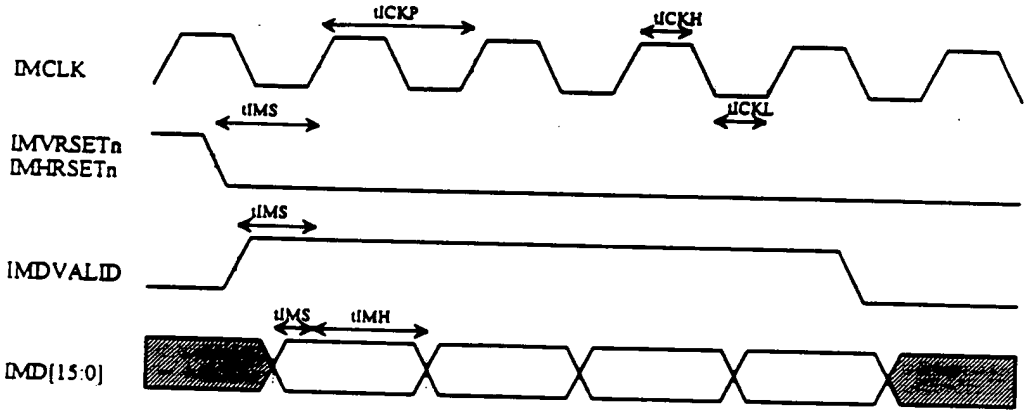
Symbol	Parameter	DS1	50MHz	DS1	50Mhz	DS2	66MHz	DS2	66MHz
	Half clock option	off		on		off		on	
t_{MP}	Memory Clock Period		20		20		15		15
t_{RC}	Random Rd/Wr Cycle time	7	140	7	140	6	90	6	90
t_{PC}	Fast Page Mode Cycle Time	2	40	2	40	2	30	2	30
t_{RAC}	Access Time From RASn	4	80	4	80	3.5	52.5	3.5	52.5
t_{CAC}	Access Time From CASn	1	20	1.5	30	1	15	1.5	22.5
t_{AA}	Access Time From Col. Addr. (MA)	2	40	2	40	2	30	2	30
t_{CPA}	Access Time From CASn Precharge	2	40	2	40	2	30	2	30
t_{OFF}	Output Buffer Turn-off Delay ***	1	20	1.3	25	1.3	18.8	1.3	18.8
t_{RP}	RASn Precharge Time	3	60	3	60	2.5	37.5	2.5	37.5
t_{RAS}	RASn Pulse Width	4	80	4	80	3.5	52.5	3.5	52.5
t_{RSH}	RASn Hold Referenced to CASn	1	20	1.5	30	1	15	1.5	22.5
t_{CSH}	CASn Hold Referenced to RASn	4	80	4	80	3.5	52.5	3.5	52.5
t_{CAS}	CASn Pulse Width	1	20	1.5	30	1	15	1.5	22.5
t_{RCD}	RASn to CASn Delay Time	3	60	3	60	2.5	37.5	2	30
t_{RAD}	RASn to Column Address Delay Time	1	20	1	20	1.5	22.5	1.5	22.5
t_{CP}	CASn Precharge Time	1	20	0.5	10	1	15	0.5	7.5
t_{ASR}	Row Address Setup Time	1	20	1	20	0.5	7.5	0.5	7.5
t_{RAH}	Row Address Hold Time	1	20	1	20	1.5	22.5	1.5	22.5
t_{ASC}	Column Address Setup Time	1	20	0.5	10	1	15	0.5	7.5
t_{CAH}	Column Address Hold Time	1	20	1.5	30	1	15	1.5	22.5
t_{AR}	Column Address Hold Ref. to RASn	4	80	4	80	3.5	52.5	3.5	52.5
t_{RAL}	Column Address to RASn Lead Time	2	40	2	40	2	30	2	30
t_{WCH}	WExxn Hold Ref. to CASn	1	20	1	20	2	30	1.5	22.5
t_{WCR}	WExxn Hold Ref. to RASn	4	80	4	80	3.5	52.5	3.5	52.5
t_{WP}	WExxn Pulse Width	1	20	1.5	30	2	30	1.5	22.5
t_{RWL}	WExxn to RASn Lead Time	1	20	1.5	30	1.5	22.5	1.5	22.5
t_{CWL}	WExxn to CASn Lead Time	2	40	1.5	30	2	30	1.5	22.5
t_{DS}	WExxn Setup to CASn	1	20	0	0	1	15	0.5	7.5
t_{DS}	MD Setup to WExxn	1	20	0.5	10	1	15	0.5	7.5
t_{DH}	MD Hold to WExxn	1	20	1.5	30	1	15	1.5	22.5
t_{DHR}	MD Hold Ref. to RASn	4	80	4	80	3.5	52.5	3.5	52.5
t_{CSR}	CASn Setup to RASn (Ref. Cycle) (3)	1	20	1	20	0.5	7.5	0.5	7.5
t_{CHR}	CASn Hold to RASn (Ref. Cycle) (3)	2	40	2	40	2.5	37.5	2.5	37.5
t_{RMW}	Read-Modify-Write Cycle Time	10	200	10	200	9	135	9	135
t_{PRMW}	Page Read-Modify-Write Cycle Time	5	100	5	100	5	75	5	75

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9.6 Imaging Interface Timing

9.6.1 Imaging Input Port Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pf)	Notes
IM1	tICKP	Imaging Clock Period	30			
IM2	tICKL	Imaging Clock Low Time	10			
IM3	tICKH	Imaging Clock High Time	10			
IM4	tIMS	Imaging Input Setup to IMCLK	4			
IM5	tIMH	Imaging Input Hold to IMCLK	4			

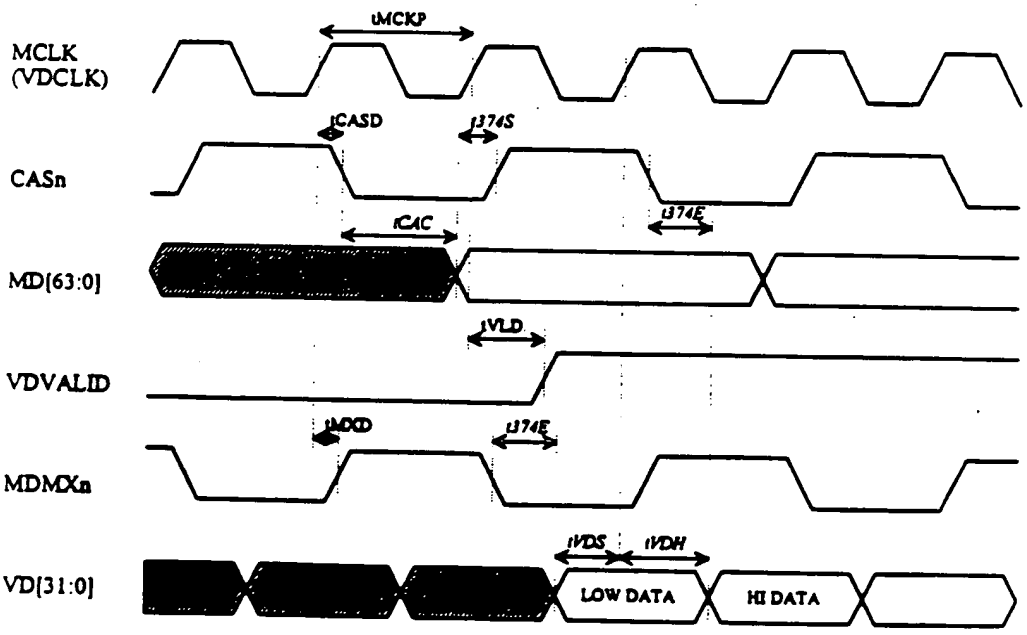


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9.6.2 Imaging Output Port (Video Window) Timing - MD64

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pf)	Notes
IM6	tICKP	Video Window Clock Period	15			
IM7	tCASD	CASxn Delay from MCLK		10	50	1
IM8	tMDXD	MDMXn Delay from MCLK		10	50	1
IM9	tVLD	VDVALID Delay from MCLK		10	50	
	tCAC	*MD[63:0] Valid from CASxn*		*tCAS-2*	50	
	tVDS	*Video Data Setup to MCLK*	*3*			2
	tVDH	*Video Data Hold from MCLK*	1			
	t374S	*MD[63:0] Setup to CASxn (Setup of 374)*		*2*	*50*	
	t374C	*VD[31:0] Delay from CASxn (374 clock to data delay)*		*2*	*50*	
	t374E	*VD[31:0] Delay from CASxn/MDMXn (374 En to data delay)*		*7*	*50*	



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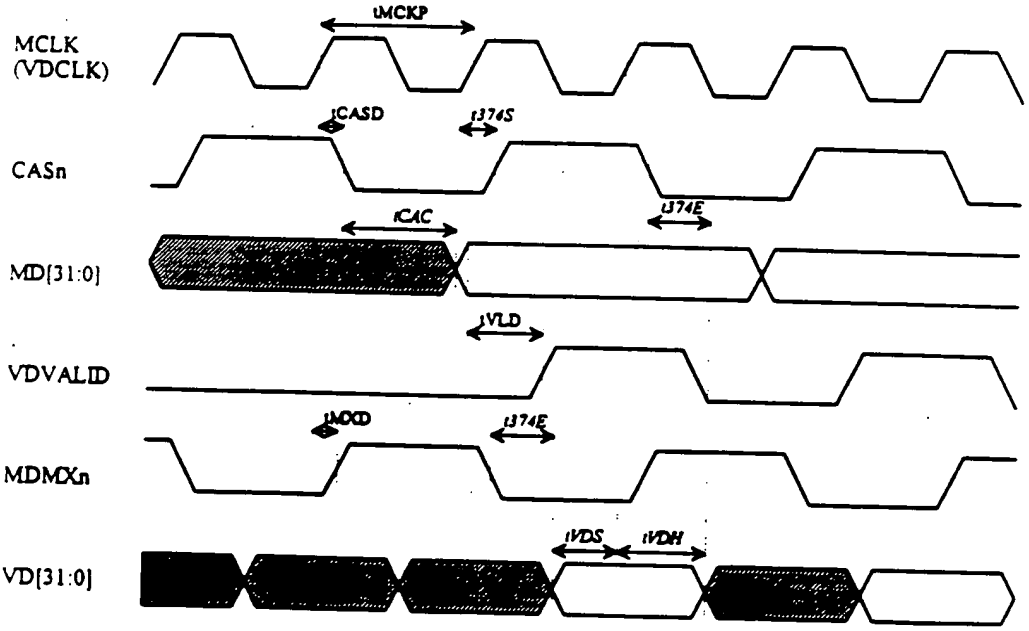
Notes:

1. The delays of these two signals should match to avoid fighting on VD[31:0].
2. tVDS=tMDXD+t374E or tCASD+t374C, whichever is worst. To improve tVDS, MCLK can be buffered to generate VDCLK.

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9.6.3 Imaging Output Port (Video Window) Timing - MD32

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pf)	Notes
IM6	tICKP	Video Window Clock Period	15			
IM7	tCASD	CASxn Delay from MCLK		10	50	1
IM8	tMXD	MDMXn Delay from MCLK		10	50	1
IM9	tVLD	VDVALID Delay from MCLK		10	50	
	tCAC	*MD[63:0] Valid from CASxn*		*tCAS-2*	50	
	tVDS	*Video Data Setup to MCLK*	*3*			2
	tVDH	*Video Data Hold from MCLK*	1			
	t374S	*MD[63:0] Setup to CASxn (Setup of 374)*		*2*	*50*	
	t374C	*VD[31:0] Delay from CASxn (374 clock to data delay)*		*2*	*50*	
	t374E	*VD[31:0] Delay from CASxn/MDMXn (374 En to data delay)*		*7*	*50*	



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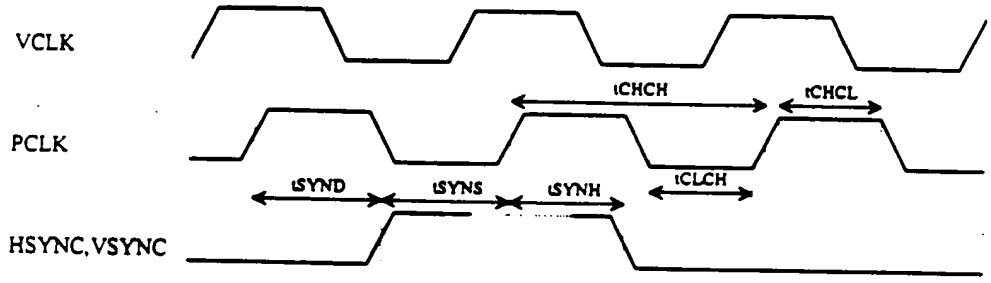
Notes:

1. The delays of these two signals should match to avoid fighting on VD[31:0].
2. tVDS=tMXD+t374E or tCASD+t374C, whichever is worst. To improve tVDS, MCLK can be buffered to generate VDCLK.

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9.7 VAFC Interface Timing

No	Symbol	Parameter	Min (ns)	Max (ns)	Load (pF)	Notes
VAFC1	tCHCH	Pixel Clock Period	26.6		50	1
VAFC2	tCLCH	Pixel Clock Low Time	11		50	1
VAFC3	tCHCL	Pixel Clock High Time	11		50	1
VAFC4	tSYND	HSYNC/VSYNC Delay from PCLK	2	15	50	2
VAFC5	tSYNS	HSYNC/VSYNC Setup to PCLK	10		50	1,3
VAFC6	tSYNH	HSYNC/VSYNC Hold to PCLK	2		50	1,3



Notes:

1. For reference only, not to be tested. These parameters are guaranteed from the DAC interface section.
2. The maximum parameter is required to guarantee parameter tSYNS, and the minimum is required for tSYNH.
3. This parameter is tCHCH-tSYND

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